



A high-precision amplitude-time-to-digital converter based on an FPGA for a digital multichannel analyzer

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Abstract

This paper presents a high-precision amplitude-time-to-digital converter (A-TDC) for use in a multichannel analyzer (MCA). With this method, the MCA quantifies and statistically analyzes the discharge time of nuclear pulse signals, ultimately reconstructing the gamma-ray energy spectrum. The autonomous linear discharge circuit presented in this paper significantly simplifies conventional discharge circuitry and its associated control logic. By leveraging the underlying logic of the FPGA's internal carry chain, a delay chain capable of precise time measurement for both leading and trailing edges is implemented. Compared with implementations employing separate delay chains for leading and trailing edges, this approach significantly conserves logic resources. The high-resolution TDC implemented on a Xilinx Artix-7 series FPGA exhibits a resolution of 69.4 ps, and the average time measurement precision is 52.3 ps. The linear discharge circuit has an inherent nonlinearity of less than 0.05 %, and its overall linearity is better than 0.1 %. When used in conjunction with a $\Phi 25 \text{ mm} \times 25 \text{ mm}$ NaI(Tl) detector to measure the 662 keV full-energy peak of a ^{137}Cs source, an energy resolution of 8.5 % is achieved.

Keywords Amplitude-to-time conversion · FPGA-TDC · Gamma-ray energy spectrum · Constant-current discharge

1 Introduction

Digital multichannel analyzers (MCAs) have been extensively used in fields such as nuclear spectroscopy, environmental monitoring, nuclear accident response, and mineral resource exploration [1–7]. Digital pulse-amplitude analyzers typically employ high-speed ADCs for full-waveform sampling of the pulse signal, followed by devices such as field-programmable gate arrays (FPGA) and digital signal processors (DSPs) to perform digital filtering, pulse shaping, and amplitude extraction [8, 9]. Applications requiring amplitude measurements across dozens, hundreds, or even thousands of channels include multichannel energy spectrum measurements, gamma irradiation imaging, and astronomical telescopes [10–14]. In such systems, the ADC circuit design is highly complex. These systems typically require a large number of high-speed ADC chips to accurately

acquire nuclear information. However, high-speed ADCs are expensive, and circuit complexity increases rapidly as the number of channels grows. Moreover, owing to large inter-channel variations in signal strength, ADCs must provide a high dynamic range to accommodate signals of different amplitudes [15–17].

Time-to-digital converters (TDCs) have been used in various fields, such as high-energy particle measurement and phase-locked loops, since the 1980s [18–21]. TDC technology has transitioned from analog to digital [22], and researchers have investigated Vernier, passive interpolation, and gated ring oscillator TDC architectures to improve timing resolution and measurement range. Some of these structures can achieve time resolution at the subgate level, and in certain applications, they can reach femtosecond (fs)-level timing resolution [23–29].

TDCs are primarily implemented using application-specific integrated circuits (ASICs) and FPGAs. TDC systems based on ASICs offer better channel stability and consistency; however, ASIC devices are complex to design and have high development costs. In contrast, FPGA-based TDCs offer a short design cycle, high flexibility, low cost,

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and high temporal resolution. Some designs can achieve a picosecond-level resolution [30–34].

The amplitude of the pulse signal output from the detector is proportional to the energy deposited by the radiation or particles therein. The pulse peak is stored in a holding capacitor using a pulse peak detection and hold circuit. Subsequently, a constant-current source discharges the holding capacitor at a uniform rate, and the discharge time is proportional to the pulse amplitude. The deposited radiation energy can therefore be accurately inferred from the measured discharge time.

Given the strong competitiveness of FPGA-based high-precision TDC pulse-amplitude analyzers in fields such as high-energy physics, radiation imaging, multichannel energy spectrum measurement, and gamma irradiation imaging [35, 36], this paper proposes an amplitude-time-to-digital converter (A-TDC) for pulse-amplitude measurement.

2 System design

A high-precision FPGA-based A-TDC primarily consists of an analog signal-conditioning circuit and an on-chip TDC module. The signal-conditioning stage performs gain adjustment, peak holding, constant-current discharge, and pulse-width conversion. The FPGA-based TDC comprises a fine counter, a coarse counter, and a processing unit. After appropriate gain adjustment, the nuclear pulse signal output from the NaI(Tl) detector is routed to the peak-holding and constant-current discharge unit. This unit converts the nuclear pulse signal into a single-slope pulse whose width is proportional to the signal peak amplitude. Subsequently,

a comparator converts the single-slope pulse into a square-wave signal, which preserves the amplitude information in the time domain and is digitized by the TDC through combined fine timing (delay chain-based) and coarse counting within the FPGA.

2.1 Automatic peak-holding and constant-current discharge

In low-channel discharge measurement systems, typical components include decision-making circuits, linear gates, and constant-current discharge circuits. These components are further coordinated using dedicated switching networks to control the discharge process [37, 38]. However, in multichannel measurement systems, implementing an independent discharge-control circuit for each channel substantially increases circuit complexity and complicates system-level control logic. Accordingly, to support multichannel operation while simplifying control logic and reducing circuit complexity, this study adopts an automatic peak-holding and constant-current discharge scheme, as shown in Fig. 1a.

After gain adjustment, the nuclear pulse signal is applied to the automatic peak-holding and constant-current discharge circuit. Owing to the direct-current (DC) bias supply V_b and diodes D_1 and D_2 , the incoming pulse charges the peak-holding capacitor C_h . The charge stored on C_h is proportional to the signal peak, expressed as $Q(t) = C \cdot V(1 - e^{-t/\tau})$. A constant-current discharge path is established through transistors Q_1 and resistors R_{dis} , R_1 , and R_2 . Based on the base-emitter characteristics of the NPN (negative-positive-negative) transistor, V_b provides a stable

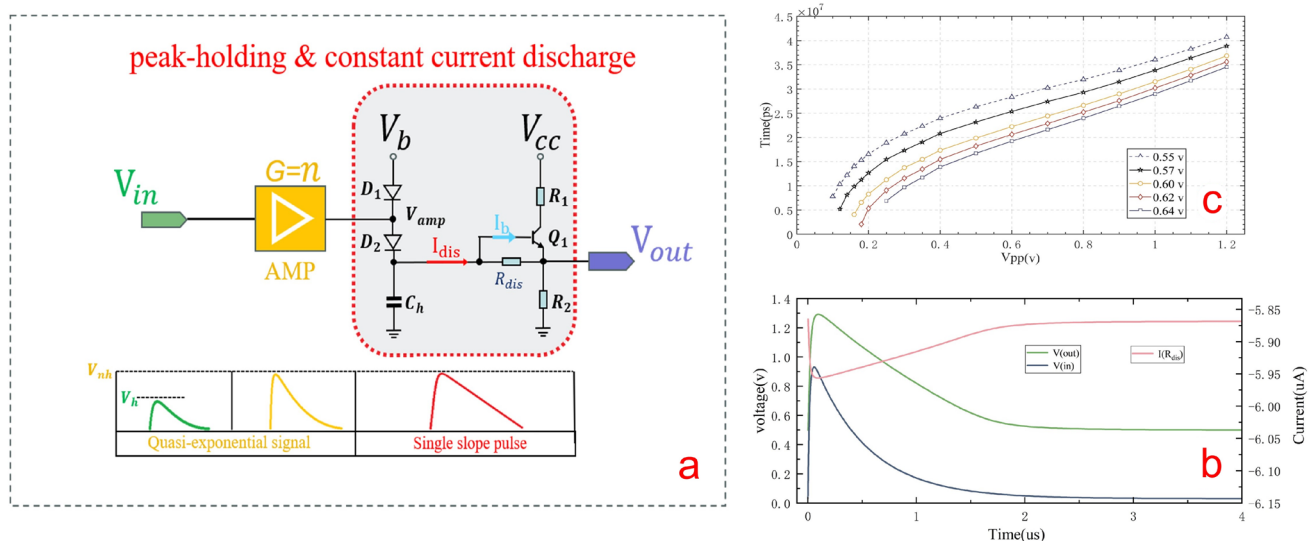


Fig. 1 (Color online) **a** Schematic diagram of peak-holding and constant-current discharge, **b** the circuit simulation of the rapid charge and the constant discharge process, **c** test results of amplitude-time conversion at different comparator threshold levels

operating bias for Q_1 following the voltage drop across the two diodes, ensuring operation in the active region during the discharge. Consequently, the base-emitter voltage V_{be} remains approximately constant at 0.6 V. During the discharge, the fluctuation in the base current of Q_1 remains below $0.05 \mu\text{A}$; therefore, its influence can be neglected. By connecting resistor R_{dis} between the base and emitter of Q_1 , the discharge current from C_h is forced through R_{dis} . Because V_{be} remains nearly constant, the discharge current is approximately $I \approx \frac{V_{be}}{R_{dis}}$, thereby realizing constant-current discharge.

Upon arrival of the nuclear pulse signal, capacitor C_h undergoes swift charging. Because of the exceptionally brief rise time of the nuclear pulse signal, the voltage across C_h rapidly reaches the peak value of the signal. The presence of V_b positions transistor Q_1 within its active region. Simultaneously, as the input nuclear pulse signal charges C_h , the constant-current discharge circuit operates concurrently. Consequently, a minor charge loss occurs during the charging phase, leading to a divergence between the peak voltage achieved by the capacitor C_h and the peak value V_{amp} of the nuclear pulse signal. This discrepancy is influenced by both the rise time of the nuclear pulse signal and the magnitude of the discharge current.

Using the NaI(Tl) detector as an illustrative example, the input signal rise time ranges from 100 to 300 ns. With a constant discharge current of $6 \mu\text{A}$ and an input amplitude of 1 V, the resulting peak voltage reduction is approximately 60 mV. Therefore, constant-current discharge introduces a peak deviation of approximately 6 %, which has a negligible effect on amplitude-to-time conversion accuracy. To maintain a uniform discharge trajectory, diode D_2 is placed above C_h . During the slow discharge of C_h , D_2 remains reverse biased, allowing current to flow only toward the subsequent stage. Consequently, the discharge current I_{dis} governs the entire discharge rate. The peak-holding and constant-current discharge circuit therefore converts the input nuclear pulse into a single-slope pulse.

The circuit simulation results, shown in Fig. 1b, indicate the presence of a small nonlinear region near the end of the discharge process, primarily arising from the current-voltage characteristics of the diode. When the applied forward voltage is below the diode threshold, the device exhibits high impedance and negligible forward current. As the forward voltage slightly exceeds the threshold, the built-in electric field of the PN junction is progressively neutralized, and the diode enters the forward-conduction region. During this transition, voltage and current are not strictly proportional. With further increase in forward bias, the diode current rises rapidly and the voltage-current characteristics become approximately linear, corresponding to full conduction. In this regime, the forward voltage drop across the diode

remains nearly constant. As observed in the simulation diagram, fluctuations in the discharge current I_{dis} remain below $0.1 \mu\text{A}$, while the nominal discharge current is $5.875 \mu\text{A}$. Experimental measurements show that for signals with peak-to-peak amplitudes of 0.4 V or greater, the inherent nonlinearity is less than 0.05 %, and the overall linearity is better than 0.1 %. These results demonstrate that the system exhibits good amplitude-to-time linearity over the effective operating range, as illustrated in Fig. 1b.

The signal transformation circuit converts the single-slope pulse signal into a square-wave signal that complies with the FPGA input levels, thereby facilitating the measurement of the pulse-width time. The transformation circuit employs a comparator to perform a threshold comparison of the single-slope pulse signal output from the previous stage, converting it into a square-wave signal. The comparator bandwidth determines the range of signal frequencies to which it can respond. If the bandwidth is insufficient, it results in an increased setup time for the output signal and a longer rise time for the leading edge of the output signal. A longer leading edge can increase the uncertainty in TDC time measurements. Therefore, it is necessary to select a high-speed comparator to ensure the resolution and accuracy of the system measurements.

The DC bias voltage V_b introduces a DC offset of approximately 0.53 V for the signal. Because the total analog noise level is below 10 mV, the comparator threshold must exceed 0.54 V to prevent noise-induced errors during pulse-width conversion. To evaluate the dependence of pulse-width conversion performance on comparator threshold, input amplitudes from 0.1 to 0.2 V were sampled at 20 mV intervals; from 0.2 to 0.4 V at 50 mV intervals; and from 0.4 to 1.2 V at 100 mV intervals. More than 100,000 samples were acquired at each test point. Additional measurements were conducted using comparator thresholds of 0.55 V, 0.57 V, 0.60 V, 0.62 V, and 0.64 V, selected relative to the discharge baseline. The corresponding results are presented in Fig. 1c.

As shown in Fig. 1c, when the input peak-to-peak amplitude is below 0.4 V, the relationship between the input signal amplitude and discharge time deviates from linearity. The primary reason for this phenomenon can be attributed to the voltage-current (V - I) characteristics of diodes. In an ideal diode, forward current increases abruptly once the forward voltage exceeds the conduction threshold. In practice, however, when the forward voltage is near the critical conduction voltage of the diode, the diode exhibits soft conduction. This implies that when the forward voltage difference across the diode is slightly greater than the critical conduction voltage, the current does not undergo an abrupt change as per ideal diode characteristics; instead, it displays a nonlinear, smooth transition. Owing to this soft conduction characteristic, when the peak-to-peak value of the input signal is

relatively small, the relationship between V_{pp} (peak-to-peak voltage) and discharge time is not strictly linear.

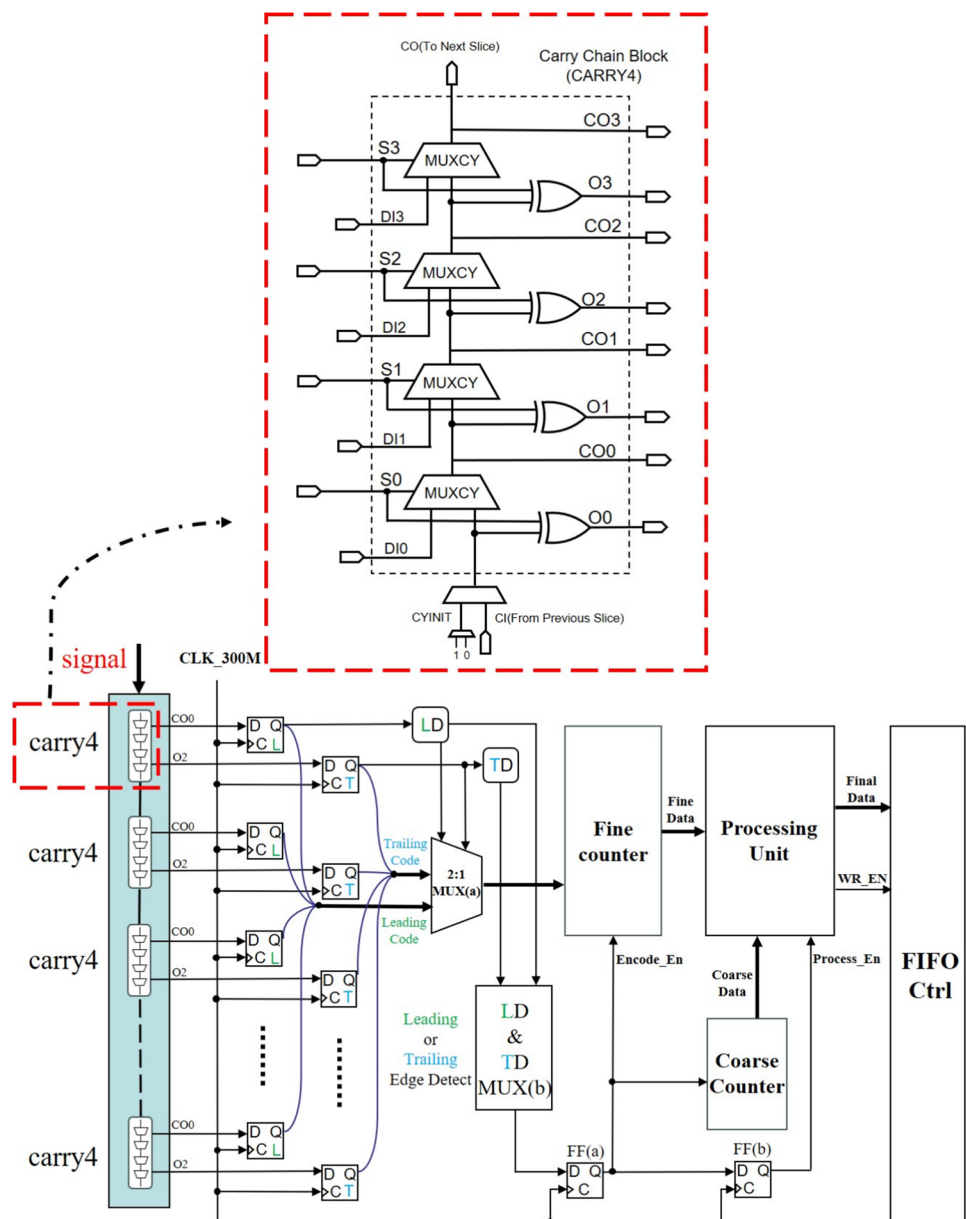
2.2 FPGA-TDC design

The direct counting method uses a high-frequency clock to measure the width of the input signal. When the leading edge of the input signal arrives, the FPGA initiates counting and halts upon arrival of the trailing edge. The pulse width of the input signal can be determined by calculating the number of clock cycles that elapse between the start and end times. Direct measurement of the pulse width using clock counts offers a wide measurement range, but the clock

period introduces quantization errors at both the leading and trailing edges.

This study uses the internal carry chain of an FPGA to construct a fine delay chain that precisely measures the leading and trailing edges of the pulse. A high-frequency clock is employed for coarse counting of the main pulse width, and the two counts are subsequently combined to obtain the total pulse width. The carry chain is a fundamental FPGA structure. In the Xilinx Artix-7 series FPGA, the structure of the CARRY4 (Carry Chain Block 4) is depicted in Fig. 2. Each CARRY4 consists of a carry multiplexer (MUXCY) and XOR gates, which together generate carry signals. The CI (carry input) is connected to the carry output of the previous stage, whereas the carry output (CO) serves as the

Fig. 2 (Color online) Fast carry logic paths and related components in the A7 series FPGAs



output of the current CARRY4. Signal S controls the output of the MUXCY.

This design establishes delay chain-based timing measurement by cascading CARRY4 units, capturing the internal tap signals, and extracting the fine timing values through encoding and decoding.

By configuring S[3:0] of CARRY4 to 1111, the four MUXCY input signals are configured to select the cascaded carry path, linking the carry-out (CO) with CI (Carry-In) and forming a single CARRY4 delay module. Within this module, carry propagation from CI to CO constitutes the minimum delay unit of the chain.

Within the CARRY4 chain, the tap signals are taken from O[3:0] and CO[3:0]. Upon arrival of the leading edge of the measured signal, each MUXCY stage drives its corresponding CO output from “0” to “1”. Conversely, when the trailing edge arrives, O becomes the XOR result of S and the carry signals. Given that S is set to 1, O also transitions from “0” to “1”. Consequently, the sensitivity of the CO and O tap signals to the leading and trailing edges of the measured signal can be used to determine the precise moment of the square-wave signal’s edge. This capability allows for simultaneous measurement of both the leading and trailing edges of the signal using a single delay chain.

Figure 2 illustrates the specific design approach of FPGA-TDC, which incorporates a fine counter to measure the temporal segments at both the leading and trailing edges of the signal. In the initial delay unit, two delay flip-flops (TD and LD) are inserted to indicate valid leading and trailing edges. After a one-clock delay, the signal branches into two paths: one path feeds MUX(a) to select the encoded leading or trailing edge, while the other path passes through MUX(b) to select the corresponding latch signal. After passing through the flip-flop FF(a), the latch signal captures the encoder output and simultaneously serves as the start and stop signals for the coarse counter.

The latch signal, after traversing flip-flop FF(b), generates the enable signal “Process_En” for the processing unit. Upon reaching the processing unit, “Process_En” combines the latched fine-count value with the coarse count to produce the final timing data, which are written to the FIFO. No additional clocks are required during encoding or data processing. Therefore, the longest delay path spans from edge detection to FIFO writing, consuming two system clock cycles. Consequently, the TDC designed in this study has a maximum dead time of two clock cycles, significantly reducing the system dead time attributed to the TDC during measurement. In the A7 series FPGAs, each clock region contains 50 slices, corresponding to 50 CARRY4 resources. The theoretical CI-to-CO delay of each CARRY4 is approximately 98 ps [39], although practical measurements indicate a shorter value. Prior to delay chain implementation, the number of delay units must remain below 50 to prevent the

chain from crossing clock regions, which would introduce nonuniform delays.

The encoder module converts the time signal into a digital signal code, resulting in a thermometer code whose bit width is equivalent to that of the carry chain (e.g., “11111...00000”). In the processing unit, which includes a thermometer code decoding circuit, the time value is derived by counting the “1”s in the thermometer code. To improve FPGA resource utilization and reduce system dead time, a binary search algorithm is adopted for decoding the thermometer code. This method offers favorable time and space complexity, allowing rapid identification of the transition point from “0” to “1” [40].

Most detector outputs fall within the system dynamic range. However, a small fraction exhibit amplitudes below the lower limit of the dynamic range, particularly pulses with widths shorter than half the sampling clock period. For these signals, the TDC measurement circuit may detect only one edge (leading or trailing), resulting in inaccurate measurements. To address this issue, an event-assembly circuit implemented as a finite-state machine (within the processing unit shown in Fig. 2) screens detected events to ensure data integrity and completeness.

2.3 TDC performance test

2.3.1 TDC code density and nonlinearity test

Owing to the influence of manufacturing processes and layout routing, it is difficult for each delay unit in the FPGA’s carry chain to have exactly the same delay time. Therefore, it is necessary to calibrate the delay time of each delay unit precisely in advance. To achieve this goal, the standard code density test method [41, 42] is typically used to measure the delay characteristics of each delay unit.

A large number of pulses with randomly varying widths uniformly distributed within $[0, T]$ were used as test signals for the TDC (where T is the period of the standard system clock). If the delay times of each delay element are the same and there are sufficient test samples, the number of signals falling on each delay element should be evenly distributed. However, as the delay time of each delay element varies, the uneven distribution of signals across the delay elements is determined by variations in their delay times. By recording the total number of times each delay element was hit by an event, the corresponding code density for each delay element can be determined.

Assuming that there are sufficient test samples and ignoring the non-uniform distribution factors of the input signal, the delay time of each delay element is proportional to the number of pulses that fall into it. This implies that the more times a random input signal falls into a particular delay unit, the longer its delay time and the greater its code density.

Because the sum of the delay times of all delay units equals one reference clock cycle, the delay time of each delay unit within the delay period T can be determined by multiplying the proportion of the code density occupied by each delay unit by the sampling period T .

To ascertain the precision and dependability of measurement outcomes, it is imperative to establish the required number of test samples before conducting the tests. Suppose that the range of values for the individual pulse signals is uniformly distributed across the interval $[0, T_c]$, where P represents the probability density function, expressed as $P = \frac{T_i}{T_c}$. The likelihood of a pulse occurring within a specific delay element is directly proportional to the delay time T_d of that element, with probability given by $P_d = \frac{T_d}{T_c}$. Given N events, the frequency of occurrence of the delay element i is denoted by $n_i = NP_i = N \frac{T_i}{T_c}$.

By leveraging the relationship between the density of the delay element codes and the sampling interval, the delay time $\hat{T}_i$ for the i -th delay element can be derived as shown in Eq. 1.

$$\hat{T}_i = \frac{n_i}{N} T_c \quad (1)$$

By tallying the number of events N_i that occur in each successive delay element, we can ascertain the delay times for all the elements. Subsequently, the sum of the delay times of the initial i elements yields the cumulative delay time t_i experienced by the pulse as it reaches each specific delay element, as detailed in Eq. 2.

$$t_i = \sum_{n=1}^i \hat{T}_i = \sum_{n=1}^i \frac{n_n}{N} T_c \quad (2)$$

In practice, the edge of the test signal falls within the interior of the i delay element; therefore, an error exists, regardless of whether t_i or t_{i-1} is selected as the total delay time. Assuming that the measured value is τ , then $t_{i-1} < \tau < t_i$ and the variance σ^2 of τ is

$$\sigma^2 = \frac{1}{t_i - t_{i-1}} \int_{t_{i-1}}^{t_i} (t - \tau)^2 dt = \frac{(t_i - \tau)^3 - (t_{i-1} - \tau)^3}{3(t_i - t_{i-1})}. \quad (3)$$

In Eq. 3, variance σ^2 reaches its minimum value when $\tau = \frac{t_i + t_{i-1}}{2}$. At this point, the observed value is t , as expressed in Eq. 4.

$$t = \sum_{n=1}^{i-1} \tilde{T}_n + \frac{1}{2} \hat{T}_i = \sum_{n=1}^{i-1} \frac{n_n}{N} T_c + \frac{1}{2} \frac{n_i}{N} T_c \quad (4)$$

Therefore, when a random signal falls within a delay element, the measured value should be taken at the midpoint of the delay element to minimize the standard deviation.

From Eq. 4, it is evident that an inadequate sample size results in excessive statistical errors, necessitating a specific requirement for the sample size in code density testing. For a finite number N of test events, the event count n_i , where the test pulse edge falls within a delay element, follows a binomial distribution $D(n_i) = NP_i(1 - P_i)$ with the expected value $\bar{n} = N \times P_i$ and the standard deviation $\sigma_{n_i} = \sqrt{NP_i(1 - P_i)}$.

Because all the events are independent, the count values n_i are also independent. Therefore, using Eq. 2 and 4, Eq. 5 is obtained.

$$\sigma_i = \sqrt{\sum_{n=1}^{i-1} \sigma^2 T_n + \frac{1}{4} \sigma^2 T_i} = \sqrt{\sum_{n=1}^{i-1} \sigma^2 n_n + \frac{1}{4} \sigma^2 n_i} \quad (5)$$

If the delay times of each delay element are equal, then the probability of a pulse falling on the i th delay element is $P_i = \frac{1}{S}$, where S is the number of delay elements in a delay chain. When $i = S$, i is the last delay element in the delay chain and σ_i reaches its maximum value, $\sigma_{\max}$.

$$\sigma_{\max} < \frac{T_c}{N} \sqrt{S \sigma n_d^2} = \frac{T_c}{N} \sqrt{1 - \frac{1}{S}} \leq \frac{T_c}{\sqrt{N}} \quad (6)$$

Given that the external signal sampling clock designed in this study was 250 MHz, we have $T_c = 4000$ ps. To ensure that $\sigma_{\max}$ does not exceed 40 ps, we set $\sigma_{\max} = 40$ ps. Substituting this value into Eq. 6, we obtain $N \geq 10000$, which implies that the number of test events must not be less than 10000.

Hence, a signal generator was employed to generate 20,000 random pulse-width square waves. The external and measurement sampling clocks should not be sourced from the same origin, and they should not be in an integer-multiple relationship, as this would result in a fixed phase between them, which is inadequate for achieving complete randomness. The sampling clock was a 300 MHz clock generated by a PLL from an external crystal oscillator with a period of 3.33 ns. According to the theoretical delay of 98 ps, 34 CARRY4 delay elements are required. However, after testing with random signals, we found that at a clock frequency of 300 MHz, the actual delay time of each CARRY4 delay element was less than 98 ps. Therefore, for both the leading and trailing edges, there are 48 delay elements, which is fewer than the maximum number of delay elements per bank mentioned earlier. Consequently, using a 300 MHz clock as the coarse-counting clock meets the design requirements, and the delay chain is theoretically expected to exhibit better linearity. The test results are presented in Fig. 3a–d.

If automatic layouts and routing are performed using software, it is common for the delay chain to span different banks, leading to uneven delays. The test results in Fig. 3a–d

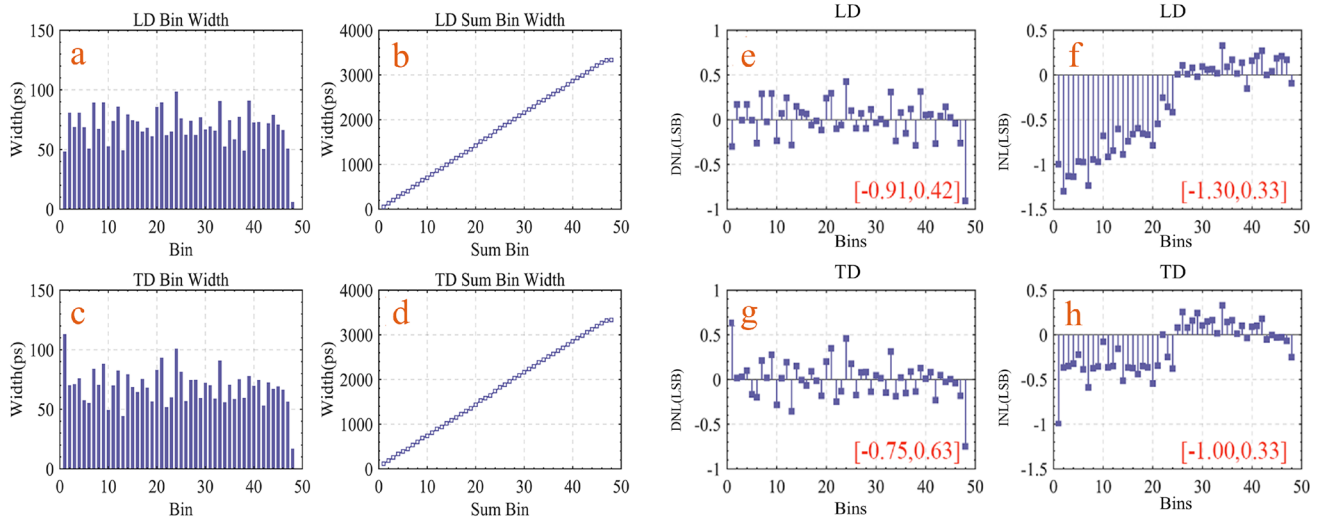


Fig. 3 (Color online) **a** Leading edge code density of delay elements, **b** cumulative leading edge code density, **c** trailing edge code density, **d** cumulative trailing edge code density, **e** leading edge differential

nonlinearity of the delay chain, **f** leading edge integral nonlinearity, **g** trailing edge differential nonlinearity, **h** trailing edge integral nonlinearity

illustrate the code density results after manual layout and routing, where the distribution of each delay element is more uniform. The delay differences between each delay element are mainly attributed to the time differences in the sampling clock reaching various registers, as well as the inherent nonuniformity of the semiconductor manufacturing process.

The nonlinear performance of a TDC is primarily assessed using two metrics: differential nonlinearity (DNL) and integral nonlinearity (INL). These parameters reflect the uniformity of the TDC's bin width. Figure 3e–h illustrates the DNL and INL of the delay units in a manually routed delay chain within a digital circuit. The formulas for calculating DNL and INL are as follows:

$$DNL_i = \frac{LSB_i - LSB}{LSB}, \quad (7)$$

$$INL_i = \frac{\sum_{i=0}^n LSB - iLSB}{LSB}. \quad (8)$$

In this context, LSB_i is the delay time corresponding to the i -th delay element. When analyzing this section, this delay time is quantized into the number of measured pulses for the corresponding delay element, and the time resolution is the average number of pulses.

The DNL for the leading edge is optimized to the range $[-0.91, 0.42]$, and the INL is $[-1.30, 0.33]$. For the trailing edge, the DNL is $[-0.75, 0.63]$, and the INL is further optimized to the range $[-1.0, 0.33]$. In an ideal scenario, the delay time of each delay unit that constitutes a TDC should be identical, implying that the widths of all bins should be exactly the same. The smaller the bin width, the higher the

TDC resolution. The average resolution of a TDC can be represented by Eq. 9, which considers the uniformity of all delay units and the effect of the bin width on the resolution.

$$LSB = \frac{T_c}{N} \quad (9)$$

In the TDC delay chain, N represents the number of effective delay units within time T_c . For a given TDC delay chain with 48 effective delay units and a sampling clock of 300 MHz for each delay unit, that is, $T_c = 3333.3$ ps. The average resolution of the delay chain was 69.4 ps.

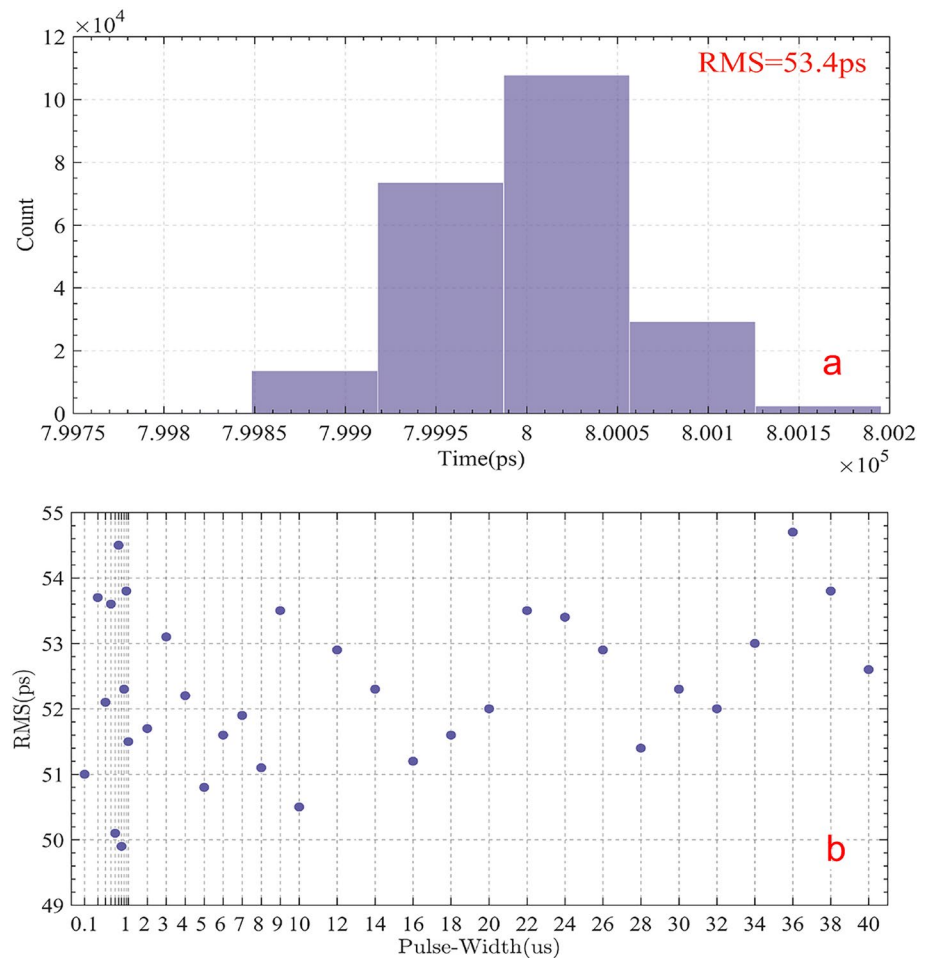
2.3.2 RMS accuracy analysis

The root-mean-square (RMS) accuracy of the TDC measurement data is assessed by conducting multiple measurements within a fixed time period and analyzing the dispersion of the resulting data. RMS accuracy is an important metric for evaluating the precision of TDC measurement results in characterizing pulse-width signals. RMS accuracy reveals the degree of deviation of the measured values from ideal values. The calculation of RMS follows Eq. 10:

$$RMS = \frac{1}{\sqrt{N-1}} \sqrt{\sum_{i=1}^N \left(X_i - \frac{\sum_{i=1}^N X_i}{N} \right)^2}, \quad (10)$$

where N denotes the number of measurements and X_i represents the data from the i -th measurement. The more data tested for a pulse of the same time width, the more accurate the calculated RMS value. Figure 4a shows the RMS test

Fig. 4 (Color online) **a** Signal width = 800 ns, RMS test value, **b** $100 \text{ ns} \leq \text{signal width} \leq 40 \mu\text{s}$, RMS test values at various test points



results for a square-wave signal with a pulse width of 800 ns and an *RMS* value of 53.4 ps.

To comprehensively evaluate the performance of the TDC designed in this study over a wide range of times, we adopted a strategy of selecting test points in stages: within the 0 to 1 μs range, a test point was set every 100 ns; within the 1 to 10 μs range, a test point was set every 1 μs ; within the 10 to 40 μs range, a test point was set every 2 μs . This distribution of test points ensured an accurate assessment of the TDC performance across different time scales. At each test point, more than 100000 sets of sample data were collected to ensure statistical reliability. Through the analysis of these data, we obtained the distribution of the time measurement accuracy results, as shown in Fig. 4b.

Based on these measurement data, the average time measurement accuracy of the TDC designed in this study was 52.3 ps. This result not only demonstrates the high performance of the TDC in the time range from nanoseconds to microseconds but also verifies its application potential in the field of high-precision time measurement.

Using the precision evaluation method mentioned above, we added three more measurement channels

identical to those in the system and tested the other three channels in the same manner. Under the condition that all the test conditions remain unchanged, the time precision results for each TDC channel are summarized in Table 1. The measurement results indicated that the average precision of the four TDC measurement channels was approximately 50 ps in the range of 100 ns to 40 μs .

Table 1 Main system parameters

Part	Parameter	Specification
FPGA-TDC	FF Utilization rate	0.48%
	LUT Utilization rate	0.60%
	Resolution	69.4 ps
	RMS	53.4 ps
	Measuring dead time	$\leq 30 \text{ ns}$
Analog circuit	Power dissipation	$\leq 100 \text{ mW/channel}$
	PCB area	$24 \text{ mm} \times 30 \text{ mm/channel}$
	Measuring range	0 – 5.3 V

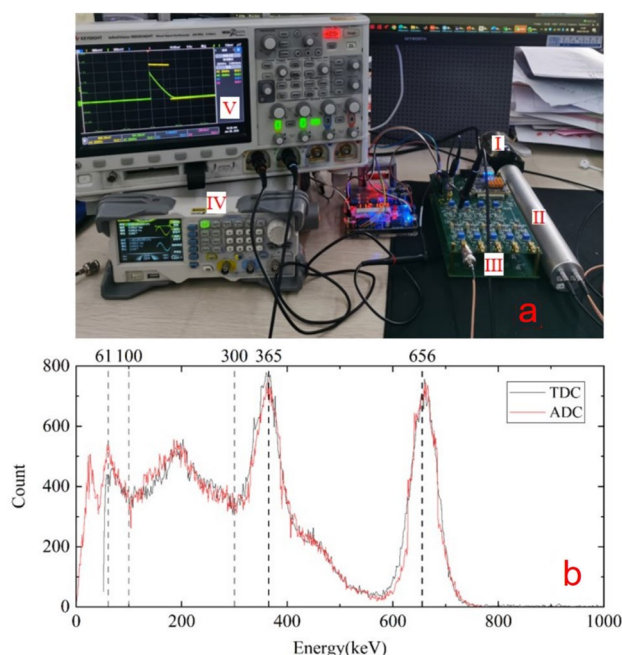


Fig. 5 (Color online) **a** The system field joint test experimental diagram, **b** comparison of spectral measurement between ADC scheme and TDC scheme

2.4 Gamma-ray spectrometry measurement and analysis

An experimental diagram of the system field joint test is shown in Fig. 5a. It includes a radioactive source (I), a NaI(Tl) detector (II), a main measurement board (III), a signal generator (IV), and an oscilloscope (V). In this study, we selected a CH132-07 type NaI(Tl) scintillation detector produced by Beijing Hamamatsu Photonics as the signal input source. This detector was equipped with a crystal measuring $\Phi 25 \text{ mm} \times 25 \text{ mm}$, and its energy resolution for the characteristic peak of ^{137}Cs was better than 9% (nominal energy resolution). During the experiment, we used the “TDC scheme” and the “ADC scheme” for comparison. We utilized ^{131}I and ^{137}Cs radioactive sources for energy calibration. The energy spectra obtained using the two schemes are shown in Fig. 5b.

In the TDC scheme, the comparator threshold was set to 0.64 V. After energy calibration, the energy spectrum results of the TDC and ADC schemes coincided at the high-, medium-, and low-energy characteristic peaks. The two characteristic peaks corresponding to the energies of 364 keV and 662 keV from ^{131}I and ^{137}Cs observed in both schemes were clearly distinguished, and the peak positions were consistent. The root-mean-square error in the range of 70 keV to 1000 keV was 12.3 keV. Under the same test conditions, the energy resolution of the ADC scheme for the

characteristic peak of ^{137}Cs was 8.3%, whereas that of the TDC scheme designed in this study was 8.5%.

3 Summary

This study proposes a high-precision TDC for a digital MCA. Using this method, the digital MCA quantifies and collects statistics on the discharge time of nuclear pulse signals, ultimately obtaining the gamma-ray energy spectrum. Experimental results show that on a Xilinx A7 series FPGA, the TDC resolution can reach 69.4 ps, the dead time is two system clocks, the differential nonlinearity range of the leading edge measurement of the delay chain is $[-0.91, 0.42]$, and the INL range is $[-1.30, 0.33]$. Moreover, the DNL range of the trailing edge measurement is $[-0.75, 0.63]$, and the INL range is $[-1.0, 0.33]$. Analysis of the key parameters revealed that for signals with voltages higher than 0.4 V, the nonlinearity of the conversion results of the autonomous linear discharge circuit was less than 0.05%. Tests were conducted using a NaI(Tl) detector with a size of $\Phi 25 \text{ mm} \times 25 \text{ mm}$, along with a linear discharge circuit and high-precision TDC for the measurement of the 662 keV full-energy peak of the ^{137}Cs source, with an energy resolution of 8.5%. Under the same conditions, the energy resolution measured using the ADC scheme was 8.3%. An analysis of the experimental results demonstrates the feasibility of the proposed method for digital MCAs. By innovating the front-end analog circuit, a compact and structurally simple autonomous linear discharge analog scheme is proposed, in which the autonomous linear discharge structure, combined with a high-precision FPGA-TDC, provides a new solution for the acquisition and measurement of multichannel systems.

Author contributions All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by Ze-Xi Wang, Yi-Ni Wu, Ke-Feng Zou, Hao-Xuan Li, Jing Peng, and Lei Wang. The first draft of the manuscript was written by Ze-Xi Wang, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data availability The data that support the findings of this study are openly available in Science Data Bank at 31253.11.sciencedb.j00186.01009 and <https://doi.org/10.57760/sciencedb.j00186.01009>.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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