



Development of an innovative real-time dosimetry monitoring system for heavy-ion radiotherapy

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Abstract

Cancer is the second leading cause of mortality globally. Radiation therapy is a critical technological approach in oncology treatment and includes conventional dose rate radiation therapy, high-dose radiotherapy, and ultrahigh-dose rate radiation therapy. Following the significant increase in radiotherapy dose rates, real-time dosimetry monitoring faces the dual challenge of enhancing both response time and measurement precision. In this study, we successfully developed a real-time dosimetry monitoring system for radiotherapy designed to accommodate a broad range of dose rates. The system consists of a dual-gated, integrator architecture, front-end and high-speed data acquisition circuit, providing accurate detection of bipolar current pulse signals with peak values from $-190\ \mu\text{A}$ to $+200\ \mu\text{A}$. The minimum current measurement range is $-1\ \text{pA}$ to $+1\ \text{pA}$. Two major technological advancements were accomplished: First, the elimination of the signal processing dead time resulted in a reduction of the single-event readout time to $5\ \mu\text{s}$; second, the nonlinear error (ranging from $-190\ \mu\text{A}$ up to the maximum current value) is within 0.67% , with a linear correlation coefficient (R^2) of 0.99992 . Experiments were conducted using an ionization chamber detector at the Heavy Ion Research Facility in Lanzhou. This system, combined with a dose detector, achieves real-time dose measurements within the dose rate range of $65\text{--}120\ \text{Gy/min}$. Excellent real-time monitoring performance is demonstrated in the high-dose range of radiation therapy, demonstrating the system's potential for additional use in dose monitoring for electron- and proton-beam radiotherapy applications.

Keywords Real-time dosimetry monitoring · Heavy-ion radiotherapy · Data acquisition circuit · Analog front-end circuit

1 Introduction

Malignant tumors pose a major threat to human health, and radiation therapy is one of the most important cancer treatment methods. Unlike traditional photon radiation schemes, heavy-ion beams exhibit a Bragg peak, causing concentrated

dose deposition whose depth can be adjusted finely by altering the beam energy [1]. This enhances the protection of healthy tissues [2]. Therefore, it is currently considered the optimal form of radiation therapy in clinical practice [3, 4]. Ion therapy includes conventional dose rate radiotherapy, high-dose radiotherapy, and ultrahigh-dose rate radiotherapy (FLASH-RT) [5–9]. Research indicates that high-dose radiotherapy can suppress tumor-reactive immunity [10], whereas FLASH-RT notably reduces the toxicity of radiation to normal cells surrounding tumor cells [11–17]. The effectiveness and quality of ion beam therapy are strongly correlated with the dose delivered to the patients. Consequently, beam monitoring is essential for ensuring the precision and efficacy of ion therapy [18]. Typically, ionization chambers are used as dose detectors at the end of heavy-ion radiotherapy to measure the dose [19–26], and the current signal produced by the ionization chamber is directly proportional to the dose delivered during beam radiation therapy. Dose ionization chamber detectors can neglect the dependence on

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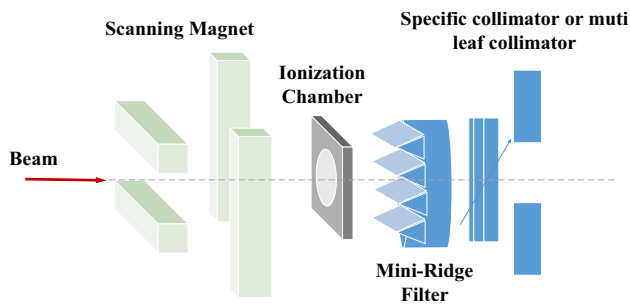


Fig. 1 (Color online) Layout of the beam-monitoring system detectors for the terminal

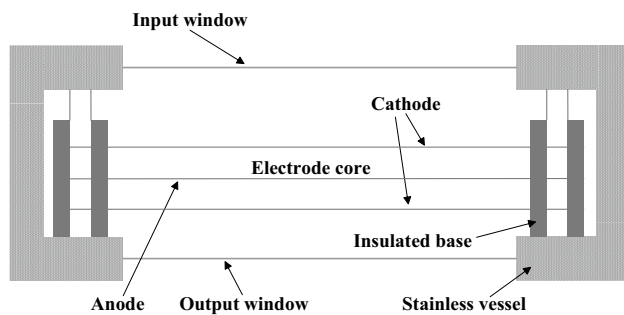


Fig. 2 (Color online) Schematic of the ionization chamber structure

particle energy and linear energy transfer while exhibiting high reproducibility and accuracy. As a result, ionization chambers are regarded as the gold standard for monitoring radiation therapy doses [27, 28].

The shallow-layer treatment and biological irradiation terminal at the Lanzhou Heavy Ion Research Facility (HIRFL) conducts mutagenic breeding and heavy-ion cancer treatment research using different ionic species, energies, and dose rates. The layout of the beam-monitoring system detectors for this terminal is illustrated in Fig. 1.

The dose measurement for the terminal used a flat-type ionization chamber, as shown in Fig. 2.

It consists of four parts: a metal-sealed housing, an entrance window, exit window, electrode core, and an insulating base. The electrode core uses a three-layer electrode comprising a central anode and cathodes at both ends, all made from a double-sided aluminum-coated polyimide film with a thickness of 13 μm . The aluminum coating thickness is 100 nm. Both the entrance and exit windows are made from double-sided aluminum-coated polyimide film with a thickness of 25 μm . The overall equivalent water thickness is less than 0.1 mm.

To eliminate the effects of air humidity and atmospheric pressure on the charge collection efficiency, high-purity nitrogen gas at a fixed pressure was used as the working gas. The ionization chamber operates at a negative high voltage to collect electrons, and the generated current (charge)

signal is directly output and read by a new, real-time dose-monitoring system. The beam energy for the shallow-layer, heavy-ion cancer treatment terminal was 80–100 MeV/u ($^{12}\text{C}^{6+}$). At atmospheric pressure, the charge signal output of the flat-type ionization chamber reached a maximum of 10 μA . The terminal is currently conducting research on high- and ultrahigh-dose rate heavy-ion cancer treatments. As the dose rate increases, the demand for real-time dose monitoring in terms of difficulty, importance, and accuracy progressively increases. This places the following requirements on electronics: The detectable current signal should reach at least 10 μA , redundancy is preferred, the front-end circuit should have minimal dead time, and the processing time for a single event should be less than 10 μs . The integral nonlinearity must be less than 1% over the entire dynamic range.

Columns 2 and 3 of Table 1 present the ranges of the current output from the ionization chamber for various radiation therapy devices under the corresponding dose rate conditions. The output signal from the dose ionization chamber detector varies owing to differences in the beam intensity and the chamber's actual gain. Therefore, dose-monitoring readout electronics must be capable of measuring input signals with intensities ranging from pA to μA [29].

Columns 4 and 5 of Table 1 [30–34] present the readout electronics system for the dose ionization chambers and their linear relationships for different radiation therapy devices. As shown in the table, the measurements of the current signal output by dose detection ionization chambers (conducted around the world) typically use very large-scale integration (VLSI) [35], application-specific integrated circuits (ASICs) [36], or discrete components [37–39]. VLSI and ASIC devices are characterized by high integration, low-power consumption, and exceptional stability. However, their development is complex, with long timelines, limited versatility, and slow technological advancements. In contrast, measurement circuits based on discrete components provide greater flexibility, lower costs, and faster technological updates; however, they tend to occupy more circuit board space, have lower integration capability, and are more susceptible to noise interference. Two commonly used readout schemes that utilize discrete components include a) an integrator circuit combined with an analog-to-digital converter (ADC) for sampling and output [22]. This approach directly integrates current to obtain charge, simplifying it and rendering it insensitive to alternating current noise. The measurement range could be adjusted by selecting an appropriate capacitance based on the beam's intensity. b) The second scheme converts the current into voltage, which is subsequently converted into a frequency output [40], with the charge measured via a count. This scheme is conducive to digital processing and provides high accuracy. However,

Table 1 Comparison of dose rate, output current, reading system, and nonlinearity for different experimental equipment

Experimental equipment	Dose rate	Output current	Electronics readout system	Nonlinearity
Heavy Ion Medical Accelerator in Chiba at the National Institute of Radiological Sciences [30]	1 Gy/min	Maximum (Max) 1000 nA	Current to voltage (<i>I/V</i>) amplifier and voltage to frequency converter + analog-to-digital converter	<1%
Elekta SL 75-5 [31]	3.5 Gy/min	Max 4 μ A	Current integration and counter-type very large-scale integration	<1%
Multipad ionization chamber and multilayer ionization chamber at the Midwest Proton Radiotherapy Institute [32]	1.5–5 Gy/min	0.125–8 nA	Sixteen channel-gated current integrator module	$R^2 = 0.999$
FLASH proton RT, University of Pennsylvania [33]	60–100 Gy/s	5–300 nA	Faraday cup and Marcus chamber	Not provided
Heavy Ion Medical Accelerator in Kansai at Japan's Atomic Energy Agency [34]	102.54–115.38 Gy/s (average dose rate)	–0.5–+50 μ A	Current to frequency amplifier	<1%

its linear range is limited; when the current approaches the measurement threshold, the linearity may deviate, leading to measurement errors. Therefore, this approach is not suitable for general-purpose designs.

To facilitate dose measurements that are compatible with high and conventional dose rate radiotherapy—specifically covering current outputs ranging from hundreds of pA to hundreds of μ A as typically provided by ionization chambers—we developed an innovative real-time dose-monitoring readout system. This system utilizes a dual-gated integrator architecture for an analog front-end (AFE) circuit to integrate directly the current. Coupled with a data acquisition (DAQ) circuit for sampling and readout, the system is capable of covering a broad bipolar dynamic current range of $-190 \mu\text{A}$ – $+210 \mu\text{A}$, thus meeting the readout requirements of the majority of ionization chamber detectors used in particle therapy dose measurements. In conventional designs, the current signals are acquired after passing through an AFE circuit. During the acquisition period, the AFE circuit must maintain the current voltage, which renders it incapable of responding to real-time input currents, thereby causing dead times. This dead time limits the ability of the detector to record all events, potentially compromising the completeness of data acquisition and subsequently affecting the precision and efficacy of the treatment process. Furthermore, the response capability to high-frequency events, which is directly related to the processing time of individual events, can affect the accuracy of real-time monitoring. To address these limitations, the proposed real-time dose-monitoring readout system utilizes a dual-gated integrator architecture in an analog front-end processing circuit. By enabling the two integrators to operate alternately, the system effectively eliminates dead time and reduces the individual event processing time to 5 μs .

2 System structure

A schematic of the development of the innovative real-time dosimetry monitoring system is shown in Fig. 3. The system comprises two primary components: an innovative AFE circuit based on a dual-gated integrator architecture and a DAQ circuit. The AFE utilizes a dual-gated integrator to segment and process weak current signals from the detector, converting them into a voltage. This voltage signal was subsequently sampled and encoded using a pipeline-style ADC. The field-programmable gate array (FPGA) on the DAQ circuit board is responsible for synchronizing and compressing the encoded data. Additionally, the FPGA logic control circuit manages the conversion of the AFE circuit, ADC sampling, and other associated operations. Finally, the FPGA communicates with the host computer via a universal serial bus (USB), enabling command transmission and the uploading of dose data. The host computer processed and displayed the transmitted data in real time.

2.1 AFE circuit

As shown in Fig. 4, the AFE circuit consists of dual-gated integrators, a multiplexer, an optocoupler isolator, an attenuation circuit, and a complex programmable logic device (CPLD). The current signal output from the ionization chamber alternately enters the two gated integrators, is converted into a voltage signal, and is then selected; the output is then controlled by the CPLD via the multiplexer. The circuit is activated upon receiving the external trigger signal TrigIn. Integrator A begins integrating during the high-level period, thereby generating voltage signals. Simultaneously, the CPLD controls the multiplexer to output the voltage from Integrator B, which is held for a certain duration to allow digitization by the DAQ circuit. Subsequently, the voltage

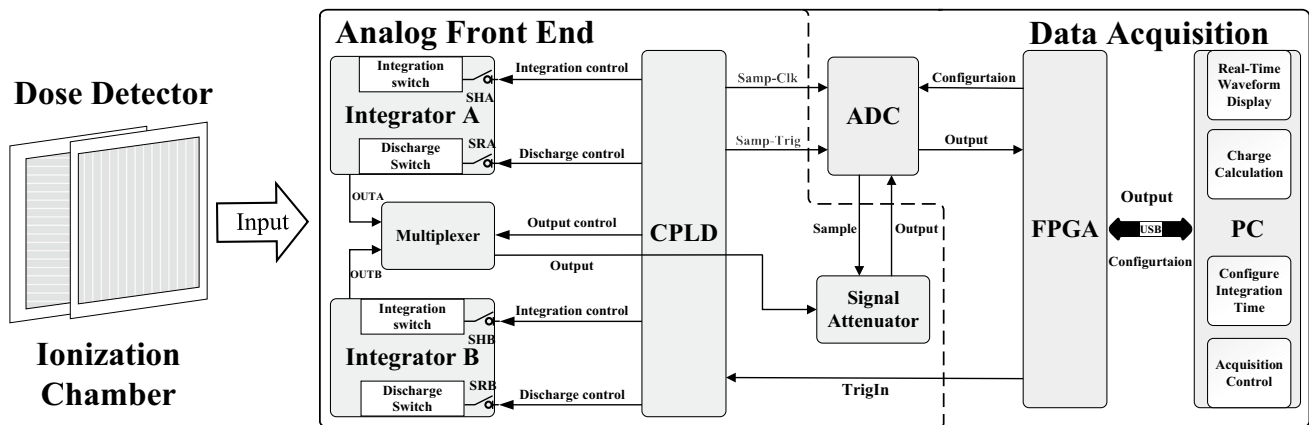


Fig. 3 (Color online) Schematic of the readout system

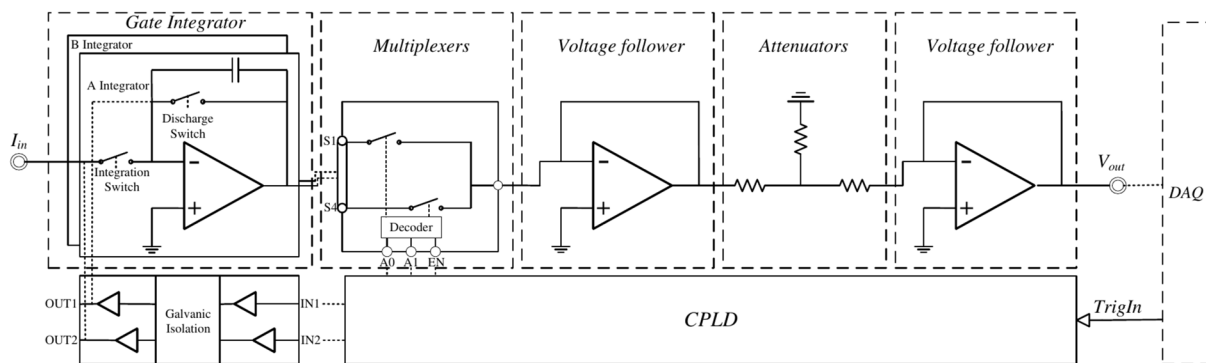


Fig. 4 Analog front-end (AFE) circuit

was discharged to complete the initialization. When TrigIn transitions, Integrator B starts integrating and generating a voltage, whereas the CPLD switches the multiplexer to output the voltage from integrator A. This voltage was held for digitization and then discharged. An image of the AFE circuit is shown in Fig. 5. Because the AFE circuit was located near the beam area, a shielding enclosure was employed to enhance its radiation tolerance, effectively reducing external radiation interference and improving system stability.

2.1.1 Dual-gated integrator architecture circuit

A dual-gated integrator architecture circuit was constructed using two integrators in conjunction with four high-speed switching gates, as shown in Fig. 6.

The dual-gate integrator architecture circuit begins operation after the power-on reset. The alternating hardware operation states during the operating period are shown in Fig. 7.

(1) **State 1:** The input current is integrated by Integrator A, with its integration switch closed and discharge switch

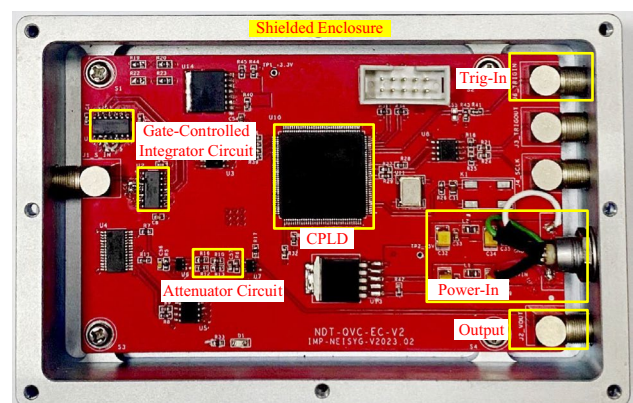


Fig. 5 (Color online) AFE circuit photograph

open. In Integrator B, both switches are open. The DAQ circuit samples the voltage from Integrator B.

(2) **State 2:** After the voltage sampling from Integrator B is completed, the AFE circuit closes the discharge switch

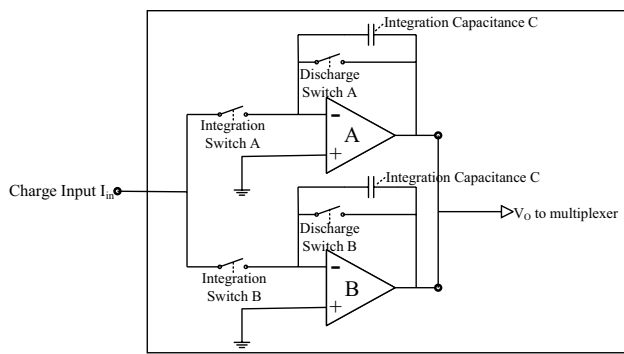


Fig. 6 Dual-gated integrator architecture circuit

of Integrator B to allow voltage discharge. Meanwhile, Integrator A continues integrating.

- (3) **State 3:** Upon completion of the discharge, Integrator B begins integration as its integration switch closes. Simultaneously, both switches of Integrator A are opened to halt integration. The DAQ circuit then samples the voltage from Integrator A.
- (4) **State 4:** After the DAQ circuit finishes sampling the voltage from Integrator A, the discharge switch of Integrator A is closed, and the AFE circuit discharges

the voltage from Integrator A. Once the voltage from Integrator A is fully discharged, the cycle returns to State 1, where the integration and discharge switches of Integrator B are both opened, halting integration in Integrator B; Integrator A then starts the integration process again. The DAQ circuit samples the voltage from Integrator B. This process repeats continuously.

The integration switch was closed only when the discharge switch was open. During the short period in which the integration switch was open (approximately 100 ns), any signal current produced by the ionization chamber charged the ionization chamber's effective input capacitor. This charge was then transferred to the integrating capacitor when the integration switch was closed. Consequently, no charge produced by the ionization chamber is lost, and the input signal is continuously integrated. Even fast input pulses were accurately integrated.

To eliminate errors caused by baseline drift, the integration output voltage V_O was calculated by subtracting the baseline voltage V_{baseline} from the measured voltage V , as defined in Eq. (1)

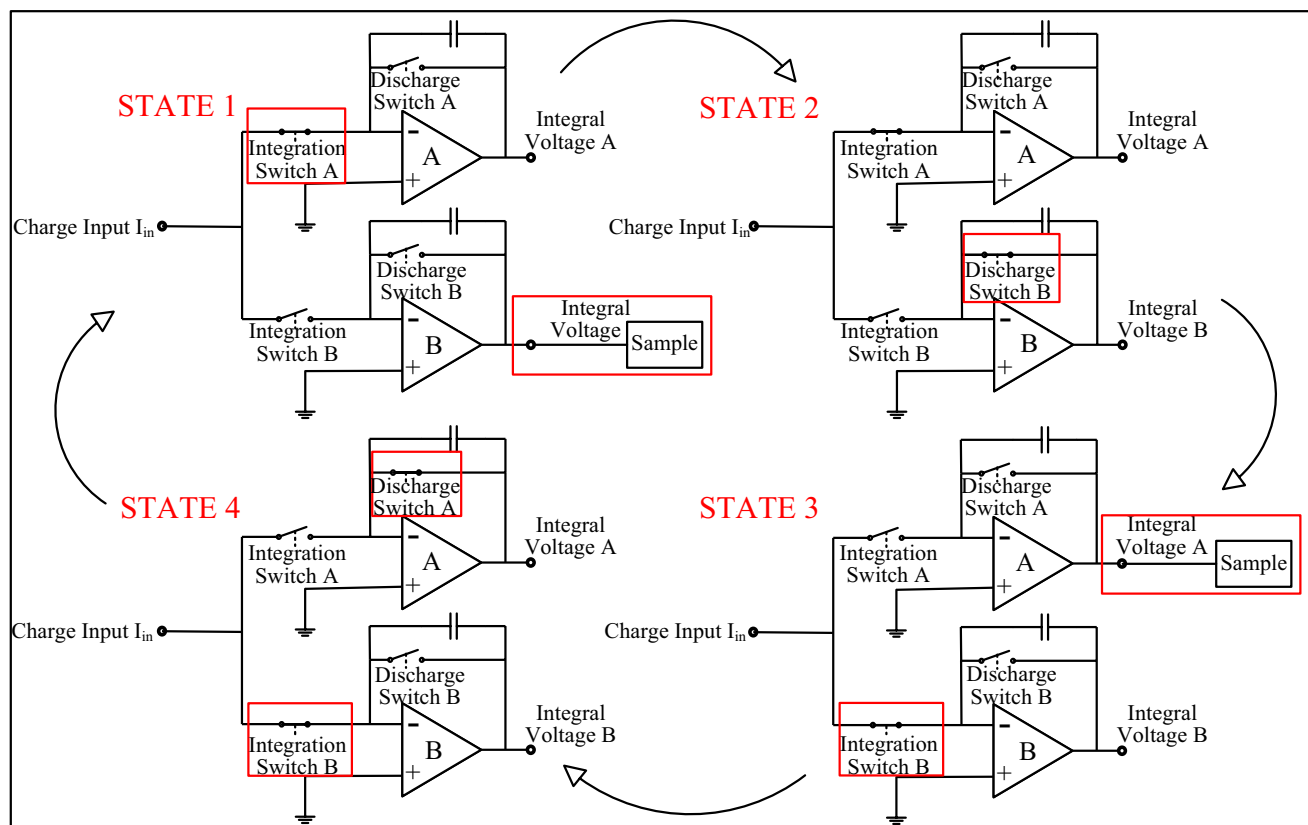


Fig. 7 (Color online) Dual-gated integrator architecture circuit alternating hardware operation states

$$V_O = V - V_{\text{baseline}} \quad (1)$$

The functional relationship between the output charge Q of a single integration and output voltage is given by Eq. (2)

$$Q = C_{\text{INT}} V_O = I_{\text{IN}} T_{\text{INT}}, \quad (2)$$

where I_{IN} is the input current, and C_{INT} is the integration capacitor. To ensure the accuracy of the calculated results, the value of C_{INT} should be accurately calibrated in the laboratory to minimize deviations from the theoretical values and ensure measurement accuracy.

Assuming that the input current is integrated over a certain period, the total accumulated charge is given by Eq. (3).

$$Q_a = \sum_{i=1}^N Q_i = Q_1 + Q_2 + Q_3 + \dots + Q_N, \quad (3)$$

where Q_i denotes the output charge of the i th integration cycle. Supposing that the input current is 100 μA , each integration period is 5 μs , the integration capacitance is calibrated to 100 pF, and the output charge per cycle is calculated using Eq. (4):

$$Q = I_{\text{IN}} T_{\text{INT}} = 500 \text{ pC}. \quad (4)$$

If the input current is continuously integrated over 1 ms, corresponding to 200 events, the total accumulated charge can be calculated using Eq. (5)

$$Q_a = \sum_{i=1}^{200} Q_i = Q_1 + Q_2 + Q_3 + \dots + Q_{200} = 100 \text{ nC}. \quad (5)$$

The output current pulse signal range of the dose ionization chamber detector exhibited a large span. The gated integrator adjusts the gain to accommodate different input ranges. The circuit's conversion gain is determined by both the integration time and integration capacitance. Specifically, the output voltage was proportional to the integration time and inversely proportional to the integration capacitance. A higher gain can be obtained by increasing the integration time or reducing the integration capacitance. When the input signal was large, the integration time of the gated integrator decreased, whereas when the input signal was small, the integration time increased. The gated integrator is highly flexible, capable of converting and amplifying current to voltage and effectively mitigating noise and interference signals that fluctuate around the baseline by integrating them, resulting in major noise and interference reductions. Furthermore, the gated integrator used in this circuit features on-chip integrated capacitors, which help minimize the impact of the leakage voltage caused by dielectric losses in the integration capacitor.

The traditional single-integrator architecture is typically associated with a dead time between the integration

and discharge phases (a blank period during charge signal processing), which can result in increased measurement errors and reduced timeliness. In contrast, the dual-gate integrator architecture alternates between two integrators to complete integration and discharge, ensure real-time and continuous processing of current signals, and provide dead-time-free readout. This is particularly critical for rapid response and high-accuracy dose measurements.

2.1.2 Attenuation circuit

As shown in Fig. 4, the attenuation circuit follows the multiplexer circuit at the backend. The voltage amplitude range of the output from the front-end multiplexer circuit is $-10 \text{ V} - +10 \text{ V}$. To reduce the power consumption of the circuit and match the signal processing range of the data acquisition circuit in the subsequent stage, a voltage attenuation circuit is designed to attenuate the signal within the $-10 \text{ V} - +10 \text{ V}$ range to values in the range of $-1 \text{ V} - +1 \text{ V}$. The attenuation was performed using a T-attenuation circuit, as shown in Fig. 8.

The circuit resistance is calculated using Eq. (6), where R_c is the circuit impedance-matching resistance of 50 Ω , and N is the attenuation factor.

$$R_1 = R_c \frac{N-1}{N+1} \quad R_2 = R_c \frac{2N}{N^2-1} \quad (6)$$

From the equation listed above, the resistance in this circuit is calculated as $R_1 = 10 \text{ k}\Omega$ and $R_2 = 560 \Omega$, and the voltage signal amplitude after passing through the attenuation circuit is $\pm 1 \text{ V}$, which is then input directly into the data acquisition circuit through a subsequent stage follower circuit.

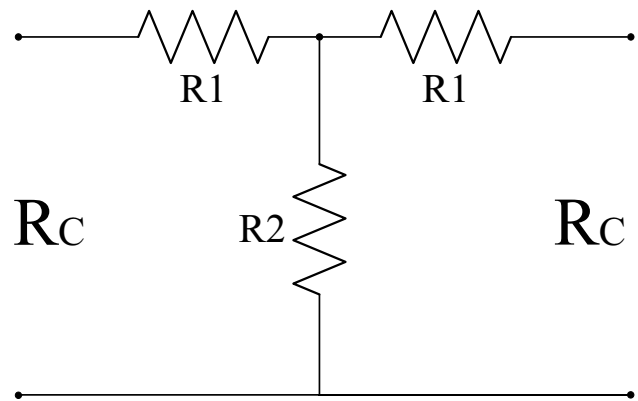


Fig. 8 T-attenuation circuit

2.2 DAQ circuit board

As shown in Fig. 9, the DAQ circuit primarily consists of a front-end preprocessing unit (PPU) and a data processing unit (DPU). The PPU amplifies and filters the raw voltage signal output by the AFE, shaping it before it is sampled by the 14-bit, onboard ADC and converted into digital signals. These digital signals were then forwarded to the DPU for further signal processing and computation. The DPU handles algorithmic data-flow processing, transmission, command reception, and parsing, as well as clock control. A photograph of the DAQ circuit board is shown in Fig. 10.

2.2.1 PPU unit

The PPU consists of four main components: a matching and protection circuit, gain amplification circuit, an anti-aliasing filter, and an ADC sampling circuit. To minimize the signal reflection and enhance the measurement accuracy, terminal matching was used as the input for proper impedance matching. A filter-shaping circuit was used to eliminate high-frequency noise. To simplify the circuit structure while achieving optimal filtering performance and to serve as the driver circuit for the ADC, the design adopted a second-order, low-pass anti-aliasing filter characterized by low noise, low distortion, and broad bandwidth as the driving circuit.

2.2.2 DPU unit

The hardware structure of the DPU unit consists mainly of an FPGA and its peripheral circuits, providing a sampling clock for the ADC and supplying clock and synchronization signals for the internal data processing modules of the FPGA. The DPU also included multiple interfaces to control the AFE circuit. The data transmission interface includes an optical fiber transmission and a USB interface. The host computer sends instructions to the FPGA via USB. After receiving the instructions, the FPGA controls operations—such as ADC sampling and first-in-first-out (FIFO) caching—and then transmits the acquired signals to the host computer through a USB transmission circuit.

3 System firmware design

The system firmware design has two main parts: One controls the high-speed switches and signal reading of the gated integrator on the AFE board using a CPLD, whereas the other manages ADC sampling, data processing, packaging, uploading, and communication with the host computer.

3.1 AFE circuit firmware design

Figure 11 shows the gated integrator where different capacitors can be selected based on the input.

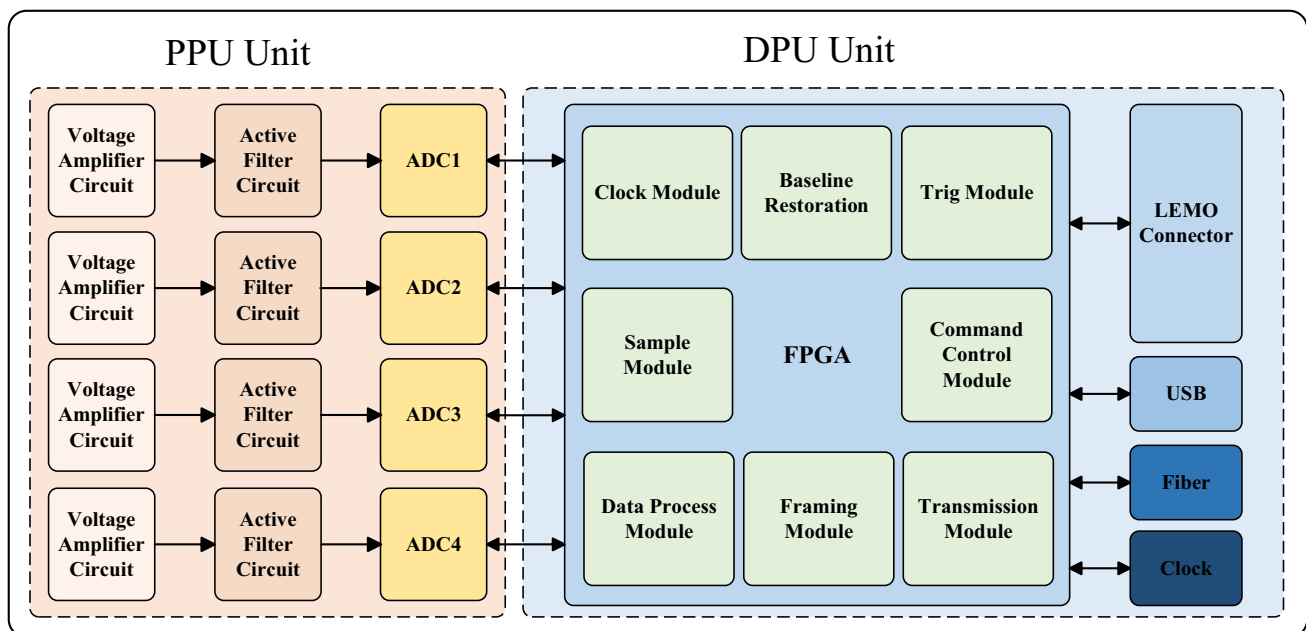


Fig. 9 (Color online) Schematic of the DAQ circuit

Fig. 10 (Color online) Photograph of the DAQ circuit board

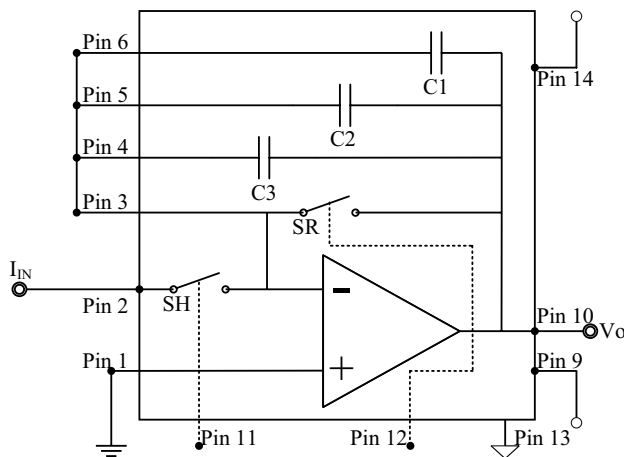
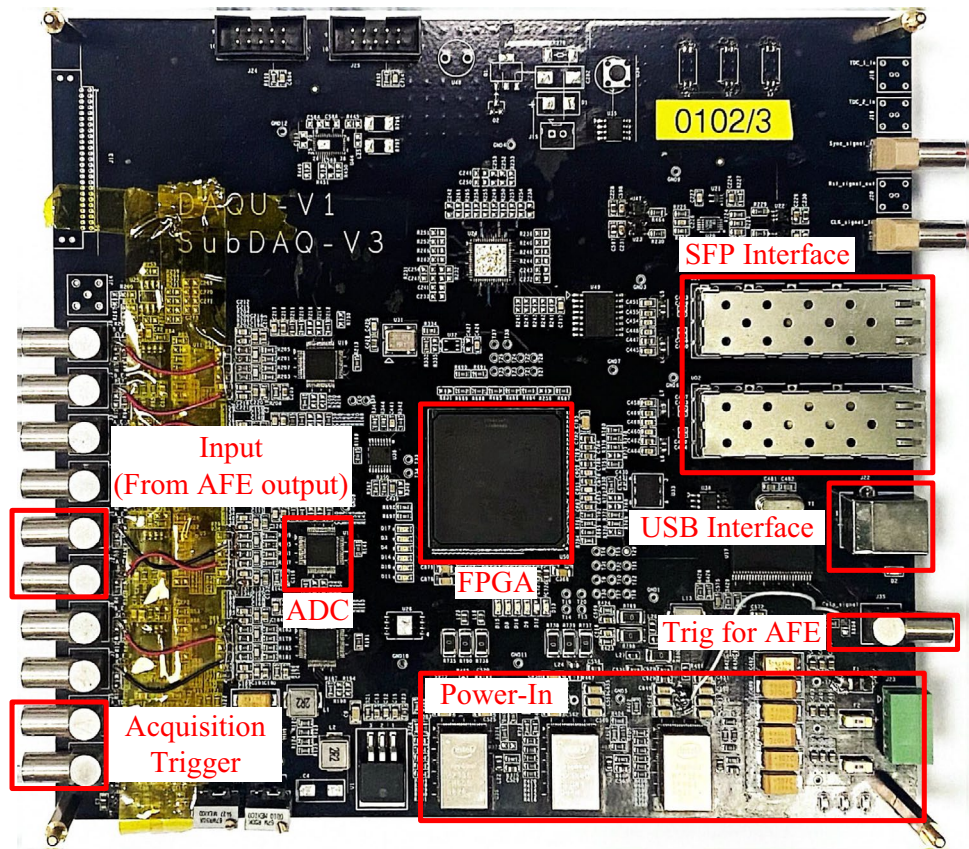


Fig. 11 Schematic of the gated integrator

Figure 12 illustrates the complete integration cycle, which consists of four stages, namely discharge, wait, integration, and hold.

- (1) **Discharge:** SH is set to high and SR to low, grounding the capacitors in the gated integrator and initiating the discharge.

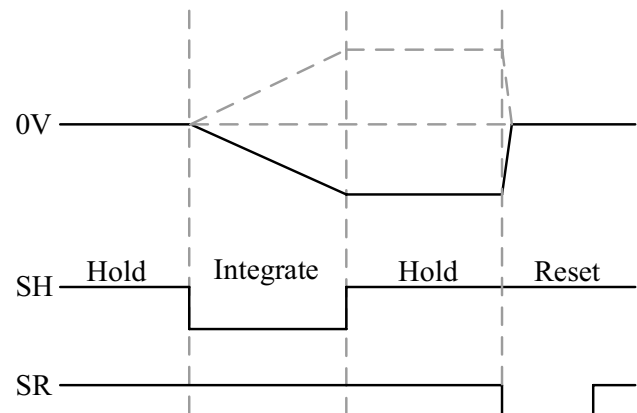


Fig. 12 Complete integration cycle of the gated integrator

- (2) **Wait:** Set both SH and SR to high, prepare for integration, disconnecting SR to prevent charge flow to the ground. The wait time should be at least 100 ns for stability.
- (3) **Integration:** SH is set to low and SR to high, activating SH and charging the capacitor.
- (4) **Hold:** Set both SH and SR to high, deactivating SH and halting the integrator's operation.

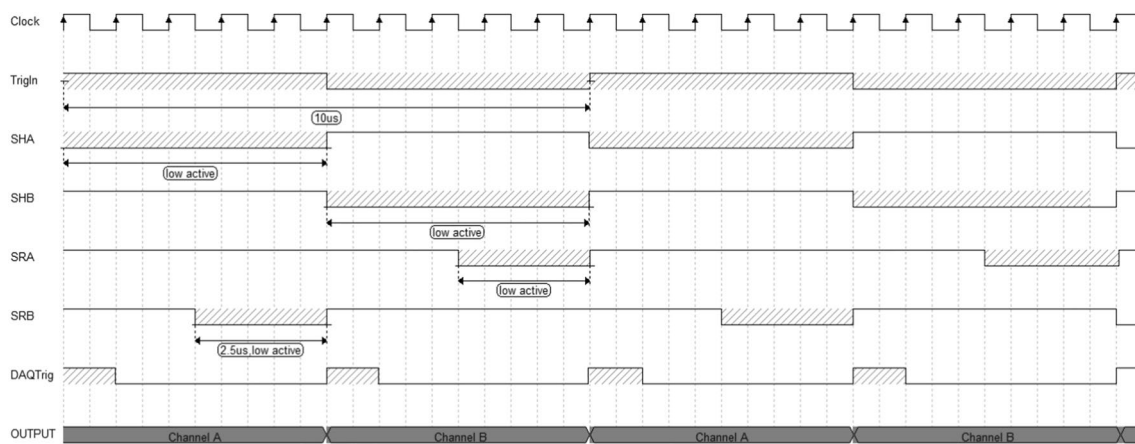
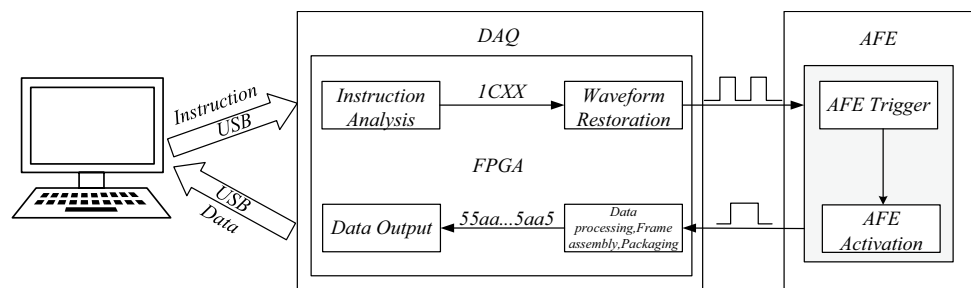


Fig. 13 AFE circuit's timing diagram

Fig. 14 System's diagram for AFE triggering, USB commands, and data transmission



The AFE firmware design involves the CPLD's logic control of the dual-gated integrator, multiplexer, and other components. A timing diagram is shown in Fig. 13, where “Clock” is the system clock provided by an external crystal oscillator, and “Trigin” is the external trigger signal corresponding to the operating cycle. SHA and SHB are the integration switches for Integrators A and B, respectively, whereas SRA and SRB are the discharge switches for Integrators A and B, all of which are actively low. “Daqtrig” is the acquisition trigger signal sent from the AFE circuit to the DAQ circuit, which instructs the ADC when to sample the data. “OUTPUT” refers to the output signals, where channels A and B, respectively, correspond to the outputs of integrators A and B.

3.2 DAQ circuit firmware design

The DAQ circuit firmware design primarily includes logic control for FPGA data framing and packaging, AFE triggering, USB commands, and data transmission.

3.2.1 AFE triggering, USB commands, and data transmission

The AFE triggers signal Trigin defines the circuit operation. The AFE operates on the period of Trigin, with the

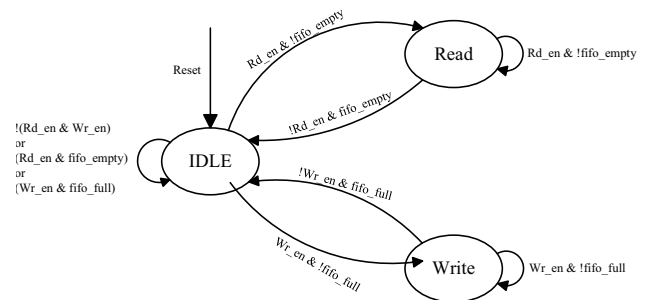


Fig. 15 State transition diagram of the field-programmable gate array and universal serial bus communication

integration duration and gain directly related to its period. The system diagram for AFE triggering, USB commands, and data transmission is shown in Fig. 14.

The host computer sends commands and integration duration via a USB to the FPGA in the DAQ circuit. The FPGA parses the commands, restores the waveform, and generates the correct Trigin signal that controls the AFE's operation time and cycle. Once the AFE is active, the output signal is sampled by the DAQ circuit, and the FPGA processes and packages the data, which are then uploaded to the host computer via a USB. Figure 15 illustrates the complete process

of a read–write operation state transition between the FPGA and USB. The FIFO_empty and FIFO_full signals shown in the figure represent the FIFO status signals of the USB chip.

- (1) **Idle state:** After reset, the system waits for the trigger condition in the IDLE state.
- (2) **Reading state:** If the read enable is active and the FIFO is not empty (Rd_en & !fifo_empty), the system enters the reading state, where the FPGA performs the read operation and increments the read counter. Otherwise, it returns to the IDLE state.
- (3) **Continue reading or waiting state:** After reading one dataset, the system checks if the read enable is active and the FIFO is not empty (Rd_en & !fifo_empty). If valid, it continues reading data; otherwise, it transitions to the IDLE state waiting for the trigger condition.

The data writing process consists of three states, namely idle, writing, and continuous writing or waiting.

- (1) **Idle state:** After reset, the system waits for the trigger condition in the IDLE state.
- (2) **Writing state:** If the write enable is active and the FIFO is not full (Wr_en & !fifo_full), the system enters the writing state, where the FPGA performs the write operation and increments the write counter. Otherwise, it returns to the IDLE state.
- (3) **Continue writing or waiting state:** After writing one data, the system checks if the write enable is active and the FIFO is not full (Wr_en & !fifo_full). If valid, it continues writing data; otherwise, it transitions to the IDLE state in anticipation of the trigger condition.

3.2.2 Data framing and packaging

After the ADC samples and quantizes the analog voltage signal, it outputs a 14-bit parallel data stream. The signals were framed in a specific data format for ease of extraction and analysis. As shown in Fig. 16, each dataset consists of 33 sampling points. The framed data are stored in an asynchronous FIFO buffer from which the data packaging module packages and transmits data. The header (55AA) and footer (5AA5) identify the packet, with the second bit indicating the channel (Integrators A or B). Bits 3–6 were reserved for future use, whereas the remaining bits contained 33 sampled data points.

3.2.3 Baseline restoration

The ADC-sampled data were temporarily stored in FIFO. When the data read condition was met, the FIFO read-enable command was triggered to retrieve the data; these data serve as the basis for subsequent pulse baseline calculations. Baseline calibration is required because baseline drift may occur owing to the detector and conditioning circuitry. The FPGA controls the ADC to sample N points and computes the average, yielding the current baseline value B_{AVG} , as shown in Eq. (7)

$$B_{\text{AVG}} = \frac{1}{N} \sum_i^N V_i, \quad (7)$$

where V_i denotes the amplitude of the i th sampled waveform point. After the baseline calculation, the charge was determined by summing the data from M sampled points, as shown in Eq. (8)

$$Q = K \cdot \sum_{i=N}^M (V_i - B_{\text{AVG}}) \cdot \Delta t, \quad (8)$$

where K is the conversion gain of the conditioning circuit, and Δt is the sampling time for each sample.

3.2.4 Real-time host computer software design

The host–computer software interface is shown in Fig. 17. This interface allowed us to select the data format, set the integration duration, and configure the FPGA. The right side displays a plotting area where data are processed by using two threads: One stores the data in a “.dat” file, whereas the other performs real-time analysis and plotting.

During event analysis, 33 sampled points were used to reconstruct the complete waveform. However, because this study focuses on amplitude, the points from the 20th to the 30th, where the amplitude is stable, were selected for calculation. To minimize baseline drift errors, the first five points of 33 were used as baseline pre-samples. An accurate peak-to-peak amplitude was obtained by subtracting the baseline value from the stable amplitude value. The AFE system used a dual-gated integrator architecture. To reduce the integrators’ errors, standard charge values are used in the host software to correct integrators A and B.

Fig. 16 (Color online) Schematic showing the data format

Packet Header	Indicator	Reserved Bit	Data	Packet Trailer
55AA	A/B	0	Sampling Point Data 1,2... to Sampling Point Data 33	5AA5

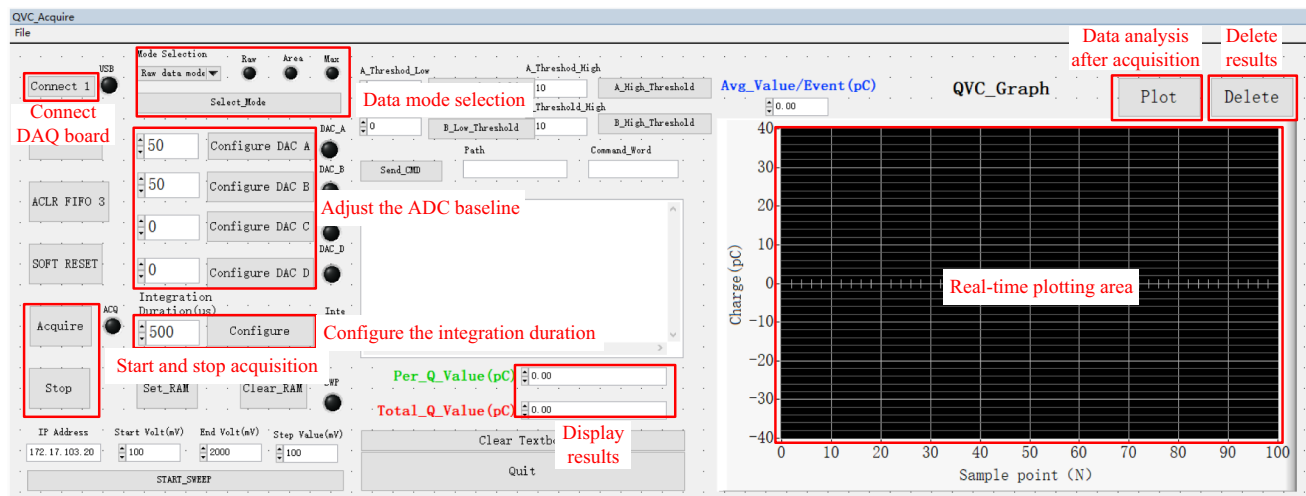


Fig. 17 (Color online) Host-computer software program interface

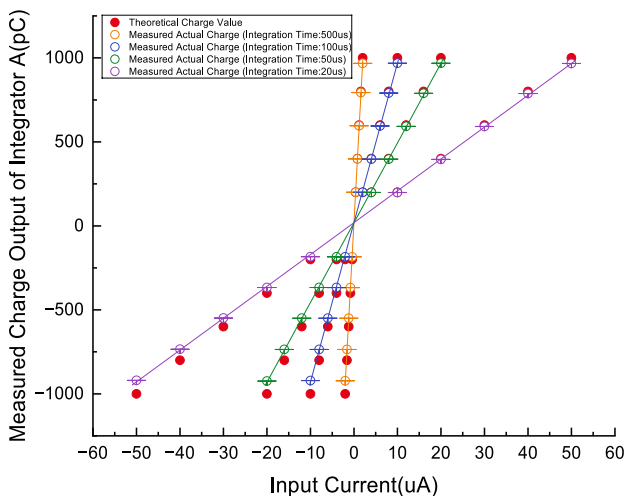


Fig. 18 (Color online) Plots of the AFE output charge errors vs. theoretical charges at different integration durations

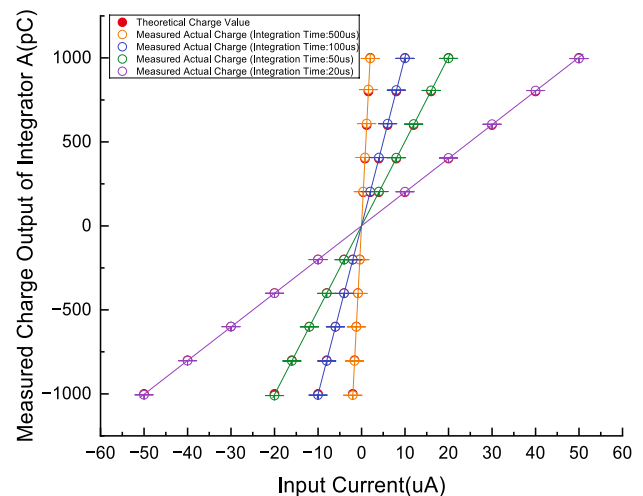


Fig. 19 (Color online) Plots of AFE output charge error vs. theoretical charge at different integration durations after calibration

4 Performance test

4.1 Electronics performance test

4.1.1 Calibration of the integration capacitance

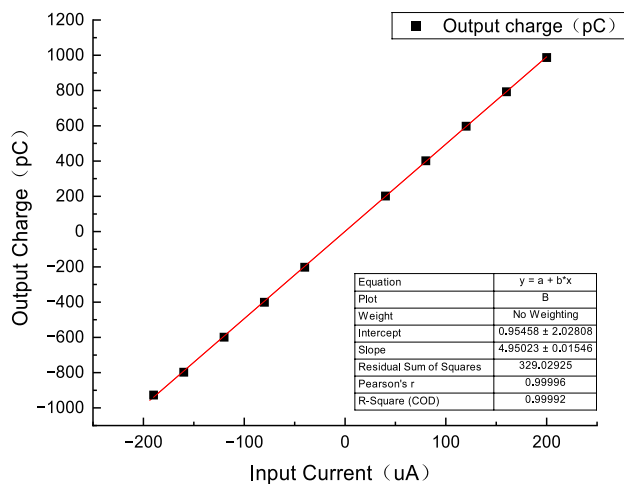
In the laboratory tests, a 100-pF on-chip integrating capacitor was used for integration. Figure 18 shows the linearity characteristics between the integrator's measured and the theoretical charge outputs at different integration times (20 μ s, 50 μ s, 100 μ s, 500 μ s). The red circles represent the theoretical charge output, whereas the orange (500 μ s), blue (100 μ s), green (50 μ s), and purple (20 μ s) circles

represent the charge outputs measured under various conditions. Significant deviations were observed primarily because of the discrepancy between the actual and nominal values of the integrator capacitor.

To reduce this error, the capacitance was calibrated, and the results were compensated using the corrected capacitance. After the calibration, the error between the measured and theoretical charge outputs was significantly reduced, with the measurements closely matching the theoretical values, as shown in Fig. 19. The maximum nonlinear error after correction is 0.55% (linear correlation coefficient $R^2 = 0.99996$). The T-shaped symbols in hollow circles in Figs. 18 and 19 represent the standard deviation error bars, which are calculated according to

Table 2 Integral nonlinearity error at different integration durations

Integration time (capacitance)	Current measurement range (dead zone measurement)	Nonlinear error (COD)
5 μ s (100 pF)	−190 μ A to +200 μ A (−180 nA to +180 nA)	0.67% ($R^2 = 0.99992$)
20 μ s (100 pF)	−50 μ A to +50 μ A (−30 nA to +30 nA)	0.35% ($R^2 = 0.99998$)
50 μ s (100 pF)	−20 μ A to +20 μ A (−12 nA to +12 nA)	0.24% ($R^2 = 1.00000$)
100 μ s (100 pF)	−10 μ A to +10 μ A (−8 nA to +8 nA)	0.42% ($R^2 = 1.00000$)
500 μ s (100 pF)	−2 μ A to +2 μ A (−1 nA to +1 nA)	0.52% ($R^2 = 0.99996$)
1 s (0.5 pF)	−4 pA to +4 pA (−1 pA to +1 pA)	0.24% ($R^2 = 0.99993$)

**Fig. 20** (Color online) Nonlinear error and coefficient of determination in the full range

Eq. (9) by measuring each data point in this test five times (yielding 400 sets of measurements in total).

$$SD = \sqrt{\frac{1}{N-1} \sum_{i=1}^N (x_i - \bar{x})^2} \quad (9)$$

where x_i is a data point, $\bar{x}$ is the mean value, and N is the sample size.

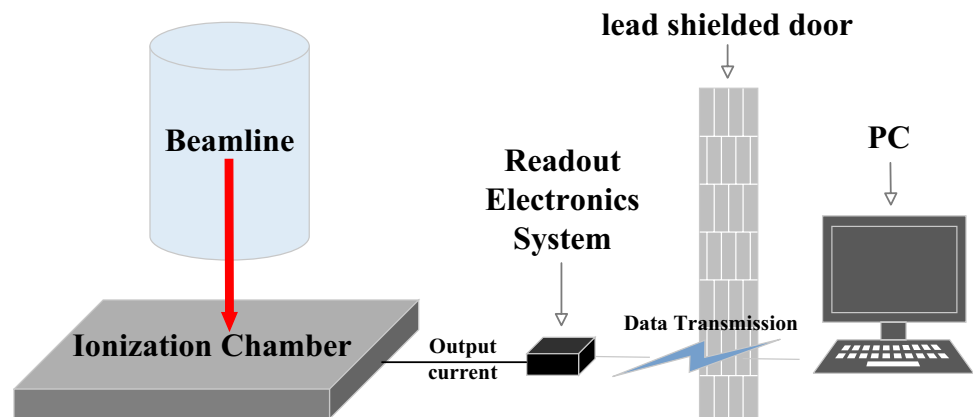
4.1.2 Nonlinear error test

When the integrator capacitor is fixed at 100 pF, the measurable current dynamic range varies with different integration times. Five integration times were selected as distinct ranges, and fitting was performed using the Origin software program to calculate the nonlinear error over the entire range. The results are listed in Table 2. When the integration time is 1 s and the capacitor is 0.5 pF, the laboratory-measured minimum current range is $-1 \text{ pA} - +1 \text{ pA}$.

Figure 20 shows the linear fit curve for the entire measurement range, with a nonlinear error in the range of $-190 \mu\text{A} - +200 \mu\text{A}$ of 0.67% and a coefficient of determination of $R^2 = 0.99992$. The tests demonstrated that the system offers high accuracy, broad dynamic range, good linearity, and excellent performance in ultralow current measurements.

4.2 Beam experiment

To verify the system's real-time monitoring capability at high dose rates, beam tests were performed in April 2024 (after the entire electronics system was completed) using the ionization chamber detector in terminal TR4 of the HIRFL. The TR4 terminus uses heavy ions at varying dose rates for fundamental research on heavy-ion cancer therapy and clinical trials for treating superficial tumors in humans. The experimental layout of the beam is illustrated in Fig. 21. The carbon-ion beam was extracted into the atmosphere and

Fig. 21 (Color online) Beam test scheme diagram

passed through a dose ionization chamber detector, which converted the ion signal into current. This current was then input to a real-time dosimetry monitoring system. The host computer was located in the control room and remotely controlled the data acquisition.

A field image of the test is shown in Fig. 22; it includes the ionization chamber detector (a), which transmits the current signal to the AFE (b) for voltage conversion. The DAQ (c) samples and processes the signal, and the results are displayed on the host computer.

Before the experiment, all the integrator capacitances were calibrated in the laboratory to ensure accurate results. In conventional and high-dose radiotherapy, the dose rate is typically < 20 Gy/min. Monitoring at higher dose rates imposes stricter demands on the dynamic range, response rate, stability, and system's accuracy. To evaluate the real-time monitoring performance of the system at higher dose rates, the beam dose range was set to 65–120 Gy/min. The terminal dose was updated every second, with the AFE circuit using a 10 pF capacitor and an integration time of 16 μ s, corresponding to 62,500 events per second.

After the analysis of the sampled current signals, a linear fit of the curve of the ionization chamber output current versus dose variation was obtained (see Fig. 23). Each data point represents the current at different beam dose levels, and the coefficient of determination is $R^2 = 0.9998$. The results show that the system can stably operate at dose rates of up to 120 Gy/min, meeting the real-time monitoring requirements for both conventional and high-dose radiotherapy, demonstrating its potential for use in ultrahigh-dose rate radiotherapy (FLASH-RT).

5 Discussion

In 2010, Furukawa and Torikoshi from the National Institute of Radiological Sciences (NIRS) in Japan measured the HIMAC dosimetry (from 1 nA [41] to 1000 nA [30]), yielding a nonlinear error of less than 1% and a dose rate of approximately 1 Gy/min. In 2017, Binqing Zhao at the

Shanghai Institute of Applied Physics at the Chinese Academy of Sciences developed a proton therapy beam delivery system with a dosimetry range of $-400 - 60$ nA, an approximate dose rate of 2 Gy/min, and a maximum linear error of ± 0.04 nA [39]. In 2020, Diffenderfer's team at the University of Pennsylvania designed a proton FLASH-RT system with a dose rate in the range of 60–100 Gy/s and a maximum beam current of 300 nA, showing a linear relationship between the proton current and the dose rate ($R^2 = 0.9952$) [33]. In 2024, Yagi et al. developed dosimetry electronics for HIMAC's UHDR carbon-ion beam with a range of -0.5μ A to -50μ A, dose rates up to 102.54–115.38 Gy/s, and a linear relationship between the ion chamber current and electronic output frequency within $\pm 1\%$ [34]. Compared with existing dosimetry electronic systems, this system offers a measurement range of ± 1 pA to $\pm 200 \mu$ A and is capable of reading both positive and negative signals, yielding a nonlinear error of $< 0.67\%$ ($R^2 = 0.99992$). This meets the ionization chamber current-monitoring requirements of most conventional and FLASH-RT dose detectors. As domestic FLASH radiotherapy terminals are still under

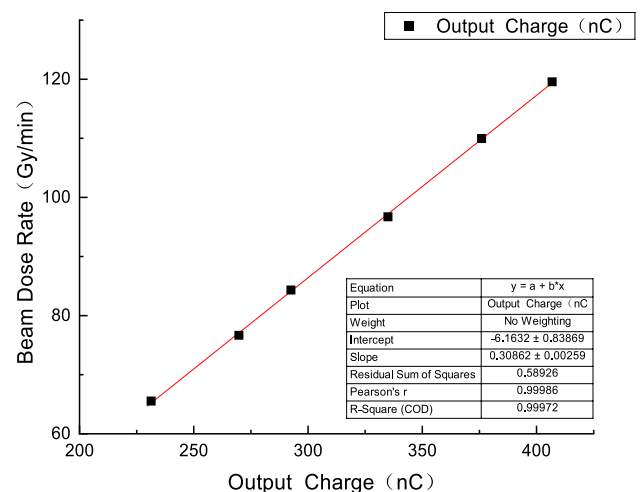
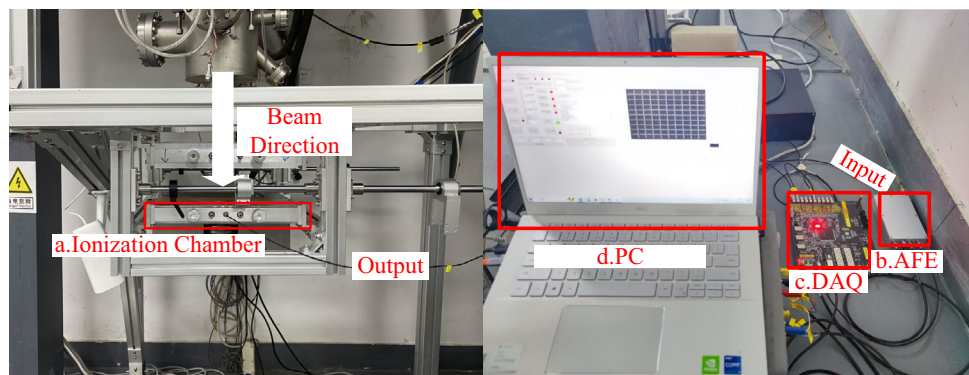


Fig. 23 (Color online) Linear fit of ionization chamber output current vs. dose rate

Fig. 22 (Color online) Beam test field diagram



development, this system has not yet been validated using FLASH beams. Nonetheless, its broad dynamic range, high linearity, and dead-time-free features demonstrate the potential for future FLASH-RT research and clinical applications. In future work, we will optimize further the experimental design and systematically explore and establish a feasible and reasonable error evaluation method by determining and including error bars in similar measurements.

6 Conclusion

This study presented an innovative real-time dosimetry monitoring system for heavy-ion radiotherapy, validated experimentally on a TR4 terminal. The system detects bipolar currents within a range of $-190\ \mu\text{A}$ – $+210\ \mu\text{A}$, maintains a nonlinear error below 0.67%, and offers a single-event processing time as low as 5 μs . The system achieved high-accuracy real-time monitoring within a dose rate range of 65–120 Gy/min in the beam experiments. Compared with existing radiotherapy dosimetry systems, it eliminates signal processing dead time in the front-end circuit, ensuring continuous and accurate dose measurements. The current measurement range of the system spans eight orders of magnitude ($-1\ \text{pA}$ – $-190\ \mu\text{A}$, $+1\ \text{pA}$ – $+190\ \mu\text{A}$), considerably enhancing its versatility across different applications. This system is optimized for high-precision monitoring of ionization chamber output currents and is compatible with various radiotherapy modes; it is also suitable for real-time dose measurement in heavy-ion radiotherapy and can be extended to electron, proton, and other high-energy particle radiotherapies, demonstrating broad application potential. To meet the growing demand for higher dose rates and support cutting-edge applications like FLASH-RT, we are developing a new generation of ultrafast front-end processing circuits and data acquisition systems. This system achieves sampling rates up to 250 MSps, data-transmission speeds $> 10\ \text{Gb/s}$, and a broader input dynamic range, enhancing the real-time monitoring capabilities in high-dose rate environments. These improvements will not only expand the system's applicability in high-dose radiotherapy but also provide a more reliable real-time dosimetry solution for accurate radiotherapy.

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Author Contributions All authors contributed to the study conception and design. Material preparation, data collection, and analysis were performed by Ling-Ling Liu, Qian-Shun She, Jie Kong, Jun-Wei Yan, and Yu-Han Dou. The first draft of the manuscript was written by

Ling-Ling Liu, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data Availability The data that support the findings of this study are openly available in Science Data Bank at <https://cstr.cn/31253.11.sciencedb.j00186.00900> and <https://www.doi.org/10.57760/sciencedb.j00186.00900>.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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