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An 8-channel, 46-ps-precision TDC ASIC with improved vernier delay loop for STCF EMC

Zi-Wei Zhao[1] · Ran Zheng[1,2] · Chao Liu[1] · Jia Wang[1] · Xiao-Min Wei[1] · Fei-Fei Xue[1] · Rui-Guang Zhao[1] · Yann Hu[1]

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Abstract

An 8-channel time-to-digital converter (TDC) with high precision and linearity designed for the electromagnetic calorimeter (EMC) in the Super Tau-charm Facility (STCF) is presented. A 3-level quantization structure is employed in the proposed TDC to achieve high time resolution and wide dynamic range simultaneously. A double-edge-triggered counter characterized by the elimination of metastability is used as the first level. The second and third levels are, respectively, implemented with a polyphase clock sampler and a modified Vernier delay loop (VDL) with an automatic reset mechanism. Two low-jitter delay-locked loops (DLLs) with different lengths are utilized to assist in vernier measurement and polyphase clocks are also provided by one of the DLLs. A theoretical analysis with respect to the optimal combination of DLL length and reference clock frequency is presented. The proposed 8-channel TDC was implemented using 180 nm standard CMOS process with 1.8 V power supply. Under a reference clock frequency of 100 MHz, the TDC is realized with a resolution of 41.7 ps and a dynamic range of 2560 ns. According to the results of an experimental evaluation, the best single-shot precision was 46 ps, and good consistency was observed among all channels. The results also establish that the sliding scaled technique improved conversion linearity. In asynchronous measurements, the maximum differential nonlinearity (DNL) and the integral nonlinearity (INL) were less than 0.4 LSB and 0.5 LSB, respectively.

Keywords STCF · TDC · Vernier · Sliding scaled technique · High linearity

1 Introduction

As key components of time measurement electronics, time-to-digital converters (TDC) have attracted considerable attention as a topic of active research in nuclear detection [1, 2] and medical imaging [3]. The Super Tau-charm Facility (STCF) currently under construction in China is a new experimental facility for particle physics based on an accelerator with ultrahigh luminosity [4]. The STCF facility is equipped with multiple detectors, including an electromagnetic calorimeter (EMC) which is used to measure the energy of photons and electrons with high efficiency and high resolution. In addition, sufficient time resolution for STCF EMC is also required for background suppression, gamma–neutron discrimination, and event identification [5]. A pure CsI (pCsI) crystal scintillator with an avalanche photodiode (APD) readout is adopted in the STCF EMC, and time stamps are acquired through a front-end readout circuit (ROC) with leading edge discrimination (LED) digitized

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✉ Ran Zheng
zhengran@nwpu.edu.cn

[1] School of Computer Science and Technology, Northwestern Polytechnical University, No. 1, Dongxiang Road, Changan District, Xi'an 710029, China

[2] Research & Development Institute of Northwestern Polytechnical University in Shenzhen, No. 45, Gaoxin South 9th Road, Nanshan District, Shenzhen 518063, China

with a TDC [6]. The time resolution for a full response is specified as better than 300 ps for 1 GeV energy deposits, including the optical process and the response of the APD and electronics [7]. While the decay time of pCsI used in this experiment was as long as 30 ns [8], the large capacitance (270 pF) of the adopted APD detector (Hamamatsu S8664-1010) result in considerable input noise at the front-end circuit [5]. Given these two factors, obtaining the time precision of an ROC at an ultrahigh level is a notable challenge. For example, an ROC for APD with a time precision of 270 ps has been implemented by our team [9]. To realize a target time resolution of 300 ps for electronics, the TDC is expected to reach a resolution of 100 ps. Because an excessive number of readout channels (6732 for the barrel part and 1938 for the endcap part [7]) are expected to be implemented in the detector, the ROC and TDC have been monolithically integrated on an application-specific integrated circuit (ASIC) for high operational efficiency. The aim of this study was to investigate the TDC ASIC suitable for multichannel integration with a resolution of 100-ps or less and high linearity.

A number of time-to-digital conversion algorithms and architectures have been proposed over the past few decades. ASIC-based TDCs can be divided into three categories [10], including sampling, noise-shaping, and stochastic TDC. Although noise-shaping TDC is performed with multiple samples to obtain a high resolution, it is not applicable here due to the requirement for real-time measurement and a high counting rate in STCF ECAL. Stochastic TDC is also not suitable in this application scenario because of the large die area it occupies [11]. The counter-based TDC is the simplest sampling TDC structure that has a scalable dynamic range ; however, it requires a high-frequency oscillator to realize a high resolution (for example, an oscillator with eight phases and a frequency of 3.125 GHz was employed to obtain a resolution of 40 ps in [12]). The tapped delay line is a popular and easily realized TDC, although its resolution is typically limited by the channel length of the transistor. The unit delay of such TDCs can be relatively fixed using a delay-locked loop (DLL) [13] or phase-locked loop (PLL) [14] to overcome the limitations of variations in process, voltage, and temperature (PVT). The front-end circuit was realized using a 180 nm CMOS process with a 3.3 V power supply to obtain better dynamic range and noise performance. As a result, given that the device is manufactured with the same process, developing a controlled gate with a propagation delay lower than 100 ps would be challenging. Thus, using only the counter or the delay line cannot achieve our design goals. Pulse shrinking [15] and time amplification [16] involve sampling TDC structures with a sub-gate-delay resolution, both operating with the propagation delay difference between the leading edge (rising edge) and the trailing edge (falling edge) of the input pulses. However, the unavoidable mismatch of delay cells in these two TDC structures usually leads to poor consistency across multiple channels. Successive-approximation TDC [17] is an alternative approach for high-resolution TDC; however, a long conversion time is one of its primary drawbacks. Considering its high resolution, high counting rate, and superior multichannel consistency, the vernier TDC [18–21] is considered more preferable in real-time measurements. Compared with the Vernier delay-line TDC, the cyclic Vernier TDC has some notable advantages in terms of area occupation and conversion linearity, while lagging in terms of conversion speed [18]. Nonetheless, the cyclic Vernier TDC can still reach a relatively high speed (i.e., a conversion rate of 6.67 MS/s was realized in [18]).

The Nutt method [22] was proposed with a counter and two fine time-interpolators to obtain a high resolution (100 ps) and a large dynamic range (2-μs) simultaneously. The counter is used to obtain the number of clock cycles between Start and Stop events, and the start and stop interpolators are used to measure the interval between Start/Stop signals and their first subsequent clock rising edge. Then, the measured interval between the start and stop signals can be expressed as

$$T_{\mathrm{IN}} = T_{\mathrm{REF}} + T_{\mathrm{S1}} - T_{\mathrm{S2}}, \tag{1}$$

where T_{REF}, T_{S1} and T_{S2}, respectively, denote the measurement results of the counter and the start and stop interpolators. A finer resolution can be realized when the start and stop interpolators are further divided into additional measuring levels. Another merit of the Nutt method based TDC is that it naturally implements the sliding scaled technique [20], which can greatly improve the measurement linearity of TDC.

In this study, we propose an 8-channel, 3-level TDC based on the Nutt method to meet the requirements of STCF EMC. The first level was realized using a coarse counter and a second level based on polyphase clock sampler is then used to measure the time residue of the first level. The time margin of the second level is quantized using a modified Vernier delay loop (VDL), which serves as the finest level of this TDC. The polyphase clocks utilized at the second level are provided by a low-jitter DLL, which performs vernier measurements in conjunction with another shorter DLL, at the finest level.

The remainder of this study is organized as follows: In Sect. 2, we introduce the overall framework and principles of the proposed TDC and provide an analysis of some key parameters. The circuit designs of the proposed DLL and 3-level TDC are described in Sect. 3. The experimental setup is presented in Sect. 4 along with the results of the

measurements. We then conclude by summarizing our findings and suggesting some possible avenues for future research in Sect. 5.

2 Framework and analysis

2.1 Framework and principles of the proposed TDC

Figure 1 shows the overall framework of the proposed TDC and the structure of a single channel. The PLL, DLLs and coarse counter are global for the chip, and eight TDC channels with the same structure can operate independently. In actual applications with ROC, one TDC channel is used to sample the external start signal and the trigger signal generated by ROC, also called as the stop signal, is measured by another channel. The time interval between the start and stop, which is known as a timestamp, is calculated and stored off-chip.

The reference clock of the chip, referred to as Clk, can be furnished by an integrated PLL or directly from the off-chip clock source. As shown in Fig. 1, DLL-1 and DLL-2 using Clk as the input clock are composed of delay lines with n and $n-1$ delay cells, respectively. The counter as the first TDC level can be triggered by both the rising and falling edges of Clk. The results of the counter are delivered continuously to each TDC channel. The second TDC level is realized with multiphase clocks produced by DLL-1, which are fed to the clock sampler in each channel. The residual time of the second level, also known as the time interval between the hit event and its subsequent polyphase clock's rising edge, is measured by the third TDC level—a VDL. The vernier measurement is carried out utilizing the slightly different delay-times between two delay cells τ_1 and τ_2, which are, respectively, controlled by DLL-1 and DLL-2. The resolution of TDC is determined by the third level and is represented as given in Eq. 2.

$$Re = \tau_2 - \tau_1 = \frac{1}{(n-1)f_0} - \frac{1}{nf_0} = \frac{1}{n(n-1)f_0}, \tag{2}$$

where f_0 denotes the frequency of Clk. The dynamic range of TDC is proportionate to the number of counter digits, which can be increased according to the limits of power consumption and die area [23]. We can use Eq. 3 to signify the dynamic range of this TDC in which N_1 denotes the number of counter digits.

$$DR = \frac{2^{N_1}}{f_0}. \tag{3}$$

2.2 Tradeoffs among key parameters

From Eq. 2, it may be observed that the values of n and f_0 should be increased to obtain a finer resolution, which means that we should insert more delay cells in DLLs or use a reference clock of higher frequency. The precision of a TDC primarily involves two components, including quantizing and random noise. The former depends on the

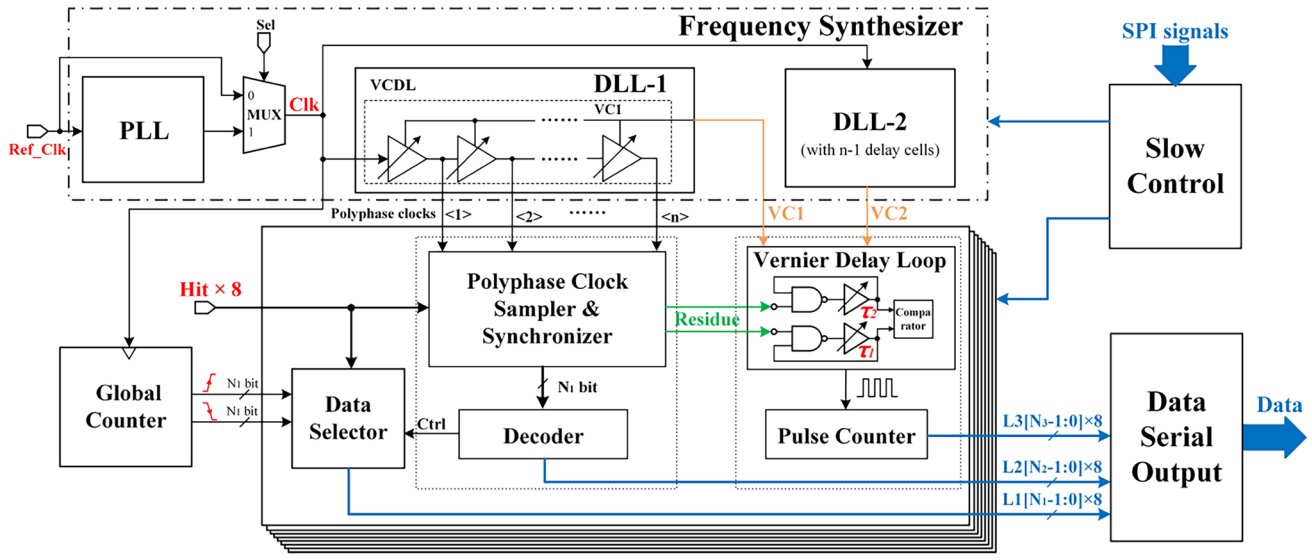

Fig. 1 (Color online) The structure of the proposed 8-channel TDC

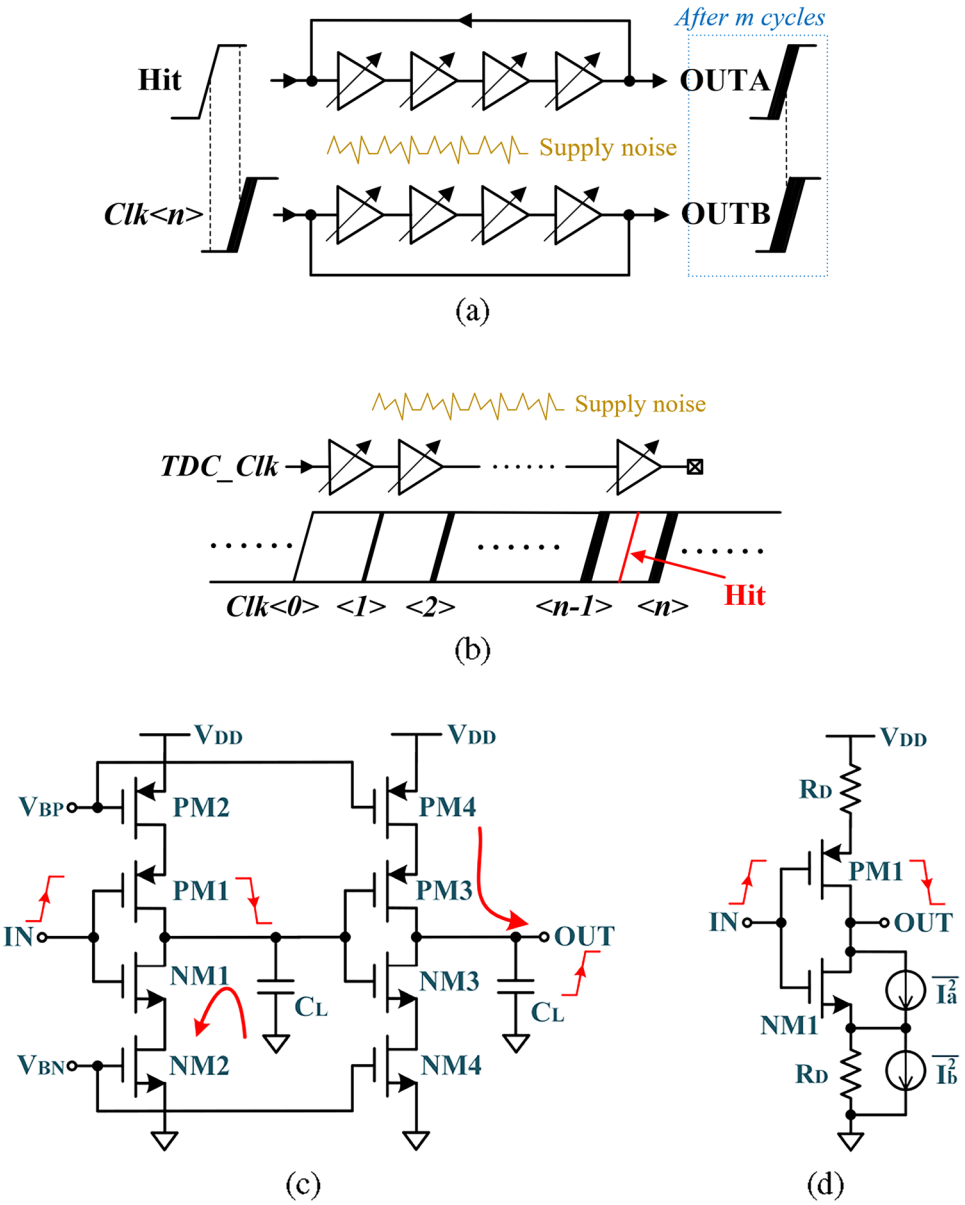

Fig. 2 (Color online) **a** Jitter accumulations in the second level. **b** Jitter accumulations in the third level. **c** The simplified schematic of delay cell. **d** The noise model of delay cell

resolution, which can be obtained in the time domain as follows [13]:

$$\sigma_q = \frac{Re}{2\sqrt{3}}. \tag{4}$$

The jitters generated from the reference clock, the hit signals, and those produced by DLLs likewise worsen the precision by contributing to random noise in the phase domain. Assuming that the clock and hit signals are as clean as expected, jitter mostly arises from DLLs. Figure 2a shows how the jitter from DLLs affects the precision of TDC. The hit signal is assumed to be located between $Clk\langle n-1\rangle$ and $Clk\langle n\rangle$ provided by DLL-1 such that a replica of $Clk\langle n\rangle$ is delivered to the VDL for the finest quantization. The jitter generated by a single delay cell is indicated as σ_0, owing to noise from the control voltage, power supply, and substrate. The jitter of $Clk\langle n\rangle$ is $\sqrt{n}\sigma_0$ which is also the maximum accumulated jitter of DLL-1. As shown in Fig. 2b, the cycling occurs for m times on loops corresponding to *Hit* and $Clk\langle n\rangle$, and OUTA and OUTB are output signals of VDL. Assuming that the jitters generated by the 4 cascaded delay cells in VDL are uncorrelated, the accumulated jitters on OUTA and OUTB are represented by Eq. 5 and Eq. 6, respectively.

$$\sigma_{r1} = \sqrt{4m}\sigma_0, \tag{5}$$

$$\sigma_{r2} = \sqrt{n + 4m}\sigma_0. \tag{6}$$

At the end of cycling, OUTA and OUTB are fed to an arbiter for phase comparison. Thus, the time uncertainty due to jitter can be regarded as the accumulation of σ_{r1} and σ_{r2} and is denoted as

$$\sigma_r = \sqrt{\sigma_{r1}^2 + \sigma_{r2}^2} = \sqrt{n + 8m}\sigma_0, \tag{7}$$

whereas the value of m can be deduced with the relation between τ_1 and Re as

$$m = \frac{\tau_1}{Re} = n - 1. \tag{8}$$

The total time uncertainty or time precision of TDC is represented as given below.

$$\sigma_T = \sqrt{\sigma_q^2 + \sigma_r^2}. \tag{9}$$

The proposed design includes a delay cell with symmetrical current-starved structure [24] as shown in Fig. 2c, which is characterized by almost equal rise and fall times. To avoid reversing the phase, the cell is composed of two current-starved inverters, the propagation delays of which are controlled by the output voltage of the DLL (VC1 or VC2). If we define the toggle point for both the rising and falling edges as $V_{DD}/2$, the unit propagation delay in DLL-1 can be obtained as

$$\tau_1 = \frac{V_{DD}C_L}{I_{CS}} = \frac{1}{nf_0}, \tag{10}$$

where C_L denotes the parasitic capacitance on the output node of each stage, I_{CS} denotes the mean value of the charging or discharging current through C_L during output level switching. According to [25], the phase noise of a delay cell is dominated by white noise, and the low-frequency noise can be neglected when the rising and falling edges are symmetric. Figure 2d shows the noise model of the delay cell considering a positive input step in which the noise contribution of PMOS is omitted. For simplicity, the bias transistors (NM2, PM2 in Fig. 2c) working in the triode region were replaced with resistors with negligible voltage drop. The input transistor (NM1 in Fig. 2d) is assumed to be saturated for simplification. Then, the spectral density of output noise [26] can be described by

$$S_{inN} = \frac{8kT\gamma I}{V_{DD} - V_{tN}} + \frac{4kT}{R_D}, \tag{11}$$

where V_{tN} is the threshold of NMOS and R_D denotes the value of the equivalent resistor of NM2 in Fig. 2c. As R_D can be considered a constant when the bias of NM2 is fixed, we adopted the phase-noise model for the inverter proposed in [27] to obtain the spectral density of the delay as given below.

$$S_{t_d} = \frac{t_d^2}{I_{CS}^2}\mathrm{sinc}^2(ft_d)S_{inN} \tag{12}$$

where t_d is the statics of the random delay variable, which can be represented as

$$t_d = \frac{\tau_1}{2} = \frac{V_{DD}C_L}{2I_{CS}}. \tag{13}$$

Then, the mean square value of t_d can be deduced using the Wiener–Khinchine theorem [27] as given below:

$$\sigma_{t_d}^2 = \int_0^\infty S_{t_d}\mathrm{d}f = \frac{t_d}{\pi I_{CS}^2}S_{inN}\int_0^\infty \mathrm{sinc}^2(x)\mathrm{d}x. \tag{14}$$

By applying Eqs. 10, 11, 12, and 13, this formula can be simplified to

$$\begin{aligned}\sigma_{t_d}^2 &= \frac{kTV_{DD}C_L}{I_{CS}^3}\left(\frac{2\gamma I_{CS}}{V_{DD} - V_{tN}} + \frac{1}{R_D}\right) \\ &= \frac{kT\left(\frac{2\gamma V_{DD}C_L}{V_{DD}-V_{tN}} + \frac{1}{R_D nf_0}\right)}{(V_{DD}C_L)^2(nf_0)^2}.\end{aligned} \tag{15}$$

On the assumption that the jitter produced with a negative input step is equivalent to that produced with a positive input step for a current-starved stage, the jitter of this delay cell with a positive input is represented by

$$\sigma_0^2 = 2\sigma_{t_d}^2. \tag{16}$$

Except for n and f_0, the terms in Eq. 15 can be regarded as constants. f_0 is confined within (50 MHz, 100 MHz) with respect to power consumption. For simplicity, the resolution of TDC is set to a fixed value (e. g. 45 ps). The quantized jitter σ_q in formula (Eq. 4) is also fixed. Thus, we only need to reduce the random part of the jitter, which is derived as given in Eqs. 2, 7, 8, 15, and 16.

$$\sigma_r^2 = \frac{(9n - 8)kT\left(\frac{2\gamma V_{DD}C_L}{V_{DD}-V_{tN}} + \frac{(n-1)Re}{R_D}\right)}{(V_{DD}C_L)^2((n-1)Re)^{-2}}. \tag{17}$$

From Eq. 17, we can understand that smaller values of n minimize the random jitter as much as possible. Given that Re is fixed at 45 ps, we determine that f_0=100 MHz and n=16. As a result, the ideal resolution of the proposed TDC is approximately 41.7 ps.

3 Design of circuit

3.1 Delay-locked loop

The structures of the two DLLs integrated into TDC are almost identical, as shown in Fig. 3a, except for the voltage-controlled delay lines (VCDLs) containing different numbers of delay cells. According to this analysis, the VCDLs in DLL-1 and DLL-2 contain 16 and 15 cells, respectively. A reference clock with a frequency of 100-MHz is fed to DLL-1 and DLL-2, which operate independently and do not need to be synchronized.

The lock controller [28] is used to prevent the DLL from false and harmonic locking events by comparing the first and several intermediate phases. The delay of VCDL is forced to range within 8 ns to 13.3 ns when the lock controller is enabled, which can also reduce the time required for the DLL to become locked. The phase detector operates in the first and last phases and determines the charging or discharging status of the charge pump. Complementary switches, dummy transistors, and a wide-swing-cascaded current mirror are adopted in the charge pump to improve the degree of matching between charging and discharging to obtain a much smaller locked phase error. In addition, a start-up circuit is used to provide an appropriate initial value to VC1 and VC2.

The VCDL is composed of 15/16 cascaded delay cells and 2 dummy cells, all of which were based on a modified current-starved structure. As shown in Fig. 3b, variable PMOS resistances (PM2, PM5) and variable NMOS resistances (NM2, NM5) are controlled by V_{BP} and VC1, respectively, which vary in opposite directions. With appropriate transistor dimensions, we can obtain an output with approximately equal rising and falling times across the tuning range. However, the transistor NM0 used for biasing can contribute considerable noise, so that only one bias circuit is used in the DLL and the two control voltages, VC1 and V_{BP}, are shared by all the involved delay cells either in the VCDL or in TDC channels. The constant MOS resistances (PM3, PM6, NM3 and NM6) are employed to supply a basic working current and guarantee that the delay cell still operates when VC1 is lower than the threshold voltage of NMOS, which can prevent the DLL from being inactive.

Figure 3c shows the simulated delay-voltage characteristics under different PVT conditions. The effective tuning range of this delay cell is 390 ps to 850 ps, which covers the expected unit delays for both two DLLs (625 ps for DLL-1

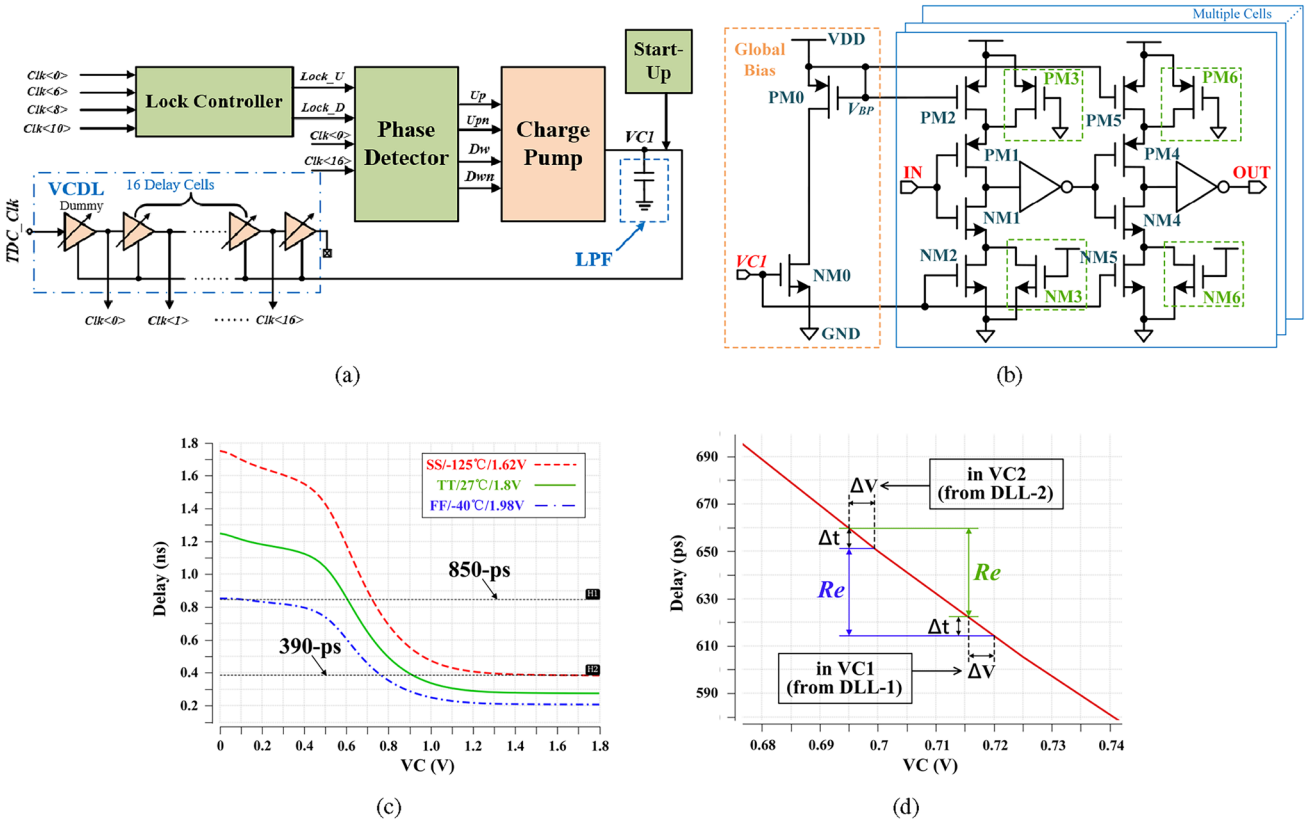

Fig. 3 (Color online) **a** The structure of DLL-1. **b** The implementation of symmetrical current-starved delay cell. **c** The delay-voltage characteristics of delay cell under different PVT conditions. **d** The effect of the control voltage shift on the TDC resolution

and 666.7 ps for DLL-2). As the control voltages are transferred to multiple channels with separate distances from the DLLs, the control voltages shift variously at each channel. As shown in Fig. 3d, we suppose that the shifts of VC1 given by DLL-1 and VC2 given by DLL-2 are both ΔV. Given the high linearity of the delay-voltage characteristics within a small voltage range, the unit delays controlled by VC1 and VC2 are both skewed by Δt. Therefore, the resolutions of all the channels can be considered as roughly consistent, as they are dominated by the difference between these two unit delays.

3.2 First and second levels

The first TDC level is based on an 8-bit global counter with a double-edge-triggered structure [29] as shown in Fig. 4a. The counting results CntP and CntN obtained with the rising and falling edges of Clk, respectively, are delivered to each channel simultaneously. The data selector in the channel is used to capture the proper counting result whenever the asynchronous Hit signal arrives, according to the result of the second level $L2[3:0]$ as shown in Fig. 4b. If the asynchronous input signal denoted by Hit is located in the first half of the clock cycle, we obtain $L2[3] = 1$ and CntN is chosen as the result of the first level. In the case that the Hit occurs in the second half of the clock cycle, CntP is selected. The implementation of a double-edge-triggered counter and appropriate settings is designed to eliminate the metastability of the counter.

One of the tasks of the second level is to measure the time interval between Hit and the first rising edge of Clk following the Hit, which can be realized using a polyphase clock sampler composed of 16 arbiters as shown in Fig. 4b. Another task is to transfer the residual time to the next level with the synchronizer. For example, if $Clk\langle 1\rangle$ is captured by the sampler, the residual time is the time elapsed between Hit and $Clk\langle 1\rangle$. Although well-matched loads are inserted in both signal paths of the synchronizer, there are still errors between the input and output intervals. According to a Monte Carlo simulation, the maximum error was approximately 5.1 ps, which is considered tolerable because the final resolution is much larger than the error.

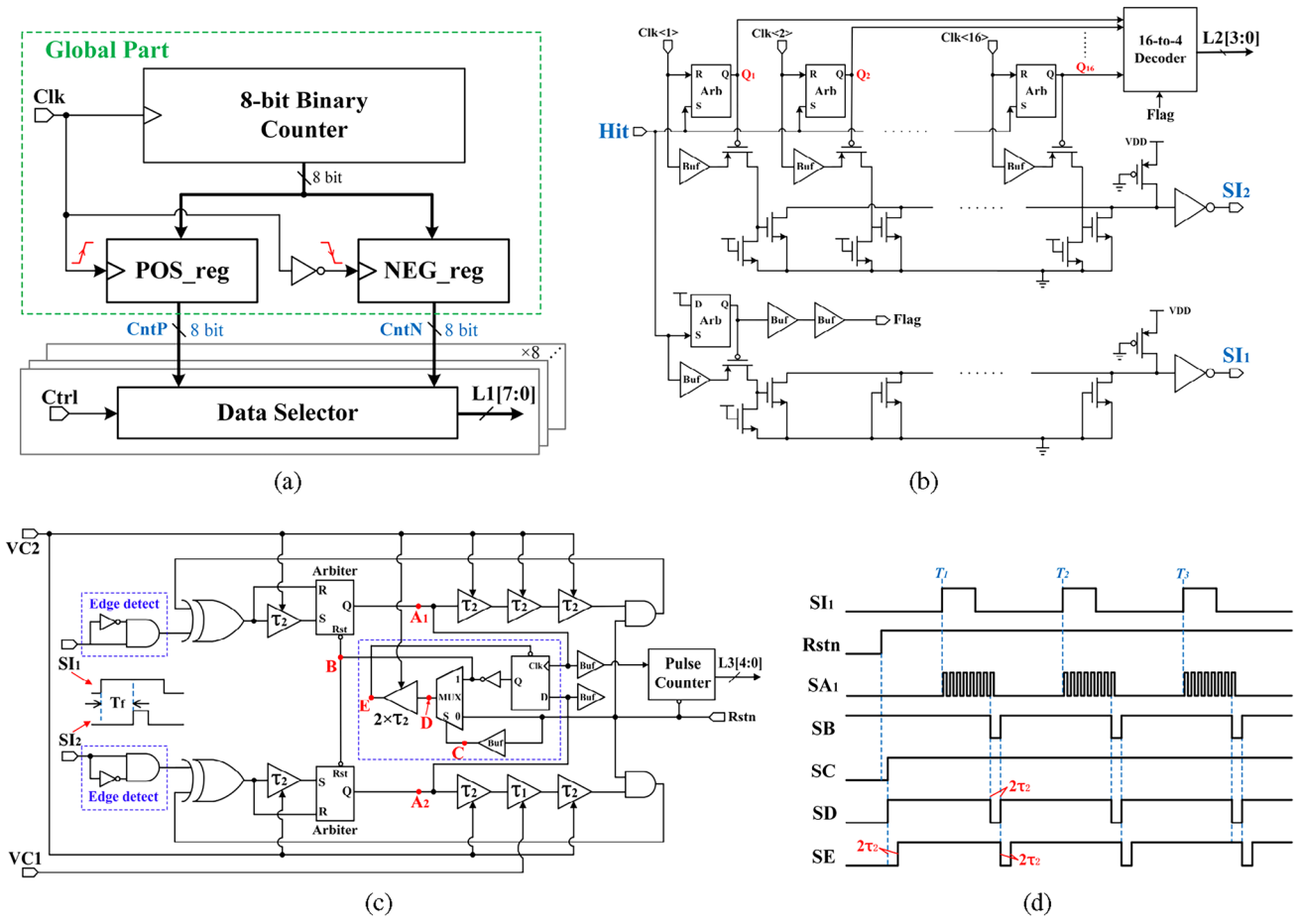

Fig. 4 (Color online) **a** Structure of double-edge-triggered counter. **b** Schematic of polyphase clock sampler and synchronizer. **c** The schematic of the modified VDL. **d** Timing diagram to illustrate the proposed automatic reset mechanism for VDL

3.3 Third level vernier delay loop

The VDL used to quantize the residual time of the second level is a modified version of that proposed in Ref. [18], as shown in Fig. 4c. The VDL contains two structurally identical loops. The loop with the input named SI_1 is a slow loop and that with the input named SI_2 is fast. SI_1 and SI_2 are the two outputs of synchronizer as shown in Fig. 4b. SI_1 precedes SI_2 and the interval between them is denoted by T_f varies within $0 \sim 625$ ps. The edge-detection circuit is used to generate a narrow pulse when the rising edge of SI_1/SI_2 arrives. There are 2 types of unit delays in each loop τ_1 and τ_2, which are regulated by the control voltages provided by DLL-1 and DLL-2, respectively. The single-delay cell and arbiter are used to convert the narrow pulse into a pulse with a width of τ_2. The cycle periods are determined by the 3-cascaded delay cells in the scenario that the delays of other logic on the loop can be neglected, which are $3\tau_2$ for the slow loop and $\tau_1 + 2\tau_2$ for the fast loop. As shown in Fig. 4c, signals at nodes A_1 and A_2 are denoted as SA_1 and SA_2, respectively. SA_1 precedes signal SA_2 by T_f before cycling, and the interval between SA_1 and SA_2 is decreased by $(\tau_2 - 2\tau_1)$ after each cycle. The cycling stops when SA_2 catches up with SA_1. The number of cycles required to align SA_1 and SA_2 can be obtained using the pulse counter and represented as

$$n_f = \left\lceil \frac{T_f}{\tau_2 - \tau_2} \right\rceil. \tag{18}$$

Ideally, the maximum n_f is 15, for which a 4-bit counter is sufficient. However, a redundant bit is added to calibrate the measurement results.

Because the VDL is expected to measure the arrival times of sequential pulses, an auxiliary circuit that can make VDL automatically reset after quantization is included as shown in the dotted box in Fig. 4c, where signals at nodes B, C, D, and E are denoted as SB, SC, SD, and SE, respectively. The timing diagram of the critical signals is shown in Fig. 4d. Before quantization, the global Rstn first takes SB to 0 to clear all nodes in the loop, and then, SB is pulled up to 1 to obtain a loop ready for cycling. The cycling stage of VDL begins as soon as SI_1/SI_2 arrives. When SA_1 and SA_2 are aligned after several cycles, the flip-flop samples are set to 1, SB is set to 0, and both two loops are cleared. Synchronized with SB, SD, and SE are successively pulled down to zero with a delay of $2\tau_2$. Subsequently, the flip-flop is cleared, and SB, SD, SE are pulled up to 1 in turn. After these steps, the VDL is once again ready for the next quantization. With this automatic reset mechanism, the maximum dead time of VDL is less than 45 ns, which implies that the conversion rate of a single channel can reach up to 22.5 MS/s. Considering the integration and serial readout of data from the 8 channels, the overall conversion rate of the proposed TDC chip can reach 5 MS/s. In addition to a fast ROC, the pileup effect in STCF EMC can be mitigated because the background counting rate is 1 MHz [7].

4 ASIC prototype and performance

4.1 ASIC prototype and experiment setups

The proposed 8-channel TDC was taped out using a standard 180nm CMOS process with a 1.8 V power supply; a microphotograph of the chip is shown in Fig. 5a. The layout of TDC channel is designed with a strip shape, and 8 channels are arranged in a column, which makes VC1 and VC2's distribution paths as short as possible. The chip has a die area of 1.55 mm × 1.42 mm, including the pad ring.

Figure 5b shows the experimental setup composed of an oscilloscope to observe the signal series, a spectrum analyzer for jitter measurement, 2 pulse generators to provide the reference clock and input signals of TDC, an FPGA board, an upper computer for chip control, and a logic analyzer used to collect and process the measured data. We adopt a clock generator chip, AD9552, to provide a 100MHz reference clock with a jitter below 1ps, rms. The reference clock is directly given by pulse generator in linearity evaluation.

4.2 Performance of DLL

Three chips were tested and verified, which are referred to as chip-1, chip-2, and chip-3. Unless specifically indicated otherwise, all measurements described below were performed with chip-2. Two approaches were adopted to obtain the jitter of DLL. The first was to obtain the phase noise curve of the last polyphase clock and integrate it within the frequency shift range of (10 kHz, 20 MHz), and the other was to measure the jitter directly with the oscilloscope. A jitter of 5 ps rms can be obtained using both approaches, which is much less than the resolution of TDC. The other performances are listed in Table 1.

4.3 Performance of TDC

For the first, we need to determine the actual resolution (LSB) of each TDC channel. Because the bin distributions are nearly consistent over all clock periods [29], we only need to evaluate the actual LSB within one clock period. One channel of the pulse generator is dedicated to providing the 100 MHz reference clock, and the TDC input with a frequency of 4.00001 MHz is derived from another channel. Thus, the interval between TDC input and the rising edge of the reference clock increases by 0.625 ps with each clock cycle. This interval is cyclically repeated within the range of

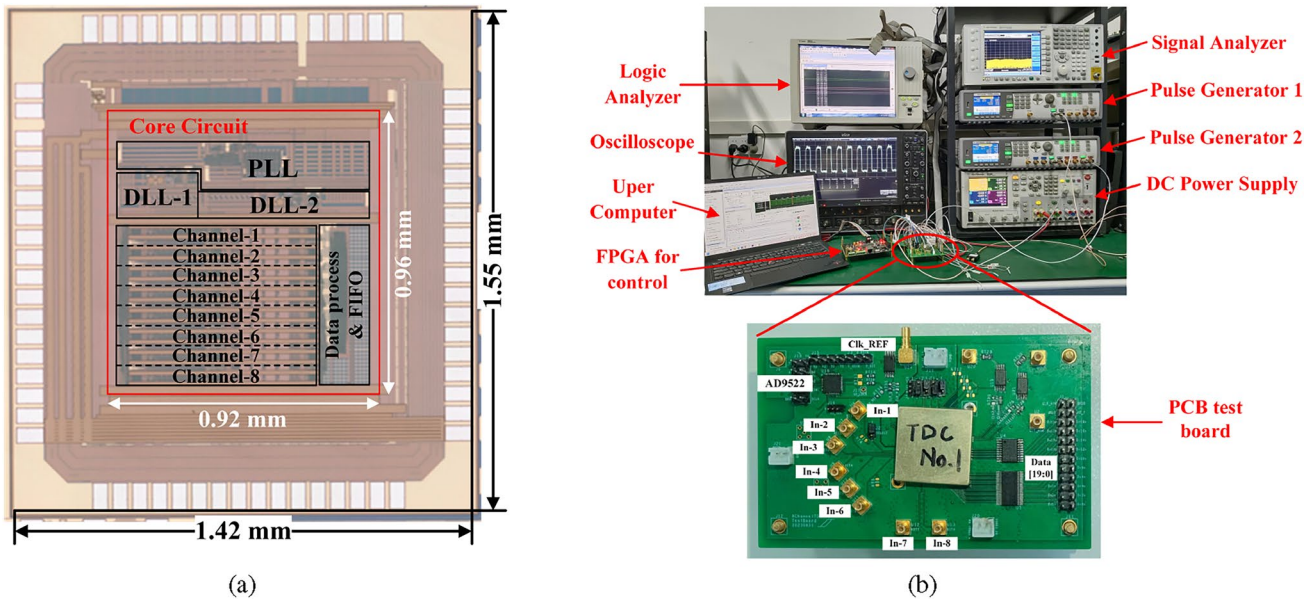

Fig. 5 (Color online) **a** The microphotograph of the proposed TDC chip. **b** The test system and PCB board for testing

Table 1 The performance of DLLs with 100MHz reference clock

Intex	DLL-1	DLL-2
Jitter of the last phase (ps, rms)	5.2	5.1
Duty cycle of the last phase	55%	54%
Locked error (ps)	29.9	35.4

0–10 ns, which can be considered as an approximate method for code density testing [30].

In ideal scenarios, the number of bins within the 10 ns measurement range is fixed (approximately 240) with an LSB size of approximately 41.7 ps. However, many non-ideal factors can cause the actual LSB to be either larger or smaller. The tested DNL and INL values of the second TDC level across eight channels with high consistency are shown in Fig. 6a and Fig. 6b, respectively. The nonlinearity of the second level mainly arose from mismatches of VCDL in DLL-1, which results in variable "margins" between the second and third levels. To explain this, we assume two types of step sizes for the second level with 600 ps and 650 ps, which are also intervals to be measured using VDL. Without considering nonideal factors in VDL, the resolution was fixed at 41.7 ps. Then, the sizes of VDL's last VDL bins for the input intervals of 600 ps and 650 ps were set to 16.2 ps and 24.5 ps, respectively.

A bin-size filtration mechanism was implemented to prevent the last bin within the VDL quantization range from becoming too narrow to worsen the DNL. First, the approximate magnitude of LSB was ascertained. If the size of the last bin was less than LSB/4, it was combined with the second-to-last bin into a new bin. Otherwise, the final bin was retained. The bin distribution of Ch-1 within a single clock period is shown in Fig. 6c. The LSBs of eight channels after processing are presented in Fig. 6d , which shows the approximate measured results across three chips. The LSB of Ch-1 was larger than those of the other channels, which can be explained by the significant deviation in the supply voltage in this channel.

The distribution ranges of DNL and INL in each of the eight channels over a single clock period (10 ns) are listed in Table 2. We also assessed the linearity in the asynchronous measurement mode, in which Ch-1 served as the start channel and one of the other channels served as the stop channel. The code density test was performed again, in which Start and Stop were provided by a single pulse generator with frequencies of 4.00001 MHz and 4 MHz, respectively. Because only the measurement results of the second and third levels are collected, the interval between the Start and Stop can be considered as randomly distributed within (0, 10 ns) with a 100 MHz reference clock. Table 3 shows the linearity performance of seven channel combinations, from which it may be observed that DNLs better than 0.4 LSB and INLs better than 0.5 LSB were obtained for all test cases. Comparing the test results of the single- and dual-channel methods demonstrates that the asynchronous TDC inherently employing the sliding scaled technique provides a great advantage in terms of linearity.

The single-shot precision (SSP) of the proposed TDC was measured in asynchronous mode. The output of the pulse generator was divided into two identical signals using a power splitter. One was transmitted to the start

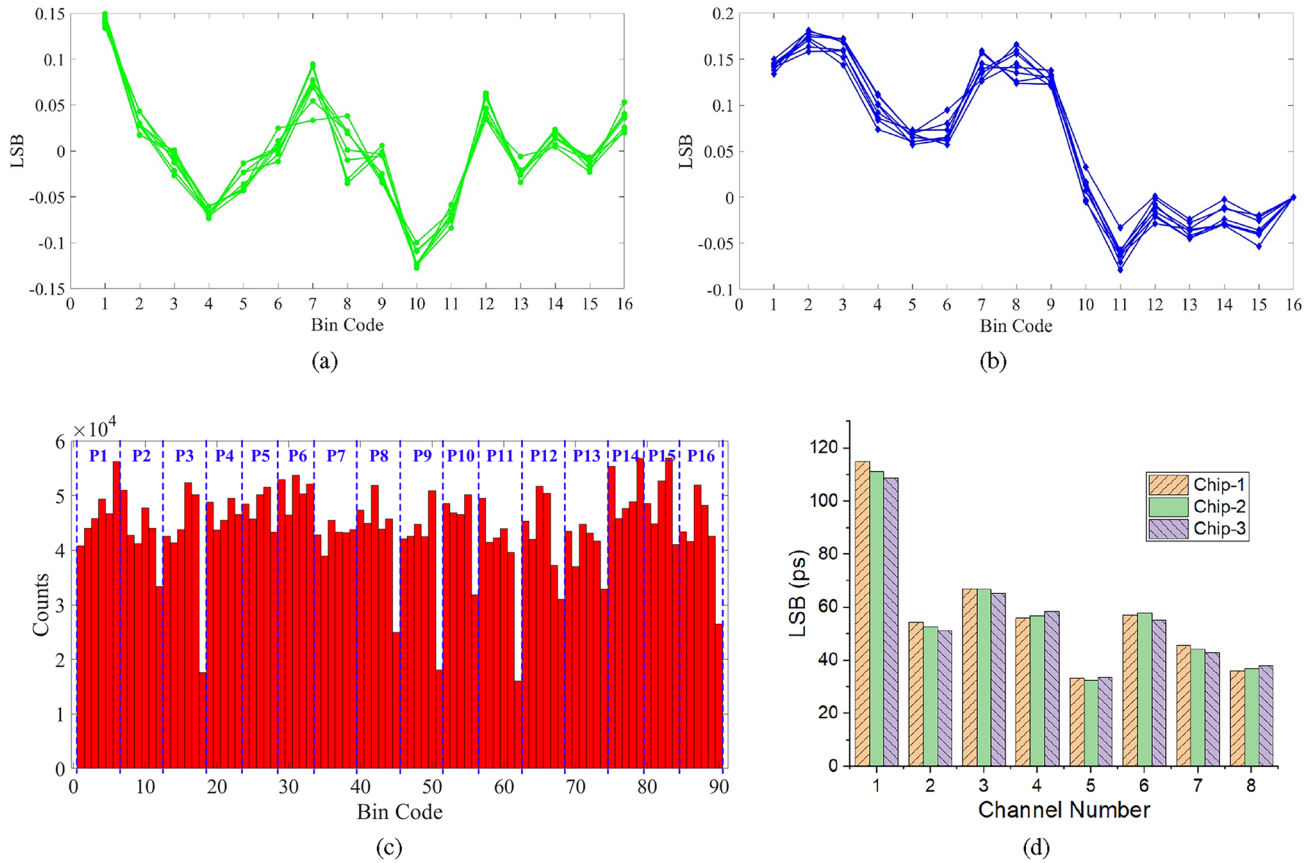

Fig. 6 (Color online) The test results of **a** DNL and **b** INL across eight channels, only considering the second level. (The bin code on the *x*-axis also represents the interval between two adjacent multiphase clocks.) **c** The bin distribution of Ch-1 within a measuring range of 10-ns. **d** The actual LSBs of eight channels across three chips

Table 2 The linearity performance of 8 individual channels

Channel number	DNL (LSB)	INL (LSB)
Ch-1	−0.64 ~ 0.28	−0.99 ~ 1.40
Ch-2	−0.66 ~ 0.44	−2.46 ~ 1.23
Ch-3	−0.68 ~ 0.60	−2.28 ~ 0.44
Ch-4	−0.71 ~ 0.48	−1.96 ~ 2.19
Ch-5	−0.73 ~ 0.83	−4.40 ~ 5.14
Ch-6	−0.70 ~ 0.47	−2.83 ~ 1.46
Ch-7	−0.66 ~ 0.58	−4.71 ~ 2.24
Ch-8	−0.54 ~ 0.67	−3.31 ~ 2.64

Table 3 The linearity performance of different combinations of Start channel and Stop channel

Start vs Stop	DNL (LSB)	INL (LSB)
Ch-1 vs Ch-2	−0.24 ~ 0.36	−0.45 ~ 0.24
Ch-1 vs Ch-3	−0.35 ~0.37	−0.22 ~ 0.49
Ch-1 vs Ch-4	−0.20 ~ 0.32	−0.15 ~ 0.44
Ch-1 vs Ch-5	−0.26 ~ 0.27	−0.23 ~ 0.48
Ch-1 vs Ch-6	−0.21 ~0.25	−0.25 ~ 0.38
Ch-1 vs Ch-7	−0.23 ~ 0.38	−0.31 ~ 0.34
Ch-1 vs Ch-8	−0.24 ~ 0.30	−0.33 ~ 0.50

channel (Ch-1) through a 0.1 m cable, and the other was transmitted to the stop channel (one of the other channels) through a 0.3 m cable, which is referred to as a cable delay measurement test [29]. The best uncalibrated SSP of 52.4 ps was obtained using a combination of Ch-1 and Ch-2, as shown in Fig. 7a. The precision was improved by using the look-up table for INL [31]. The principle of calibration is expressed as follows:

$$\mathrm{TDC_{CAL}} = \mathrm{TDC_{RAW}} + \mathrm{INL}[\mathrm{TDC_{RAW}}] \tag{19}$$

where $\mathrm{TDC_{RAW}}$ and $\mathrm{TDC_{CAL}}$ denote the raw and calibrated TDC digits, respectively. The calibrated SSP for 46 ps is shown in Fig. 7b. The tested SSPs with other channel combinations are shown in Fig. 7c, which are all in the range of 45 ps to 70 ps after calibration.

To validate the effectiveness of the calibration, we measured SSP along an input interval range of (0.5 ns, 10 ns). As

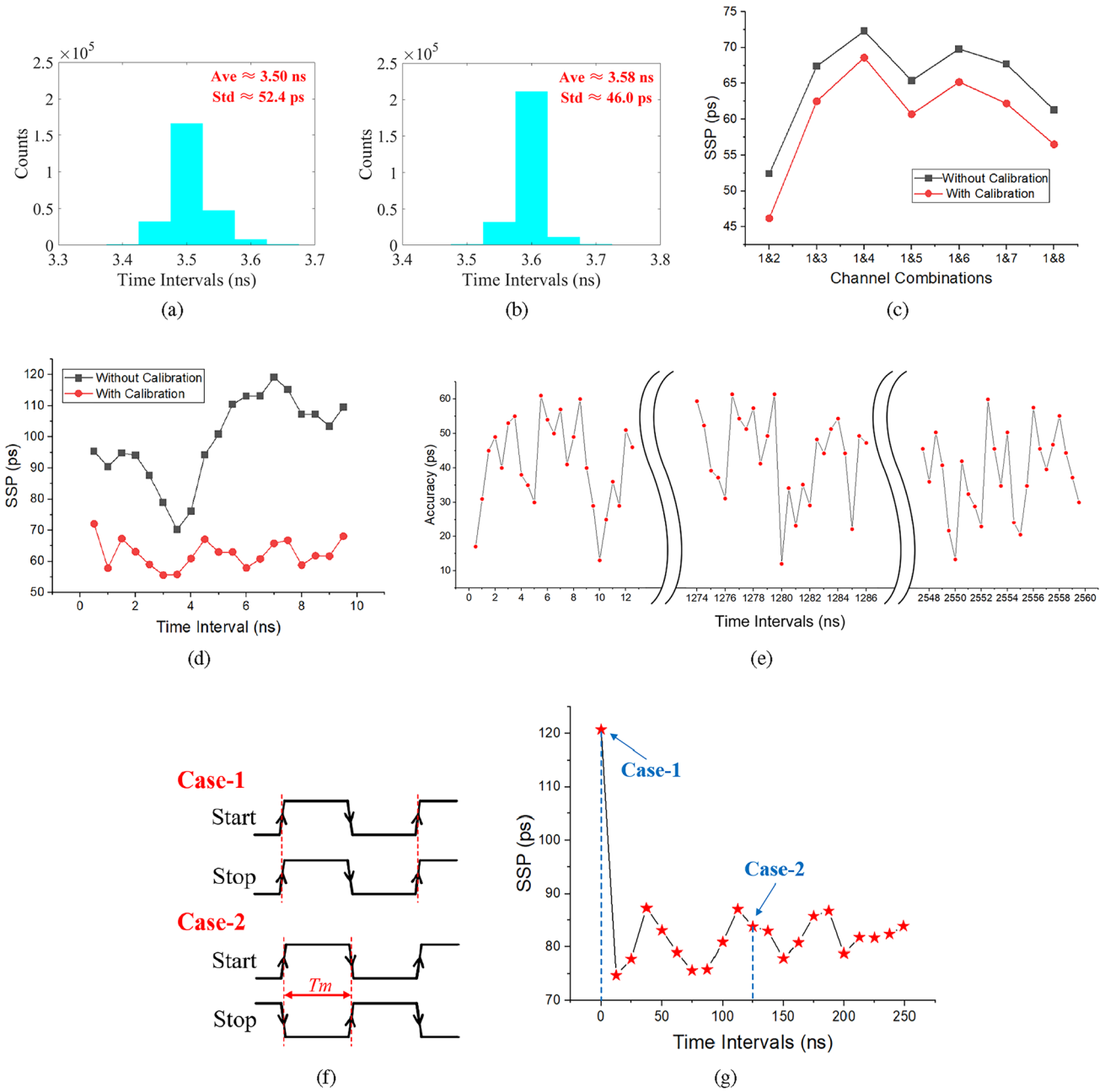

Fig. 7 (Color online) **a** Uncalibrated SSP and **b** the calibrated SSP with the combination of Ch-1 and Ch-2. **c** SSP results across seven channel combinations with cable delay measurement test. **d** SSP results along the range of (0.5-ns, 10-ns) with the combination of Ch-1 and Ch-2. **e** Tested accuracy along TDC's dynamic range with the combination of Ch-1 and Ch-2. **f** Specification of two cases of correlated cross talk between Start and Stop. **g** Measured SSP curve with time intervals within (0, 249-ns), which includes the two cases of correlated cross talk

shown in Fig. 7d, SSP results with different inputs become more consistent after calibration. As this calibration method relying on INL results is designed to compensate for nonuniform LSBs, the test results can mutually corroborate this theory. Hence, the test and calibration methods employed were proven to be correct. The accuracy represents the error between the input and output, which was also measured over the dynamic range of TDC as shown in Fig. 7e. Because the metastability was eliminated with the double-edge-triggered counter, no significant deviation in accuracy was observed in the test results.

The precision of TDC can be degraded due to the effect of cross talk, which introduces distortion of the edges of the Start or Stop signals. Both correlated and uncorrelated

Table 4 Comparison of multichannel TDCs

Parameters	Ref. [33]	Ref. [34]	Ref. [35]	Ref. [36]	Ref. [37]	Ref. [38]	Ref. [39]	This work
Process (nm)	130	350	65	110	180	28	28	180
Type	Delay line	GRO*	Vernier	Counter	VCRO*	RO	Counter	Vernier
Channels	1024	48	2	17	1024	/	64	8
Dynamic range (ns)	100	51.8	2500	3400	2100	30	/	2560
SSP (ps)	78.5	93.2	27.6	104	62.1	20	96.8	46.0
DNL/INL (LSB)	0.4/1.2	2.0/2.4	1.7/2.8	0.3/2.5	0.5/2.2	0.7/1.0	0.2/0.3	0.4/0.5
Conversion Rate (MS/s)	500	40	1	/	/	17.2	/	22.2
Power (mW)**	90	/	51.4	188.8	>1200	/	/	93.6***

* Gated ring oscillator (GRO); voltage controlled ring oscillator (VCRO)

** The power consumptions of all TDC channels are included

*** The presented power dissipation of proposed chip is obtained with the conversion rate of 4-MS/s

cross-talk mechanisms can have an effect. Uncorrelated cross talk is typically difficult to evaluate, and we focused more on correlated cross talk [32]. An experiment was conducted to study the effects of the cross talk. Two adjacent channels, Ch-1 and Ch-2, were used to obtain timestamps of the Start and Stop signals, respectively. The input pads of these two channels are close to each other so that the effect of cross talk on them can be more significant. The Start and Stop signals were both 4 MHz, and the time intervals between them (denoted as T_m) varied within (0, 249 ns). As shown in Fig. 7f, the rising edges of the Start and Stop signals were distorted by each other with $T_m = 0$, and the rising edge of Stop will be distorted by the falling edges of Start with $T_m = 125$ ns. The SSP evaluations were performed at various time intervals. Although it may be observed from Fig. 7g that the SSP with $T_m = 0$ was significantly worse than other cases, it was not significant with the case of $T_m = 125$ ns. We speculate that this may be because the effect of cross talk is greater when the rising edges of the Start and Stop are coincident. The effects of metastability can be neglected because of the asynchronous measurement mechanism and double-edge-triggered counter of this TDC, and the degradation of SSP can be explained by cross talk. Therefore, these instances with correlated cross talk should be excluded from the system's operating mode of TDC.

Table 4 shows the comparison of the proposed TDC with others [33–39], which are all suitable for multichannel applications. Compared with the delay-line structure in Ref. [33] and the counter structure in Ref. [36], the proposed TDC has a notable advantage in terms of precision. These results show that our design exhibited superior conversion linearity in contrast to the structures based on ring oscillators given in Refs. [34] and [37]. The TDC proposed by Ref. [35] is also based on a vernier controlled with dual DLLs, but it exhibited worse linearity and a slower conversion rate compared to the proposed TDC [38] and [39] provide two TDCs based on Xilinx 7-series 28 nm FPGA, and the performance of our TDC was still competitive among them.

5 Summary

The design of an 8-channel, high precision TDC ASIC for STCF EMC has been reported along with the results of an experimental evaluation. The proposed TDC is based on a 3-level Nutt structure that can reach a wide dynamic range and high resolution. The sliding-scale technique is employed with the proposed TDC, and its role in improving the conversion linearity was demonstrated. The prototype chip was implemented using a standard 180 nm CMOS process with a die area of 1.55 mm × 1.42 mm. According to the testing results, the proposed TDC features a single-shot precision of 46 ps for the best channel, DNL better than 0.4-LSB and INL better than 0.5-LSB, and good consistency among all channels was observed. Moreover, it also exhibited good consistency in performance across all TDC channels. Considering the flexible vernier-type framework employed by this chip, our next step will be to further improve the TDC's resolution and expand it to accommodate more channels. Synchronization and matching among multiple channels remains as an important direction for future work, along with the development of methods to suppress jitter and techniques to compensate for temperature.

Author contributions All authors contributed to the study conception and design. Material preparation, data collection, and analysis were performed by Zi-Wei Zhao and Ran Zheng. The first draft of the manuscript was written by Zi-Wei Zhao, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data availability The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.j00186.00828 and https://www.doi.org/10.57760/sciencedb.j00186.00828.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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