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Hardened design and practical effect of 60 V trench MOSFET resistant to irradiation

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Abstract
This study focuses on a 60 V trench MOSFET device designed for operation in space radiation environments. By increasing the bulk region concentration and placing the etched gate trench after the P+ implantation process, we successfully reduced the threshold voltage shift from 6.5 to 2.2 V under a total dose of 400 krad(Si) ^{60}Co, allowing the device to operate normally. Structurally, by embedding the source metal in the active and terminal regions, the device demonstrated current degradation without experiencing single-event burnout when subjected to a drain voltage of 60 V and a linear energy transfer value of $75.4\,\text{MeV}\cdot\text{cm}^2/\text{mg}$ from tantalum-ion incidence. TCAD simulations verified that the embedded source metal effectively suppressed parasitic transistor conduction and eliminated the base-region expansion effect, thereby lowering the maximum temperature from 8000 to 1400 K. The irradiation effects of the embedded source metal in the terminal region were also investigated, which can improve the reverse recovery and ensure that the terminal metal does not melt prematurely, thereby significantly enhancing the radiation hardness of the device.

Keywords Trench MOSFET · Single-event burnout (SEB) · Total ionizing dose (TID) · Hardened structure · Lattice temperature

1 Introduction

As power electronics become fundamental to spacecraft and military systems, the demand for electronic devices that can undergo radiation hardening under ionizing radiation has surged. MOSFETs are widely used in electronic power systems due to their high switching speed, low power consumption, and high power density [1, 2]. Compared to planar gate MOSFET structures, trench MOSFETs have a smaller device area due to the junction field-effect transistor region, which limits cell unit miniaturization [3, 4]. Trench MOSFETs have shown significant applicability in deep space exploration and spacecraft [5, 6].

For critical applications that require expansion in high-radiation environments, power MOSFETs must account for both total ionizing dose (TID) effects and single-event burnout (SEB) effects to develop devices that are more resistant to radiation impacts. TID effects refer to the process in which radiation particles traverse the oxide layer, depositing energy that generates electron–hole pairs. Some holes are trapped, creating an interface charge at the SiO_2/Si interface, which leads to a threshold voltage shift [7–10]. In addition, in space environments, the presence of high-energy neutrons, protons, and heavy ions can create high-density plasma paths within the device, altering the internal electric-field distribution and causing parasitic transistor conduction, resulting in various SEB effects that can lead to premature device failure [11–13]. Efforts to mitigate TID effects in power MOSFETs have primarily focused on reducing gate oxide traps, such as by controlling the gate oxide processing temperature [14] and increasing the hafnium oxide dielectric layer [15]. Methods to improve the SEB performance of power MOSFETs include suppressing the parasitic effects of bipolar junction

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transistors, such as extending the P+ base region [16, 17] and introducing an n-type buffer layer between the epitaxial layer and substrate to improve the electric-field distribution [18, 19]. In response to the challenges faced by 60 V trench MOSFETs in space radiation environments, we enhanced the resistance to total-dose effects through process modifications and improved the SEB capability through structural changes. Total-dose experiments revealed that increasing the bulk region concentration and adjusting the order of the gate trench etching process significantly enhanced the total-dose resistance and reduced the threshold voltage shift during the on state from 6.5 V to 2.2 V compared to traditional 60 V silicon power MOSFETs below the turn-on voltage of the hardened structure, thereby allowing the device to remain fully operational. Heavy-ion irradiation experiments demonstrated that the hardened structure only exhibited current degradation without SEB at a drain voltage of 60 V and a linear energy transfer (LET) value of $75.4\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$ from tantalum ions [20]. Utilizing the two-dimensional numerical simulator SILVACO TCAD [21], we studied how the embedded source metal allows the current generated by irradiation to be efficiently extracted without passing through parasitic transistors, thereby eliminating the base-region expansion effect and reducing the maximum temperature from 8000 K to 1400 K, thus enhancing the resistance of the device to single-event radiation. Furthermore, we verified that the embedded source metal in the terminal region led to a current concentration, resulting in temperature elevation, but remained below the melting temperature of the metal. The experimental and simulation results indicate that the 60 V radiation-hardened trench MOSFET demonstrates high operational capability in radiation environments, effectively balancing the resistance to the TID and single-event irradiation.

2 TID hardening method and experimental verification

2.1 TID mechanism and hardening process realization

Total-dose experiments were conducted at the Atomic Energy Research Institute using a ^{60}Co irradiation source with a dose rate of 200 rad (Si)/s. Each irradiation dose was 50 krad (Si) and the threshold voltage shift was tested. The schematics of the device and circuit used in these experiments are shown in Fig. 1a, where the four devices on the left are XTMT06N80D nonhardened radiation-resistant 60 V power MOSFETs, serving as controls, and the devices on the right were hardened through process modifications. The upper four devices are connected in series to a voltage source with a gate voltage of 4 V, which keeps them in the "on" state, while the lower devices have a gate voltage of 4 V, placing them in the "off" state. A total dose of 400 krad (Si) was applied during the irradiation experiments.

A schematic of the threshold voltage shift generated during the total-dose irradiation process is shown in Fig. 1b. During irradiation, radiation particles penetrate the oxide, depositing energy that generates electron–hole pairs. Within the oxide insulator, the electrons flow toward the gate, whereas the holes move toward the Si substrate. When an electric-field stress occurs across the insulator, holes are transported through the oxide, and a portion of these holes are trapped at long-term capture sites at the SiO_2 interface, resulting in a residual negative voltage shift. In addition, radiation-induced interface traps may form within the Si bandgap in an irradiated environment, causing a negative threshold voltage shift in the power MOSFET [8, 22]. This shift is more pronounced when the device is in the "on" state, both of these factors significantly impact the threshold voltage shift.

Both the interface trap charges and oxide charge traps significantly affected the threshold voltage shift. To reduce the interface trap charges, a method involving etching grooves

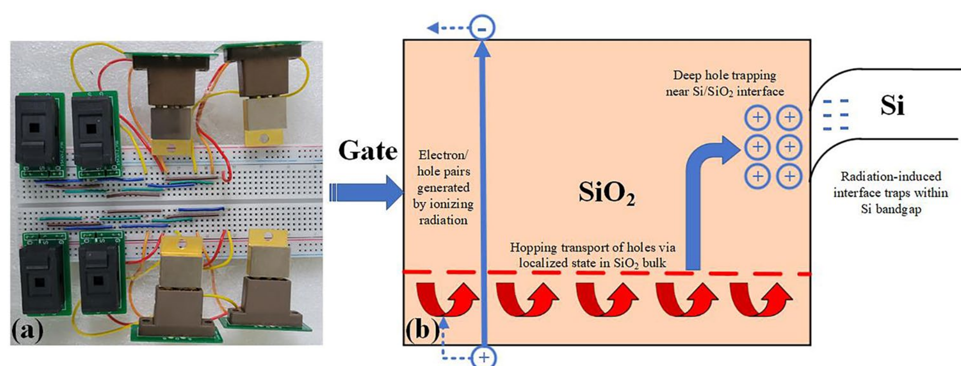

Fig. 1 (Color online) **a** Total-dose experiment circuit and test device diagram. **b** The process of total-dose-induced threshold voltage shift in an MOSFET

followed by implantation is used, along with traditional processes such as annealing in N_2 for 30 min after oxidation and low-temperature growth of gate oxides, to decrease the interface trap charge density. In addition, by introducing chlorine ions during the oxidation process to neutralize charge accumulation, the number of positive charge traps in the oxide was reduced, thereby enhancing the total-dose tolerance of the device.

Figure 2a–f shows the detailed process flow of the source area and terminal of the reinforced structure in this experiment. First, a buffer region (N-Buff) and drift region (N-Drift) were formed on the Si substrate, as shown in Fig. 2a. The construction of the buffer region was intended to mitigate the effects of heavy-particle irradiation. Low-doped p-type body region (P-body), junction termination extension (P-JTE), and field ring termination (P-ER) are formed through ion implantation, as shown in Fig. 2b. The source metal region was etched within the body region, and ion implantation was conducted to form the source region (N+) and the p-type shielding region (P+). A high concentration of body-region doping and a low concentration of channel-region doping are formed through the lateral diffusion of the P+ region, which enhances the radiation tolerance without affecting its conduction characteristics, as shown in Fig. 2c. Because each ion-implantation step requires high-temperature annealing, the traditional approach of etching the gate trench structure before annealing can lead to an increase in defects [23]. Subsequently, as shown in Fig. 2d and e, the gate trench is etched, and then high-pressure thermal oxidation is performed at a growth temperature of 900° to form the gate oxide layer. During the oxidation process, the introduction of chlorine ions neutralizes charge accumulation, reduces positive charge traps in the oxide, and absorbs and extracts various metal impurities from the silicon [14]. After oxidation, the structure was annealed in a N_2 atmosphere at 450° for 30 min to significantly reduce interface defects, followed by filling with polycrystalline silicon. Finally, the etched trench requires additional etching processes due to the epitaxial growth of the oxide, compared with traditional non-embedded source metal structures, the process complexity is improved, but the TID sensitivity of the device is also greatly improved, and metal is deposited to form electrodes.

2.1.1 TID experiment results

The results of the total-dose irradiation experiments are shown in Fig. 3. The vertical axis represents the change in the threshold voltage under irradiation relative to the threshold voltage of the device in the non-irradiated state. The increase in P-body doping led to a higher threshold voltage for the hardened device in the non-irradiated state compared to that of the original device, whereas the change in threshold voltage more directly reflected the variations introduced by the gate oxidation process. The threshold voltage drift for

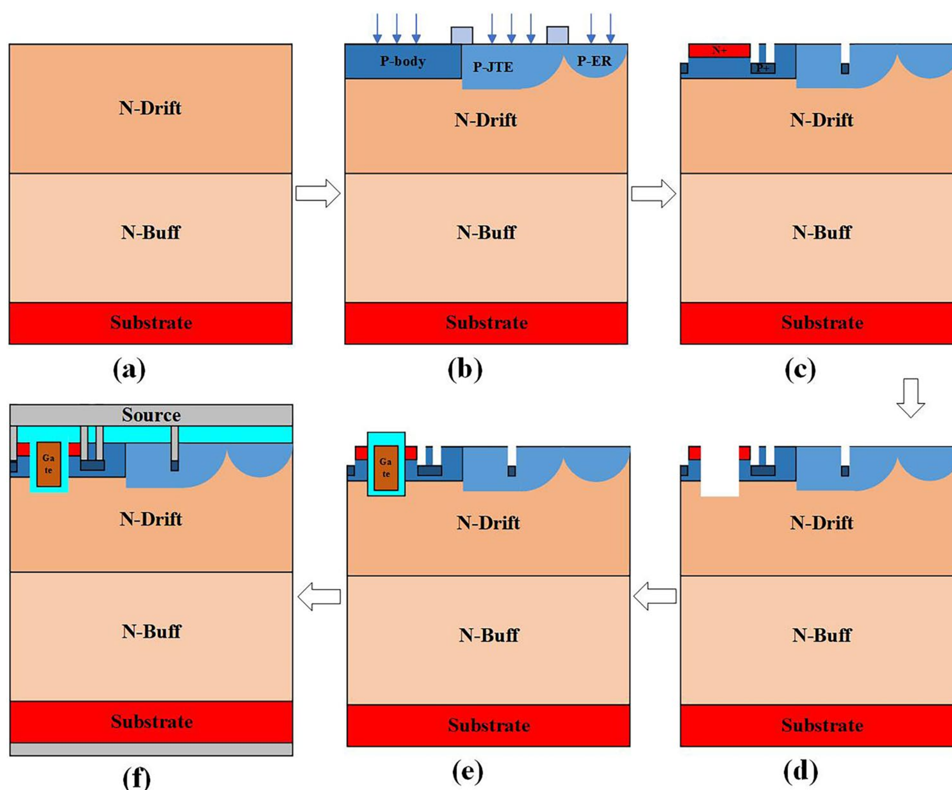

Fig. 2 (Color online) Manufacturing process of the 60 V radiation-hardened trench MOSFET

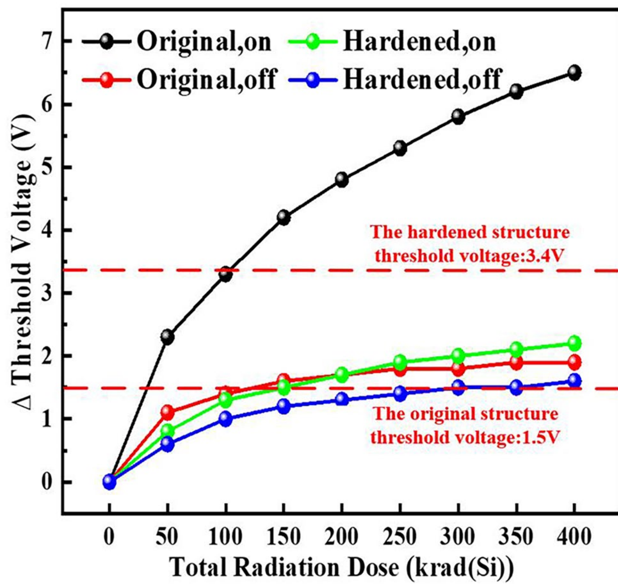

Fig. 3 (Color online) Impact of total-dose irradiation on the threshold voltage shift of XTMT06N80D device and the 60 V radiation-hardened trench MOSFET device

both devices in the "on" state is greater than that in the "off" state [24, 25]. Regardless of whether tested in the "on" or "off" state, the threshold voltage shift for the XTMT06N80D devices is higher than that for the 60 V radiation-hardened trench MOSFET structure that has been improved through our process. In addition, Ref. [26] reported that the threshold voltage shift of split-gate trench VDMOS devices at a total dose of 150 krad (Si) was 7.2 V, with a shift of approximately SI1.5 V in the off-state. Reference [27] stated that the threshold voltage of radiation-hardened IRH-254 power MOSFETs showed a positive shift of 1.8 V at a total dose of 100 krad (Si). Both these values are higher than those of the hardened structure proposed in this study, with a positive gate bias and a total dose of 400 krad (Si), and the threshold voltage drift for the hardened structure is 2.2 V, which is significantly less than the device's designed turn-on voltage of 3.4 V. This indicates that the hardened 60 V MOSFET structure retains good performance under total-dose irradiation conditions.

3 SEB experiment test and simulation analysis

3.1 SEB experiment results

The continuous heavy-ion irradiation experiments were conducted at the Lanzhou Institute of Modern Physics [28]. The irradiation source consisted of tantalum ions with a flux of 1×10^4 ions/(cm$^2 \cdot$ s), a total fluence of 1×10^6 ions/cm^2, and a LET value of 75.4 MeV $\cdot$ cm^2/mg in the normal direction. The reverse leakage current (I_{DS}) and gate current (I_{GS}) of the 60 V-radiation-hardened trench MOSFETs were measured under different V_{DS} irradiation conditions using a QTSA1501A-1 M instrument, as shown in Fig. 4a. To make the heavy-particle experiment more effective, a 60 V radiation-hardened trench MOSFET was decapsulated before the experiment. To ensure that the TCAD modeling aligns with the actual production structure, a cross-sectional analysis of the source and terminal regions of the radiation-hardened structure was performed, as depicted in Fig. 4b. The basic structure was consistent with that shown in Fig. 2. In addition, to differentiate between the buffer and drift regions, a staining treatment was applied, as illustrated in Fig. 4c. Traditional silicon dioxide is used as the gate oxide material. The other device structural parameters are listed in Table 1.

Figure 5 shows the I_{DS} and I_{GS} curves under heavy-ion irradiation for both the original 60 V trench MOSFET device and the 60 V radiation-hardened trench MOSFET devices at different drain-source voltages V_{DS}. The irradiation curves of the original 60 V trench MOSFET device are shown in

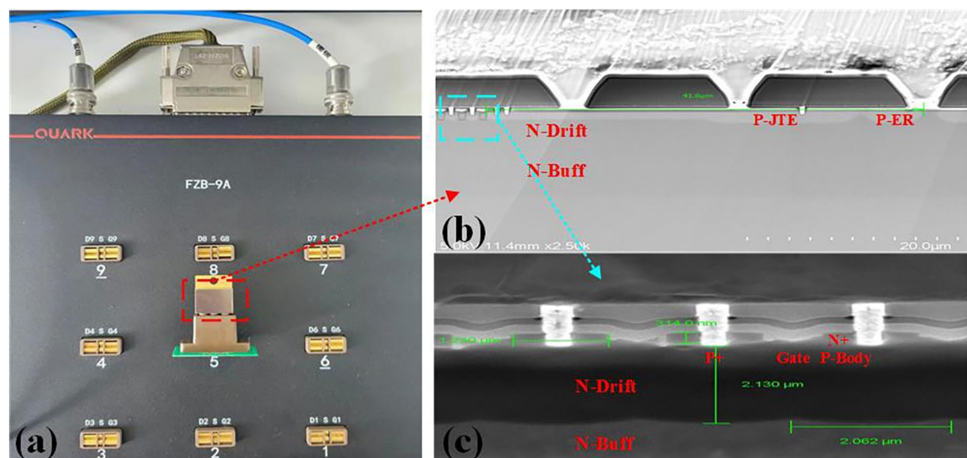

Fig. 4 (Color online) Schematic diagram of the heavy-ion irradiation experiment test board of the 60 V radiation-hardened trench MOSFET device (**a**), cross-sectional structure diagram (**b**), and stained structure diagram (**c**)

Table 1 Device structure size

Structure name	Structural parameter
Chip size (mm×mm)	5.9×4.9
Cell width (μm)	2
Groove depth (μm)	1.28
Channel gate oxygen thickness (nm)	79.4
Channel length (μm)	7
Source metal length (μm)	1.05
Source metal width (μm)	0.403

Fig. 5a and b. At $V_{DS} = 40$ V and 50 V, the drain current has already experienced degradation, and the gate current is also high. At this point, the device suffers from gate and drain degradation owing to the high temperatures. When $V_{DS} = 60$ V, both the drain and gate currents increase uncontrollably and rapidly reach the limit current set to protect the circuit, indicating a severe SEB within the device and resulting in damage. Figure 5c and d presents the irradiation results for the 60 V radiation-hardened trench MOSFET device. This indicates that when V_{DS} is less than 60 V, both the drain and gate currents exhibit slight increases during irradiation. This is attributed to the continuous tantalum ion beam generating electron–hole pairs within the device, which are subsequently expelled from the drain and gate. These changes were reversible and had minimal impact on the device. However, at $V_{DS} = 60$ V, both the drain and gate currents decreased, and the gate current changed more significantly. This degradation is due to prolonged high temperatures that cause gate degradation [29]. Notably, neither current exhibited a rapid increase, suggesting that no SEB occurred within the silicon device and that no single-event gate rupture occurred owing to the increased electric fields.

In addition, Ref. [30] presents the relationship between the failure voltage and the breakdown voltage for over 20 MOSFET devices operating within a range of 20 V to 100 V. Thus, the SEB threshold is concentrated between 0.2 and 0.6 for the breakdown voltage. However, the hardened structure proposed in this study increases this value to 1. The experimental results demonstrate that the 60 V radiation-hardened trench MOSFET device exhibits superior resilience to heavy-ion irradiation under a rated breakdown-voltage operating environment owing to its structural reinforcement.

3.1.1 SEB simulation setup

Using the two-dimensional simulation tool Silvaco ATLAS, the SEB performance of the reinforced structure was analyzed. During heavy-particle incidence, numerous incident positions [31, 32] are possible; however, the current research

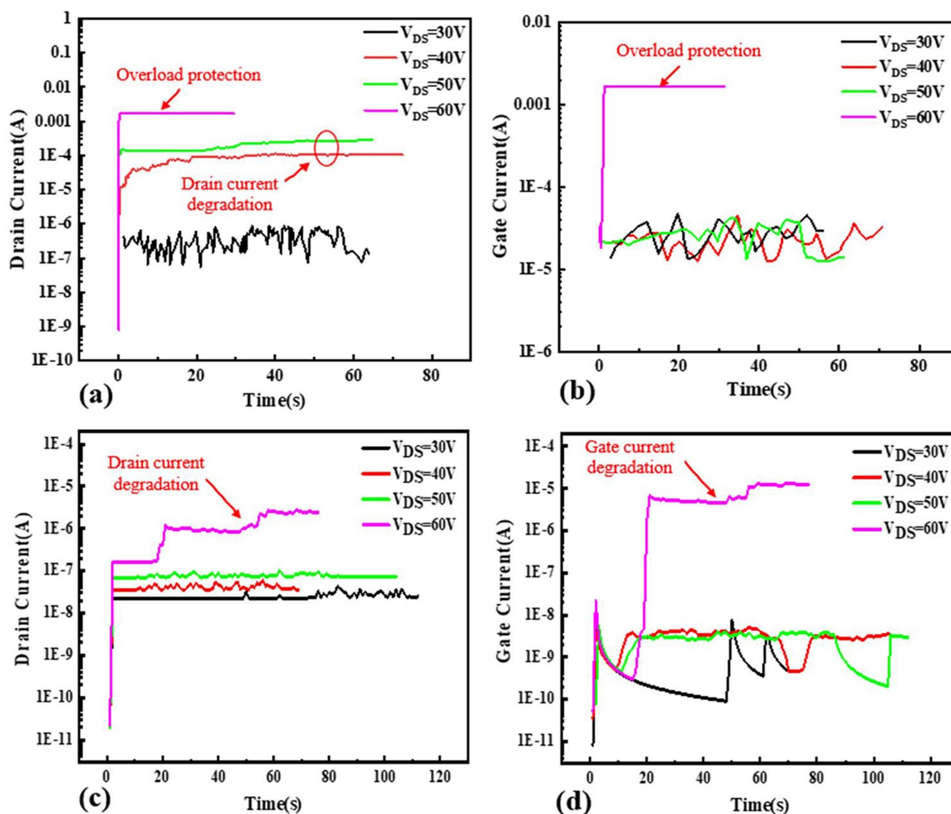

Fig. 5 (Color online) Current degradation curves of the original 60 V trench MOSFET (**a**, **b**) and the 60 V radiation-hardened trench MOSFET (**c**, **d**) in heavy-particle irradiation experiments

primarily focuses on source–region position analysis. This simulation analysis included a terminal position analysis; the detailed structures are shown in Fig. 6. Figure 6a shows the original 60 V device structure, where the reinforced structure incorporates an embedded source metal at both the source and terminal regions, as shown in Fig. 6b). This design aims to utilize the source metal to absorb holes generated during irradiation, thereby suppressing parasitic transistor conduction and reducing the device temperature, while not compromising the device's TID capacity in the manufacturing process. The size of the reinforced structure adopted in the simulation was strictly in accordance with the results presented in this section.

Figure 7 shows the experimental and simulation results of the conduction and transfer characteristics of the hardened structure. Owing to the limitations of the testing equipment, the test current was maintained at a low value to prevent device damage due to overheating. The results demonstrated a strong consistency between the simulation and experimental data. In addition, through testing and calculations, the specific on-resistance of the hardened device at gate voltages of 5 V and 10 V is $1.76\,\mathrm{m\Omega \cdot cm^2}$ and $1.50\,\mathrm{m\Omega \cdot cm^2}$, respectively, which represents an increase of 17% and 3% compared to the commercial device. Because the lateral diffusion of the P+ region has a minimal impact on the channel-region concentration, the overall trade-off is minimal. Figure 8 shows the breakdown characteristics of the devices under high-voltage stress for the unterminal, original, and hardened structures. The original 60 V trench MOSFET structure and the hardened structure exhibited similar breakdown voltages. In comparison, Fig. 8a shows that the absence of a terminal structure causes the electric field to concentrate at the junction between the P-body and the drift regions, leading to a rapid increase in the electric field at this location. Consequently, the breakdown voltage was reduced by approximately 30 V. This highlights the importance of discussing the terminal designs of critical device components in the context of SEB.

Various physical models were employed to predict the electrical characteristics of the device during SEB simulations, including the concentration-dependent mobility (CONMOB) model and the parallel electric-field-dependent mobility (FLDMOB) model. Additionally, the collision ionization model (Overstraeten–de Man) [33] and temperature-dependent thermal model (late.temp) [34, 35] were considered because SEB processes involve the generation of electron–hole pairs via collision ionization. The normal incidence LET value for tantalum ions is $75.4\,\mathrm{MeV \cdot cm^2/mg}$, which corresponds to an LET value of $0.785\,\mathrm{pC/\mu m}$ when simulating Si materials, as calculated using Eq. (1), where $E_{\mathrm{e-h}}$ represents the energy required to generate a pair of electron–hole pairs in the material and ρ represents the material density.

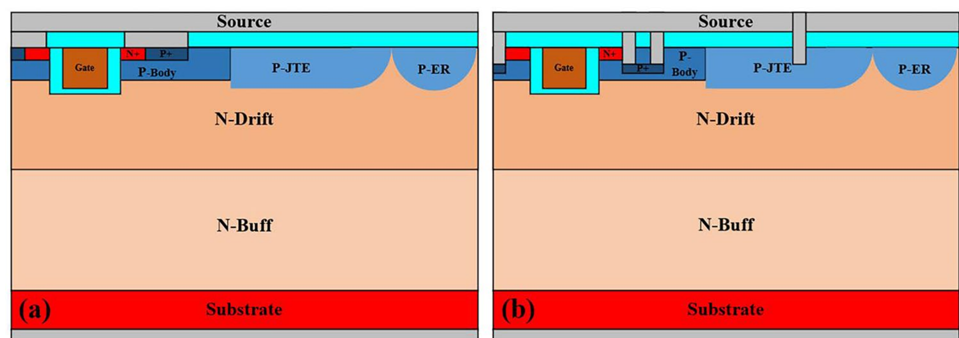

Fig. 6 (Color online) Schematic diagrams of **a** original 60 V trench MOSFET device and **b** 60 V radiation-hardened trench MOSFET device

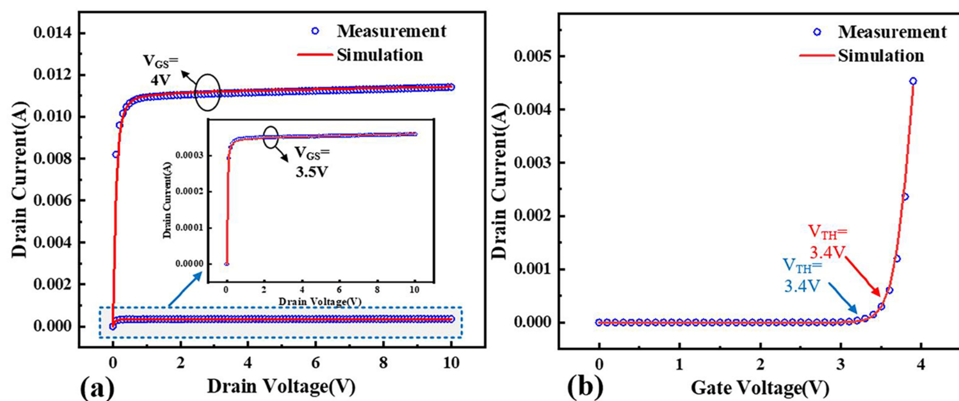

Fig. 7 (Color online) Simulation and test results of the conducting characteristics (**a**) and transfer characteristics (**b**) of the 60 V radiation-hardened trench MOSFET device

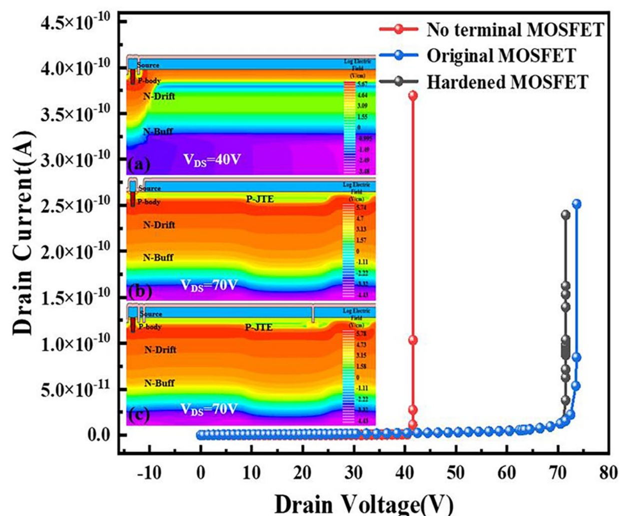

Fig. 8 (Color online) Breakdown characteristics of different structures. Electric-field distribution: **a** MOSFET without termination structure at $V_{DS} = 40\,\text{V}$; **b** original 60 V trench MOSFET device at $V_{DS} = 70\,\text{V}$; **c** 60 V radiation-hardened trench MOSFET device at $V_{DS} = 70\,\text{V}$

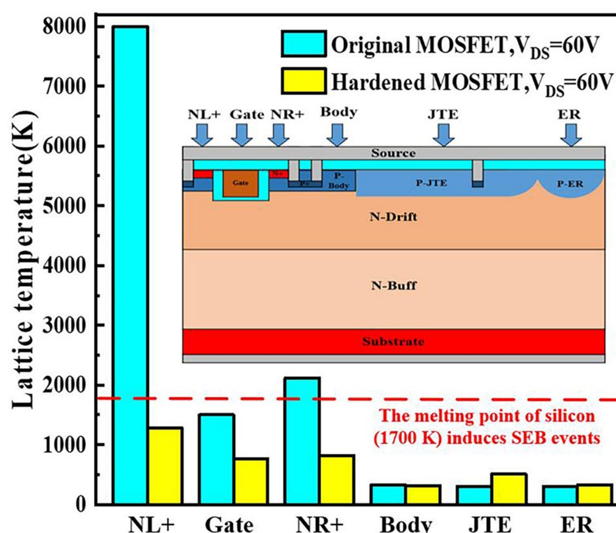

Fig. 9 (Color online) Lattice temperatures of the 60 V radiation-hardened trench MOSFET device and the original 60 V trench MOSFET device under different ion impact positions at $V_{DS} = 60\,\text{V}$

$$1\,\text{pC}/\mu\text{m} = E_{\text{e-h}}/(\rho q)\,\text{MeV}\cdot\text{cm}^2/\text{mg} = 96\,\text{MeV}\cdot\text{cm}^2/\text{mg}. \quad (1)$$

3.1.2 SEB simulation analysis

In TCAD Silvaco, the lattice temperature is typically calculated by solving the thermal transport equation, which is closely related to the thermal behavior of semiconductor devices, as shown in Eq. (2).

$$\frac{\partial T_{\text{lattice}}}{\partial t} = \nabla \cdot (k(t)T_{\text{lattice}}) + Q_{\text{source}}. \quad (2)$$

Here, T_{lattice} represents the lattice temperature (in Kelvin), k is the temperature-dependent thermal conductivity (in $\text{W}/(\text{m}\cdot\text{K})$), and Q_{source} is the heat source term, which typically includes heat transport by charge carriers, heat injection, and external heat sources (e.g., heating caused by the injected current). In the case of single-particle incident processes, the heat source term primarily corresponds to carrier heating. Heavy-ion bombardment generates numerous charge carriers in the device. As the current density increases, the carriers (typically electrons) inside the device carry more energy. When current flows through a semiconductor, the charge carriers interact with the lattice, particularly through carrier-phonon scattering. This scattering transfers the kinetic energy of the carriers to the lattice, causing the lattice vibrations (i.e., temperature) to increase.

To investigate the vulnerabilities of SEB injection in 60 V MOSFET devices, we selected seven different injection locations: left source, gate, right source, body, JTE terminal, and ER terminal regions. The breakdown thresholds of the original 60 V MOSFET and hardened radiation-resistant trench MOSFETs at a drain voltage of 60 V are shown in Fig. 9. As shown in the figure, during injection into the source region, the hardened structure suppresses the conduction of parasitic transistors, reduces the current density, and significantly lowers the internal lattice temperature, keeping it below the melting point of silicon. This corresponds to the absence of SEB phenomenon during the experimental process. However, for injections in the end regions (JTE and ER), the temperature in the hardened structure exceeded that in the original structure, requiring a detailed analysis of these two phenomena.

Figure 10 shows the variation in lattice temperature over time when the original 60 V MOSFET and hardened radiation-resistant trench MOSFET were incident from the left source region. Evidently, as the drain-source voltage (V_{DS}) increases, the maximum lattice temperature of the hardened radiation-resistant trench MOSFET rises, reaching 1260 K at $V_{DS} = 60\,\text{V}$, which has not yet reached the melting point of silicon devices, thus no SEB phenomenon is observed. However, prolonged exposure to high temperatures can lead to gate degradation, whereas the original trench MOSFET structure exhibits uncontrolled temperature behavior. As shown in Fig. 10a, the highest temperature in the hardened structure occurs at the interface between the drift and body regions, whereas in the

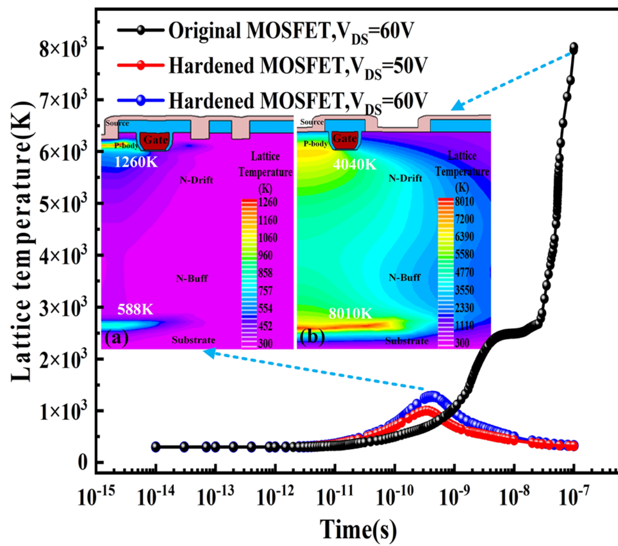

Fig. 10 (Color online) Hardened radiation-resistant trench MOSFET device and the original 60 V trench MOSFET device after a heavy ion hits the left source region when V_{DS} = 50 V and 60 V. Lattice temperature distributions: **a** 60 V radiation-hardened trench MOSFET device; **b** original 60 V trench MOSFET device

un-hardened structure, it occurs at the interface between the substrate and drift regions, as illustrated in Fig. 10b.

To analyze the different reasons for the temperature variations in the two types of devices, we present the current distributions of both structures in Fig. 11. The hardened radiation-resistant trench MOSFET allows the current to flow directly from the P-body region to the source owing to the embedded source metal, whereas in the original structure, the current can only flow through the body region to the source. This results in a reduction of the body-region concentration from 4.3×10^6 A/cm^2 to 8.5×10^5 A/cm^2 in the hardened structure compared to the original structure. The decrease in current significantly suppresses the conduction of the parasitic transistor formed by the source-body-drift (NPN) configuration and mitigates the electric field changes caused by the base-region extension effect.

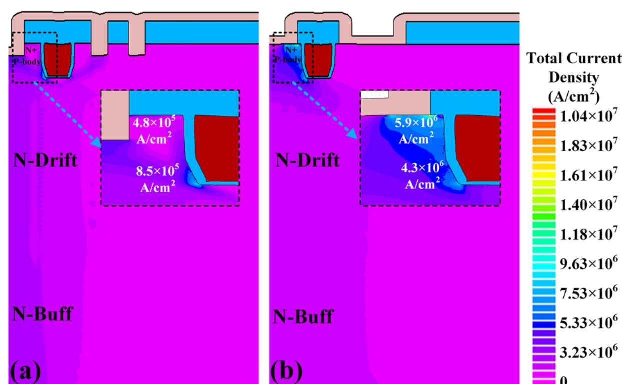

Fig. 11 (Color online) Total current densities of the 60 V radiation-hardened trench MOSFET device (**a**) and the original 60 V trench MOSFET device (**b**) after a heavy ion hits the left source region at V_{DS}= 60 V

Figure 12 shows the electric-field variation curve along the incident position from the source to the substrate. In the original structure, the conduction of the parasitic transistor leads to an extension effect, causing a sharp increase in the electric field at the interface between the drift region and substrate [36]. As the collision ionization rate increases, the device experiences avalanche breakdown, continuously generating electron–hole pairs, which results in the simultaneous presence of high electric fields and high currents within the device, leading to a temperature avalanche. In contrast, the hardened structure, owing to rapid current evacuation, suppresses the base-region extension effect, leading to a reduction in the electric field at the drift-substrate interface from 2.1×10^6 V/cm to 3.1×10^5 V/cm, allowing the temperature to decrease appropriately. The variations in incident temperature at other source region locations followed a process similar to that described above. The source metal extracts the current, suppressing the conduction of parasitic transistors, and leading to a decrease in temperature.

In practical heavy-particle irradiation experiments, the incident position is uncontrollable. The terminal, which is a critical component of the device, is highly likely to be affected by particles; however, very few studies have

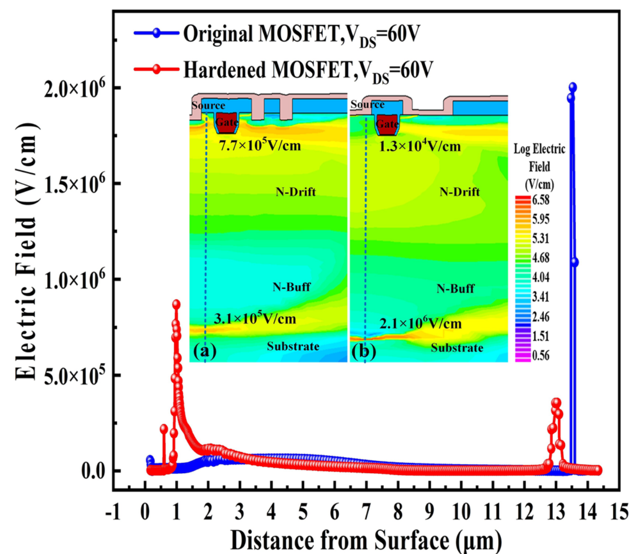

Fig. 12 (Color online) Electric-field change curves of the 60 V radiation-hardened trench MOSFET device (**a**) and the original 60 V trench MOSFET device (**b**) after a heavy ion hits the left source region at V_{DS} = 60 V. Electric-field distributions: **a** 60 V radiation-hardened trench MOSFET device; **b** original 60 V trench MOSFET device

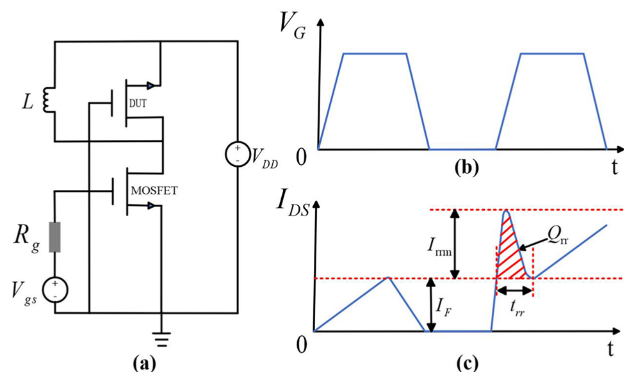

Fig. 13 (Color online) Reverse recovery characteristic test. **a** Simulated circuit. **b** Gate drive voltage. **c** Drain-source current output

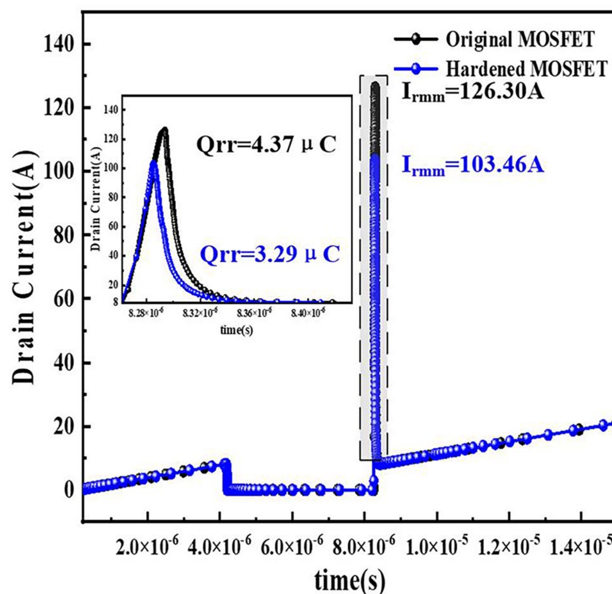

Fig. 14 (Color online) Reverse recovery characteristics of a 60 V hardened radiation-hardened trench MOSFET device and an original trench MOSFET device

specifically addressed this aspect. In the terminal region, the embedded source metal can also extract current from the source region and suppress the parasitic transistor triggering. However, this structure can enhance the reverse recovery characteristics of the body diode.

However, this structure can enhance the reverse recovery characteristics of the body diode. Circuit simulation was performed using the circuit shown in Fig. 13. In this circuit, the MOSFET acts as a switch. When the gate voltage (V_G) is high, the body diode in the device under test is reverse-biased, and the current flowing out of V_{DD} can only pass through the parallel inductor, during which V_{DD} is charged. When V_G is switched to a low level, the lower transistor is turned off. Because the current in the inductor cannot change suddenly, it can only flow through the inductor and form a loop with the device under testing, while maintaining a constant current (I_F). When the switch was turned on again, the body diode transitioned from forward to reverse blocking. During the forward conduction process, a large number of charge carriers accumulate in the drift region. When the diode is suddenly turned off, these carriers must be swept out of the depletion region, leading to significant reverse current (I_{rmm}) and reverse recovery current (t_{rr}) through the MOSFET. The areas enclosed by I_{DS} and I_F define the reverse charge recovery (Q_{rr}).

The simulation results are shown in Fig. 14 indicate that for a 60 V radiation-hardened trench MOSFET, the reverse recovery current is 103.46 A, the reverse recovery time is 0.149 μs, and the reverse recovery charge is 3.29 μC. Owing to the embedded source metal in the terminal region of the radiation-hardened structure, which causes the device to have an additional body diode, the reinforced structure reduces the reverse recovery current by approximately 18.1% and the reverse recovery charge by approximately 24.7%, thereby improving the reverse recovery characteristics.

Figure 15 shows the influence of the source metal embedded on the lattice temperature of the JTE terminal region when incident. Simulation results showed that the lattice temperature of the hardened structure was higher than that of the original structure. This is due to the terminal structure of the embedded source metal, which leads to an excessive current concentration. The current density increases from 7.7×10^3 A/cm^2 to 4.6×10^6 A/cm^2. This results in a relative increase in temperature. However, because the melting point of aluminum, the source metal, is 930 K [37], the temperature of 490 K does not cause the source metal in the terminal region to melt. Owing to the narrow junction current channel between the JTE terminal region and the field ring terminal region, the lattice temperature of the hardened device increases from 305 K to 329 K when incident from the ER region, which is similar to the incident from the JTE region. However, this temperature increase is very small and has little impact on the device. Therefore, the simulation analyses indicate that embedding the source metal in the terminal position did not lead to premature burnout in that area.

4 Summary

This study investigated the improvement of radiation hardening in 60 V trench MOSFET devices through enhancements in both the process and structure to achieve better radiation resistance. TID experiments demonstrated that under a total dose of 400 krad (Si) from ^{60}Co irradiation, the threshold voltage shift of the hardened devices decreased from 6.5 to 2.2 V compared to the nonhardened

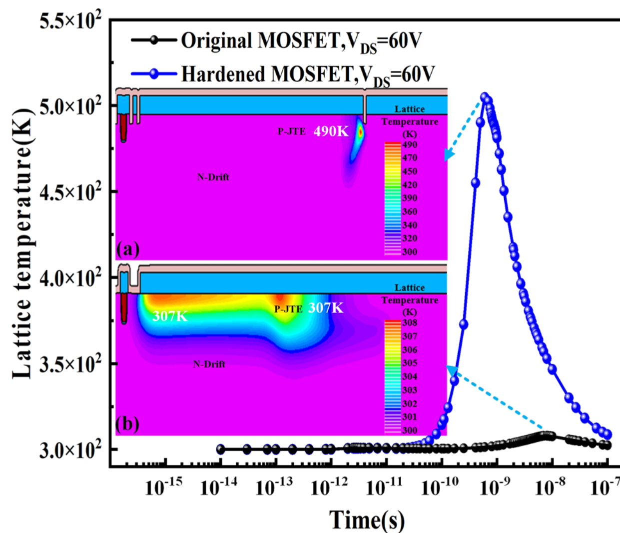

Fig. 15 (Color online) SEB responses of the 60 V radiation-hardened trench MOSFET device and the original 60 V trench MOSFET device after a heavy ion hits the JTE termination region at $V_{DS} = 60\,V$. Lattice temperature distributions: **a** 60 V radiation-hardened trench MOSFET device; **b** original 60 V trench MOSFET device

devices, while still maintaining normal turn-off capability. SEB experiments indicated that when subjected to a drain voltage of 60 V and an LET value of $75.4\,MeV \cdot cm^2/mg$ from tantalum-ion incidence, the devices exhibited only current degradation without experiencing any SEB. TCAD simulations corroborated these findings, revealing that the embedded source metal effectively suppressed the conduction of parasitic transistors, significantly reducing the temperature of the device during irradiation, while also ensuring that the terminal metal did not melt prematurely. The experimental and simulation results indicate that hardened radiation-resistant 60 V trench MOSFET devices can maintain reliable operation in high-radiation environments.

Author Contributions All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by De-Xin Chen, Ying Wang, Huo-Lin Huang, Yan-Xing Song, Meng-Tian Bao and Fei Cao. The first draft of the manuscript was written by De-Xin Chen, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data Availability The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.j00186.00905 and https://www.doi.org/10.57760/sciencedb.j00186.00905.

Declarations

Conflict of interest The authors declare that they have no Conflict of interest.

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