



# Quantitative investigation of well contact impact on single-event transient in sub-20 nm FinFET process

Qian Sun<sup>1,2</sup> · Bin Liang<sup>1,2</sup> · Ya-Qing Chi<sup>1,2</sup> · Ming Tao<sup>3</sup> · Zhen-Yu Wu<sup>1,2</sup> · Hong-Xia Guo<sup>4</sup> · Wang-Yong Chen<sup>5</sup> · Jian-Jun Chen<sup>1,2</sup> · Peng-Cheng Huang<sup>1,2</sup> · Deng Luo<sup>1,2</sup> · Han-Han Sun<sup>1,2</sup> · Ya-Hao Fang<sup>1,2</sup> · Yu-Lin Gao<sup>1,2</sup> · Ming-Yan Ma<sup>1,2</sup> · Yang Guo<sup>1,2</sup>

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## Abstract

This paper quantitatively discusses the influence of well contact on single-event transient (SET) in sub-20 nm FinFET by two-photon absorption (TPA) pulse laser. Two groups of inverter chains were designed to investigate the impact of well contact distance on the FinFET process. The experimental results show that the SET pulse width has a bimodal symmetric distribution, which is different from that of a bulk planar CMOS device. To investigate the detailed mechanism of the phenomenon, a high-precision FinFET TCAD model was established, in which both Id-Vd and Id-Vg errors were less than 10% compared to the SPICE model provided by the commercial process. TCAD simulation under heavy ion injection showed the mechanism of the abnormal phenomenon, where the well contact plays a major role in charge collection at the near-well contact distance, while the source plays a major role at the far distance. This phenomenon is completely different from that of planar CMOS devices. This indicates that the SET mechanism becomes more complicated during the FinFET process. Therefore, more effective SET hardening methods should be investigated for FinFET.

**Keywords** FinFET · Single-event transient (SET) · Well contact distance · Pulse laser

## 1 Introduction

Integrated circuits (ICs) are essential for satellites and spaceships in the cosmos, which are crucial for the exploration of the universe. The performance and reliability of IC decide the range and ability of human cosmos ambition. With the shrinking size of silicon devices for more powerful performance and smaller area requirements, the short-channel effect (SCE) [1, 2], drain-induced barrier lowering (DIBL) [3, 4], and hot carrier injection (HCI) [5–7] effects have become major barriers that inhibit the characteristic size shrinking of traditional bulk planar CMOS devices [8]. To solve these problems, FinFET, which is a three-dimensional device structure, has been demonstrated and become the mainstream advanced IC manufacturing process [9]. Compared to the bulk planar CMOS device, FinFET devices are three-dimensional with a thin body for higher gate control ability. This means that FinFET has different features under radiation compared with bulk planar CMOS. Investigating the radiation mechanism of FinFET is important for high-performance IC applications in the universe.

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✉ Bin Liang  
liangbin110@126.com

✉ Yang Guo  
guoyang@nudt.edu.cn

<sup>1</sup> College of Computer Science and Technology, National University of Defense Technology, Changsha 410073, China

<sup>2</sup> Key Laboratory of Advanced Microprocessor Chips and Systems, College of Computer Science and Technology, National University of Defense Technology, Changsha 410073, China

<sup>3</sup> College of Electrical and Information Engineering, Hunan University, Changsha 410082, China

<sup>4</sup> School of Material Science and Engineering, Xiangtan University, Xiangtan 411105, China

<sup>5</sup> School of Microelectronics Science and Technology, Sun Yat-sen University, Guangzhou 510275, China

Single-event transient (SET) is a critical reliability factor for the space application of IC. A SET is generated when an energetic particle is injected into the active device. The injected particle ionizes a number of electron–hole pairs toward the path of particle movement. The source and drain collect the ionized charges, leading to potential fluctuations in the electrode. SET is shown as the pulses in voltage and current. Such pulses seriously hamper the reliability of the IC in a space environment, leading to state machine errors, incorrect outputs, and even functional interrupts or failures [10]. Thus, investigating the SET of FinFET devices and circuitry is essential.

Well contact is the power or ground connection point of N-well and P-well, as illustrated in Fig. 1. The influence of well contact on SET has been widely investigated in planar CMOS [11–15]. Several SET hardening techniques have been proposed based on the well contact structure. Amusan et al. pointed out that shorter N-well contact locations and larger contact areas could reduce the PMOS SET pulse width in combinational circuits [16]. Narasimham et al. investigated the radiation hardening method by which a guard-ring can shrink the SET pulse width to mitigate the influence of SET in NMOS and PMOS in the 130-nm process [17]. Ahlbin et al. investigated the impact of the N-well contact area ratio on SET in 90-nm CMOS. The experimental results showed that a larger n-well contact area can lead to lower SET cross-sections and pulse widths owing to the inhibition of bipolar amplification in PMOS [18]. Therefore, the traditional method indicates that closer well contact means shorter SET pulse width. However, FinFET devices differ from planar CMOS devices in terms of geometry, shallow trench isolation (STI) depth, and well doping concentration. Thus, further investigations into the influence of SET on FinFET are required.

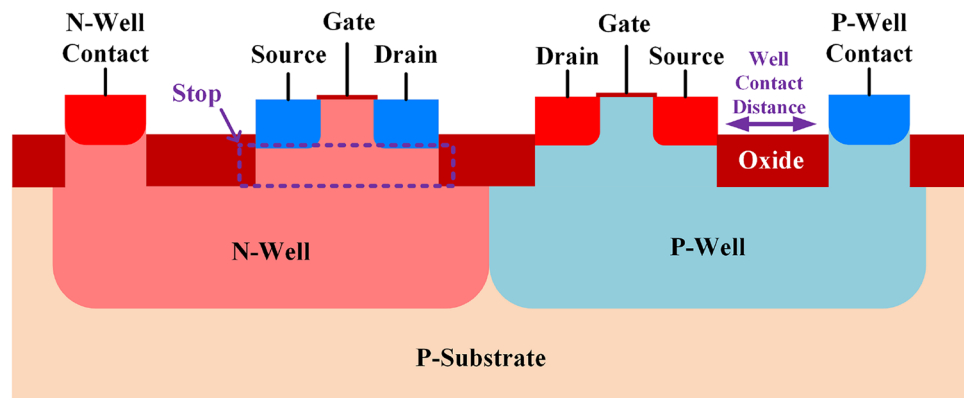
The pulsed laser is a typical investigation approach for single-event effect (SEE) [19]. It is widely used to investigate SET [20–25], single-event upset (SEU) [26–29], and single-event latchup (SEL) [30–35]. Pulsed laser testing is divided into two categories: single-photon absorption

(SPA) [36] and two-photon absorption (TPA) [37], which depend on the electron and hole generation mechanisms. SPA generates electron–hole pairs through photons with energy above the bandgap, while TPA is generated by photons whose energy is sub-bandgap. Photon absorption by semiconductors induces electron–hole pairs at the laser spot, which is similar to energetic particle injection in silicon devices. Thus, pulsed lasers can be used for SEE investigation. Meanwhile, the pulsed laser can shoot a specific position on the die by moving the design under test (DUT) or laser beam at multiple levels of energy to locate the sensitive area precisely and conveniently. Therefore, the pulsed laser is an important quantitative investigation approach for SEE, which addresses the deficiencies of heavy ion experiments.

Several investigations have focused on the influence of well contact on SET in FinFET. Zhang et al. and Xu et al. designed DFF test circuitry with dual and triple wells in 16-nm and 7-nm FinFET nodes, respectively. The experiments showed insignificant differences in the SEU cross-section between dual and triple well structures [38]. The triple well showed a higher SET sensitivity than the dual well in 7-nm FinFET [39]. Calomarde et al. investigated the impact of well depth on Static Random-Access Memory (SRAM) in 22-nm bulk-FinFET. Simulation results showed that a lower well depth can lead to a lower SET without SRAM performance variation [40]. Previous studies showed an uncertain trend in the well impact of SET in FinFET [38–41]. However, distinguishing the impact of well contact distance on SET would influence the radiation hardening method in FinFET. There is an urgent need for emergency research on SEE, the results of which could determine the feasibility of the traditional hardening method. Thus, it is essential to investigate the impact of well contact distance on SET in FinFET.

This study discovered a new phenomenon in FinFET: the maximum SET pulse width occurs at the midpoint as the well contact distance increases. First, we designed a SET capture and measurement test chip to investigate the relationship between well contact distance and SET pulse width

**Fig. 1** (Color online) The well and its contact structures in the FinFET process

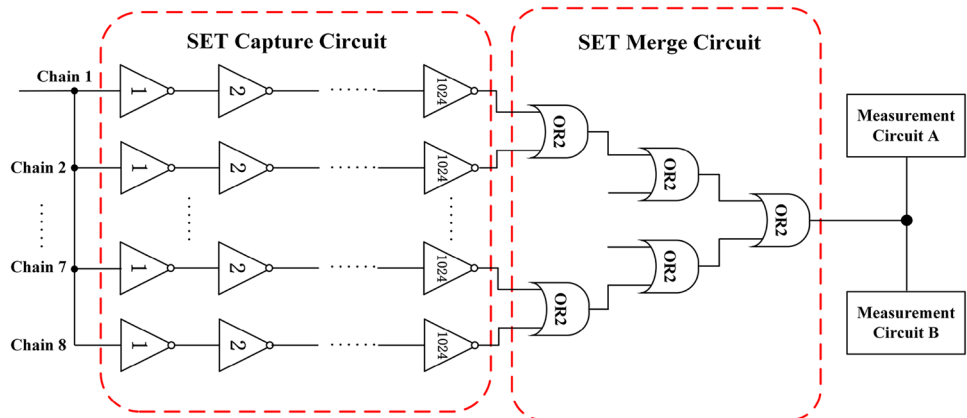


in the sub-20 nm FinFET process. A pulsed laser experiment was conducted to measure the SET generated at different well contact distances. The results show that the peak SET pulse width occurs at the midpoint of the mirror side in the FinFET, which differs from the phenomenon in bulk planar CMOS. Second, we established a high-precision inverter TCAD model to investigate the mechanism of the abnormal connection between well contact distance and SET pulse width in FinFET. Third, after comprehensive simulations and inference, the mechanism of the abnormal phenomenon was uncovered. The well contact and source play major charge collection roles at the near- and far-well contact distances, respectively. The SET pulse width increases as the well contact distance increases when the well contact collects the most charges, while it decreases when the source is the major charge collection factor. The peak SET pulse width at the midpoint affects the threshold position. Finally, we concluded that this phenomenon affects the hardening method, and the SET hardening methodology fitted to the FinFET process should be investigated.

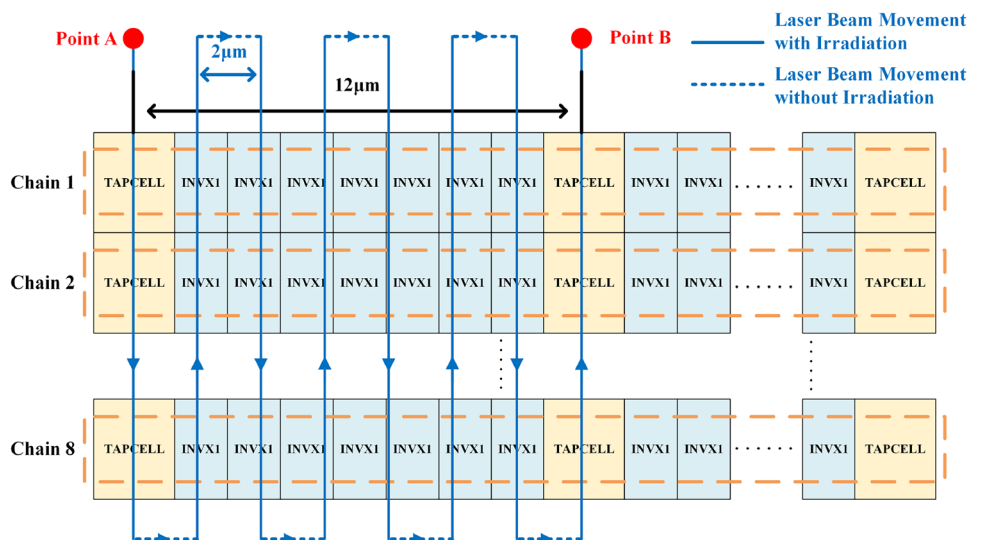
## 2 Experimental setup

To evaluate the relationship between well contact distance and SET pulse width, we designed SET capture and measurement circuits, which were fabricated using the 16-nm gate length FinFET process. A schematic of this process is shown in Fig. 2. The SET capture circuit comprises eight INVX1 cell chains. Each chain contains 1024 INVX1 inverters. X1 represents the driving ability of the inverter, which is composed of one 4-fin NMOS and PMOS. The OR8 tree merges the eight inverter chain outputs and is then connected to the two measurement modules. The two measurement modules sample one inverter group to avoid energetic particle impact on one measurement module. However, the well contact distance investigation should consider the physical design of the circuits. The layout of the SET capture circuit is shown in Fig. 3. The Tapcell is the well contact position in digital circuits. The distance between two Tapcells on a line is 12  $\mu\text{m}$ . The INVX1 and

**Fig. 2** (Color online) Schematic of SET test circuit. Two measurement modules are applied in the same SET capture circuit to avoid radiation affecting the measurement



**Fig. 3** (Color online) Laser beam test procedure. The laser beam moves toward the “S” like path



Filler cells are filled between two Tapcells. The fillers are inserted between two INVX1 cells to satisfy the routing requirements of the foundry. There are 128 INVX1 cells between two Tapcells.

The SET measurement circuits were first described in Ref. [42] and are illustrated in Fig. 4. Two groups of latches and DFFs were applied to sample the SET to mitigate the SEU impact on the measurement circuit in the measurement module; one samples the even stages, and the other samples the odd stages. A typical SET pulse pattern looks like “00000111110000”. The even and odd measurement circuits sample the same SET pulse but 1-bit shorter or longer, respectively. If the SEU happens in one measurement circuit, the SET pulse pattern would be like “00000110110000” or “0100011110000”. The error can be corrected by comparison with the other measurement circuit result. Meanwhile, two measurement modules were used to measure the same SET capture circuit to filter the SET event in one of the measurement modules. If the SET occurs in one measurement module, only one measurement module outputs the data, while the other waits. The typical SET capture flow is as follows. If the SET occurs in the inverter chains, the HOLD port will flip to HIGH, and then, the first stage latches the sample of the SET pulse and stores it. The outer FPGA obtains the captured signal from HOLD and then provides the clock to the CK port. The S0 port holds LOW from HIGH so that the SET pulse can be pushed out to Q. Finally, S0 changes to HIGH, and RESET is triggered. The final SET

data are cleaned, and the measurement circuit waits for the next SET pulse.

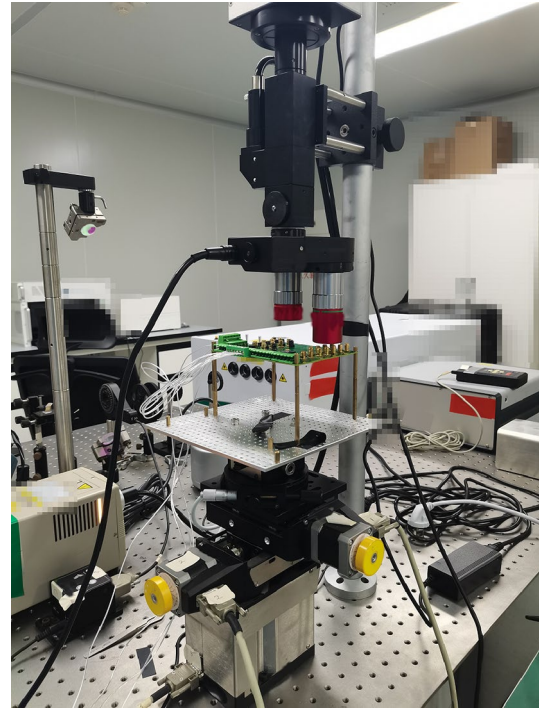
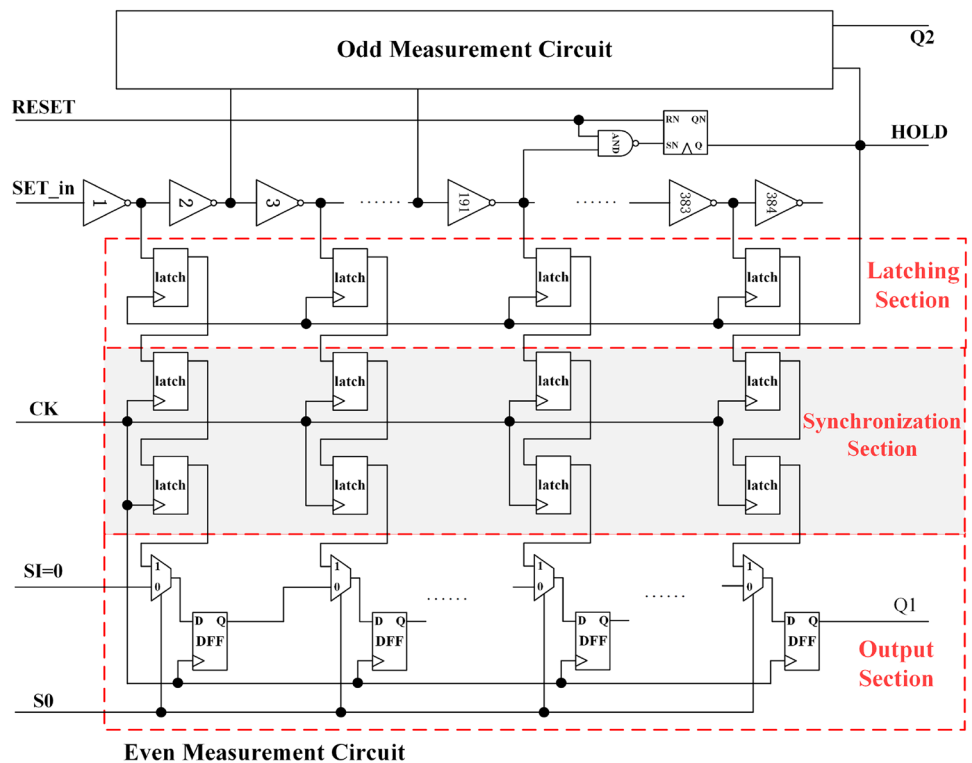


Fig. 5 (Color online) Photograph of the laser experiment system

Fig. 4 (Color online) Schematic of SET measurement circuit

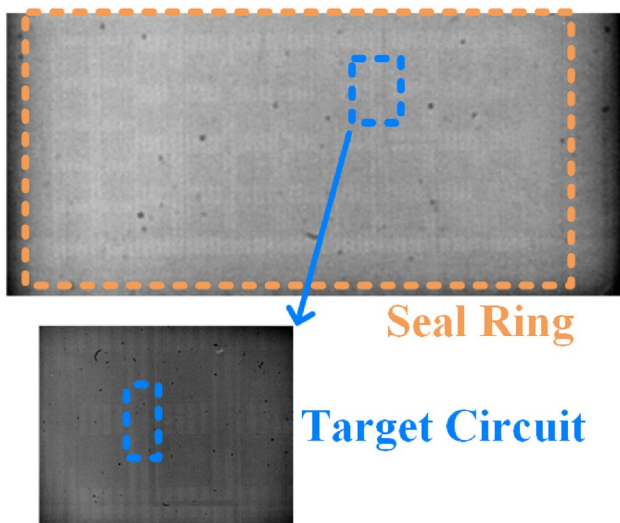


The laser experiment system is shown in Fig. 5; it was performed at the Key Laboratory of Advanced Microprocessor Chips and Systems, National University of Defense Technology. The chip, including the DUT, was packaged as a flip chip. To radiate the DUT effectively, we stripped the top of the package until the die was exposed. A photograph of the die is presented in Fig. 6, captured using a near-infrared camera. The DUT was controlled by an FPGA board, which was used to monitor the DUT, process the SET data, and send the data to a laptop. The TPA was applied in the pulsed laser experiment with a wavelength of 1064 nm, pulse duration of 5 ps, and spot size of 1  $\mu\text{m}$ . The DUT was irradiated with 3.0 nJ energy. The procedure of the laser experiment is described as follows and illustrated in Fig. 3. The laser beam was moved to the edge of the Tapcell, which is Point A in Fig. 3. The laser beam was then vertically swept 10 times. The SET pulse width was calculated as the average of the 10 sweeps to avoid shaking impact when the motor moved the DUT. After capturing the SET data near Point A, the laser beam moved 1  $\mu\text{m}$  toward Point B horizontally, which is the nearest Tapcell to Point A. SET pulse capture was continued until the laser beam arrived at Point B.

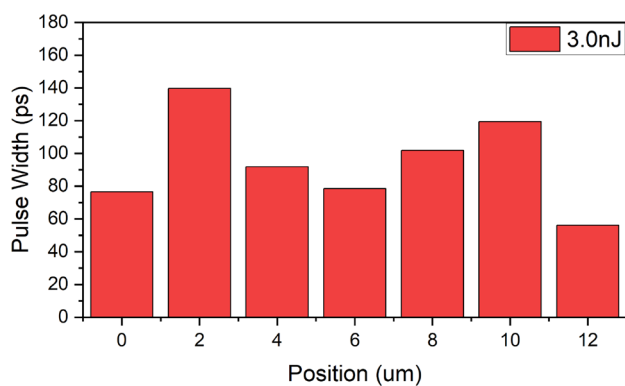
### 3 Experiment result and TCAD modeling

#### 3.1 Experiment results

Figure 7 shows the results of the pulsed laser experiment. The X-axis represents the distance between the laser beam and Point A in Fig. 3, while the Y-axis indicates the SET pulse width. The pulse laser beam energy was 3.0 nJ. The



**Fig. 6** (Color online) Die photograph shot by near infrared camera. The target circuit is marked by the rectangle



**Fig. 7** (Color online) SET distribution under 3 nJ laser TPA irradiation

experimental results show that the lowest SET pulse width was only observed at 0  $\mu\text{m}$  and 12  $\mu\text{m}$ , which are the Tapcell positions. This means that the pulse laser beam center radiates the Tapcell, and only adjacent inverter cells are affected by the outer side of the pulse laser beam. However, the maximum SET pulse width was caught at the 2  $\mu\text{m}$  and 10  $\mu\text{m}$  positions. The SET pulse width was almost the same between 4  $\mu\text{m}$  and 8  $\mu\text{m}$ . A bimodal symmetric SET pulse width distribution was observed. This is an abnormal phenomenon compared to bulk planar CMOS devices. Therefore, the experimental results show that the distance between the device and well contact affects the SET pulse width nonlinearly, which indicates a new mechanism of well contact distance on SET.

The pulsed laser experimental results show that well contact distance has less impact on SET pulse width in the sub-20 nm FinFET process. According to the traditional knowledge of SET in bulk planar CMOS processes, well contact distance linearly affects the SET pulse width. The smaller the distance between devices and well contact, the lower the SET pulse width. However, a nonlinear phenomenon was observed in the pulsed laser experimental results on FinFET. Thus, it is essential to understand the mechanism of the lower impact of well contact distance in the sub-20 nm FinFET process. A high-precision FinFET TCAD model with accurate geometry and doping profile was developed to investigate this phenomenon numerically.

#### 3.2 TCAD model setup and calibration results

A precise TCAD model is essential for investigating the SET mechanism. To ensure the accuracy of TCAD simulation results, it is important to select the correct physical models and device parameters. This section discusses the TCAD simulation settings, physical model selection, and device profile used to establish a reliable TCAD simulation.

The carrier transport equation is the major numerical method in TCAD simulation. Conventionally, for such a small channel length, hydrodynamics should be used to simulate the carrier in a FinFET device. However, the hydrodynamic model considers the electron affinity and band gap impact on carriers, which results in a longer simulation time and difficulty in convergence when the carrier density and potential change rapidly, similar to heavy-ion injection. Thus, using the Monte Carlo-calibrated drift-diffusion model to simulate advanced devices becomes another efficient choice. The Monte Carlo carrier transport simulation was performed based on the Boltzmann equation for a full band structure and accounts for ballistic transport, which is a more precise method. However, Monte Carlo simulation requires considerable computing time, even more than the hydrodynamic model. Therefore, a calibrated drift-diffusion model based on the Monte Carlo method was considered, providing equal simulation results for the same device. We used the Monte Carlo-calibrated drift-diffusion model as the basic device parameter data to calibrate the FinFET TCAD model for a more precise simulation.

For the physical model, typical models that satisfy FinFET were applied to device simulation, including the following:

#### **IAL mobility model:**

The Inversion and Accumulation Layer (IAL) mobility model considers carrier movement at the inversion and accumulation, which is located in the channel of the device [43]. The IAL model is widely used in advanced bulk silicon devices, including FinFET. Meanwhile, the IAL also describes the carrier degradation factors, including Coulomb, phonon, and surface roughness scattering.

#### **High-field saturation model:**

In a device with a high electric field channel, the carrier velocity is not proportional to the electric field. This maintains a finite velocity after the device is saturated, which is called the saturation velocity. The high-field saturation model describes the saturation phenomenon in advanced devices [44].

#### **Thin-layer mobility model:**

The thickness of the FinFET device channel is only several nanometers, which means that the carrier mobility becomes quantized and cannot be expressed by the traditional model like surface roughness [45]. The thin-layer mobility model considers the influence of channel thickness. This calibrates the mobility of a thin-channel device.

#### **Stress effect model:**

Strain engineering is essential for the advanced silicon device [46]. The stress at the channel induces energy band separation, leading to higher electron and hole mobility. Silicon germanium and silicon carbon have been applied in PMOS and NMOS FinFET devices, respectively. Thus, it is necessary to use the stress effect model to describe the band variation in the FinFET device.

#### **Remote Coulomb Scattering (RCS) [47] and Remote Phonon Scattering (RPS) [48] models:**

In advanced silicon devices, hafnium dioxide has been applied to the gate oxide to achieve higher gate control ability and breakdown voltage. However, HfO<sub>2</sub> cannot satisfactorily bond with silicon or silicon oxide. Thus, an Internal Layer (IL) is established between HfO<sub>2</sub> and silicon. A number of traps still accumulate between HfO<sub>2</sub> and IL, leading to RCS and RPS degradation. RCS and RPS cause threshold voltage shifts and mobility degradation, which should be considered in the FinFET.

It should be noted that the ballistic mobility model was considered in the Monte Carlo simulation, which was used for the drift-diffusion model calibration; therefore, it was not applied in the simulation model.

Parameter extraction from the FinFET process is another complex problem that has confused many research groups. This paper explains the methodology of parameter extraction with respect to individual properties. The geometry and parameters were extracted from the BSIM-CMG model [49] provided by the foundry. For an end-user of the foundry, process information is obtained by reading the PDK information and finding the paper on the target process. Most foundries apply the SPICE and RC extraction models, which can release some process information. The SPICE model of FinFET must obey the BSIM-CMG model definition, and extra-defined models are appended around the Compact core model. Table 1 lists some parameters extracted from the SPICE model. These parameters are related to the doping and geometry that can be used to build the FinFET TCAD models. The parameters extracted from the SPICE model may be incorrect; however, the SPICE model has the same theory as TCAD for essential technology. Thus, the SPICE model provides a basis for calibrating the TCAD model. Owing to commercial secrets, the detailed process names and parameters cannot be released. Thus, the parameters listed in Table 1 are not sufficiently precise to repeat the simulation, but the magnitudes are correct. It should be noted that the data in this study were from a foundry PDK, and approximately parameters are shown to protect the foundry's commercial secrets.

**Table 1** NMOS SVT geometry and doping parameters extracted from SPICE model

Parameter name	Description	Value
phig	Work function	4.4 eV
toxg	Oxide thickness for gate current model	$1.4 \times 10^{-9}$ m
toxp	Physical oxide thickness	$1.1 \times 10^{-9}$ m
nbody	Channel (body) doping concentration	$1 \times 10^{23}$ m <sup>-3</sup>
nsd	S/D doping concentration	$1 \times 10^{26}$ m <sup>-3</sup>
lrsd	Length of the source/drain	$7 \times 10^{-8}$ m
fpitch	Fin pitch	$4.8 \times 10^{-8}$ m
hfin	Fin height	$3 \times 10^{-8}$ m
tfin	Body(fin) thickness	$6 \times 10^{-9}$ m

Furthermore, the parameters that the SPICE model does not release should be set in the TCAD model, including well doping concentration, SiGe and SiC mole fractions, and well depth. These parameters are not considered in the SPICE model but are necessary for the radiation effect feature TCAD simulation. Thus, we collected the parameters from publications to improve the TCAD model. In Refs. [50–53], basic FinFET geometry parameters have been provided. Reference [54] provides the contact resistivities in FinFET process. In Refs. [55–57], the gate oxide geometry, work function and trap features have been revealed. In Refs. [58–60], the doping profiles of FinFET have been provided. The ranges of several process parameters were provided in these papers above, and then, we imported them and adjusted the values to calibrate the  $I$ – $V$  features of the TCAD model. Table 2 shows the ranges of the features that can be calibrated, as shown in other papers, and fit the FinFET process. Meanwhile, the parameters in publications were used to verify the SPICE-provided parameters, which may not be filled based on physical data but only calibrated by mathematical fitting. Therefore, these works guarantee the quality of the TCAD model and match the foundry-processed device.

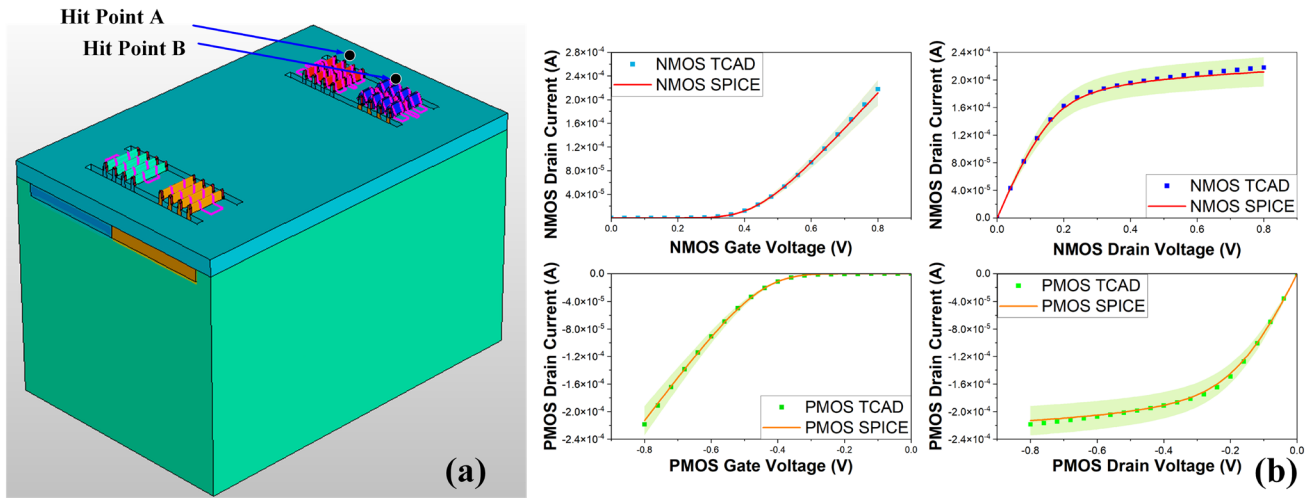
To validate the modeling methodology, a mainstream FinFET process with a channel length of 16 nm was selected. A commercial TCAD software was used for the simulations. Figure 8a shows the TCAD model with well contact, and Fig. 8b shows the individual device  $I$ – $V$  calibration results for the standard threshold voltage (SVT, the highest threshold voltage) selected to establish the four-fin inverter. The points indicate the TCAD simulated results, while the constant line indicates the golden and green areas' mean  $\pm 10\%$  difference ranges extracted from SPICE models. The SPICE  $I$ – $V$  curves are set to the golden curve; then, the 10%  $I$ – $V$  curves are the upper bound, and  $-10\%$  are the lower bound. The results show that the TCAD simulation result lies between the upper and lower bounds of the golden curves, indicating that the TCAD model has excellent precision. Three other threshold voltage transistors were calibrated, and the results were within the  $\pm 10\%$  difference range lines.

## 4 Discussion

We established the inverter model with different well contact distances based on the calibrated FinFET TCAD model to measure the impact of well contact distance. The well contact distance was set to 1.0  $\mu\text{m}$ , 3.0  $\mu\text{m}$ , 6.0  $\mu\text{m}$ , and 12.0  $\mu\text{m}$ . 1.0  $\mu\text{m}$  is near the lowest well contact distance allowed by the foundry design rule. Typically, the well contact distance is 12.0  $\mu\text{m}$  in the digital circuit layout at the FinFET process node. Thus, we established the FinFET inverter TCAD model with fin–well contact, as shown in Fig. 8a on the left side of the model. We chose the SVT transistors to build the inverter TCAD model. The physical models were imported similarly to the simulation in the  $I$ – $V$  calibration. For the heavy ion simulation setting, the radius of the heavy ion was set to 100 nm, according to a previous study [61]. The linear energy transfer (LET) was set to 70 MeV  $\cdot$  cm<sup>2</sup>/mg based on the TPA equivalent LET calculation method in Ref. [62]. Figure 8a shows the hitting position when the heavy ion simulations are performed. Hit Point A is for NMOS, while

**Table 2** Key feature ranges in FinFET Model

Property name	Range
Stress from STI	1 GPa tensile stress normally
Mole fraction of Si <sub>x</sub> Ge <sub>y</sub>	$x = 0.5, y = 0.5$ normally. $0.3 < y < 0.7$
Mole fraction of Si <sub>x</sub> C <sub>y</sub>	$x = 0.97, y = 0.03$ normally. $0.02 < y < 0.04$
Trap concentration	Both acceptor and donor in the range of $1 \times 10^{10} \sim 1 \times 10^{12}$
Trap band structure	Middle band, normally
Trap cross section	$1 \times 10^{-10} \sim 1 \times 10^{-19}$
Dielectric constant of High-K	16~26
Contact resistance	Below $5 \times 10^{-8}$
Velocity of carrier	$0.9 \times 10^7 \sim 8 \times 10^7$ , refer to the SPICE model.



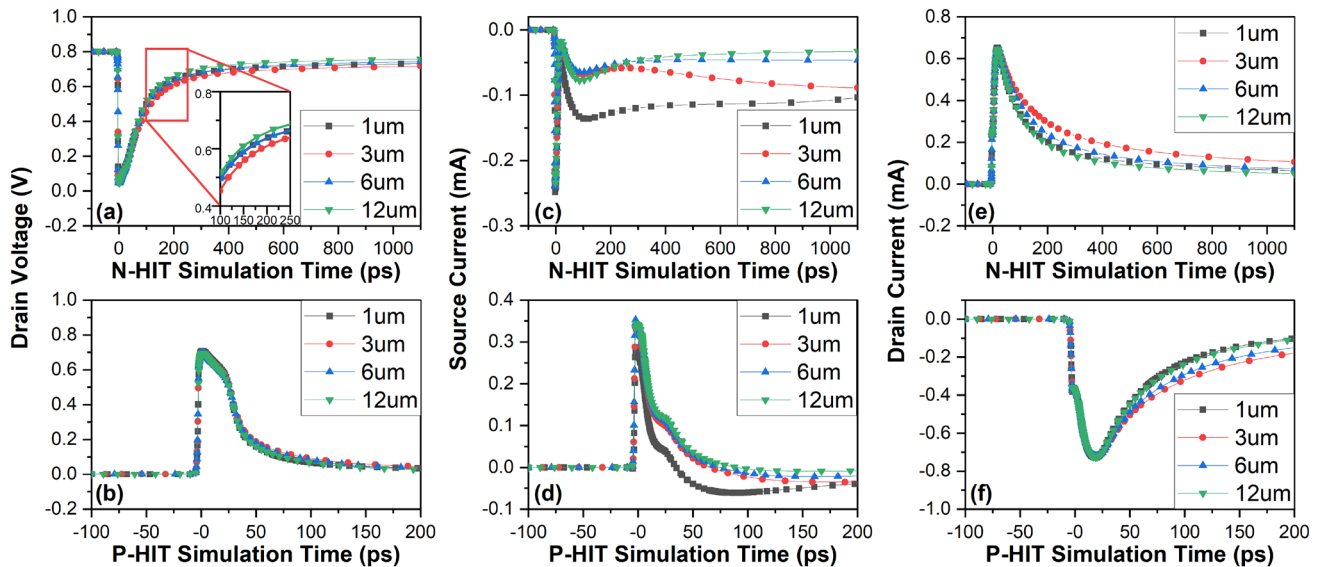
**Fig. 8** (Color online) TCAD model for heavy ion simulation and NMOS and PMOS  $I$ - $V$  calibration results. **a** Blue represents the P+ doping of silicon, and red represents the N+ doping of silicon. Light blue represents the oxide, and green represents the P substrate. When

the NMOS SET feature is tested, Point A will be hit. Otherwise, Point B will be hit. **b** TCAD  $I$ - $V$  simulation results compared to the golden model. The golden model of  $I$ - $V$  was extracted from the SPICE model

Hit Point B is for PMOS. The heavy ion hits the drain of NMOS or PMOS when the device is off, which is the worst and most typical SET case condition [63–65]. Then, we monitored the drain voltage and source current variation to analyze whether bipolar amplification or Drift & Diffusion is the major mechanism.

The relationships between NMOS and PMOS hit SET pulse width and the well contact distance simulation results are shown in Fig. 9a, b, respectively. In the NMOS hit, the drain voltage curve shows that the SET pulse width peak

is caught when the well contact distance is 3  $\mu\text{m}$ , while the minimum SET pulse width is at 12  $\mu\text{m}$ . The simulation results approached the experimental results, which obtained the maximum SET pulse width at 2  $\mu\text{m}$ . However, the SET pulse widths remained constant as the well contact distance increased in PMOS hit. The source and drain currents of the hit transistor results are presented in Fig. 9c–f. The NMOS hit has a longer SET pulse width than the PMOS hit, as reported in Ref. [66]. In the NMOS hit, the source and drain have contrasting current directions after a heavy ion strikes



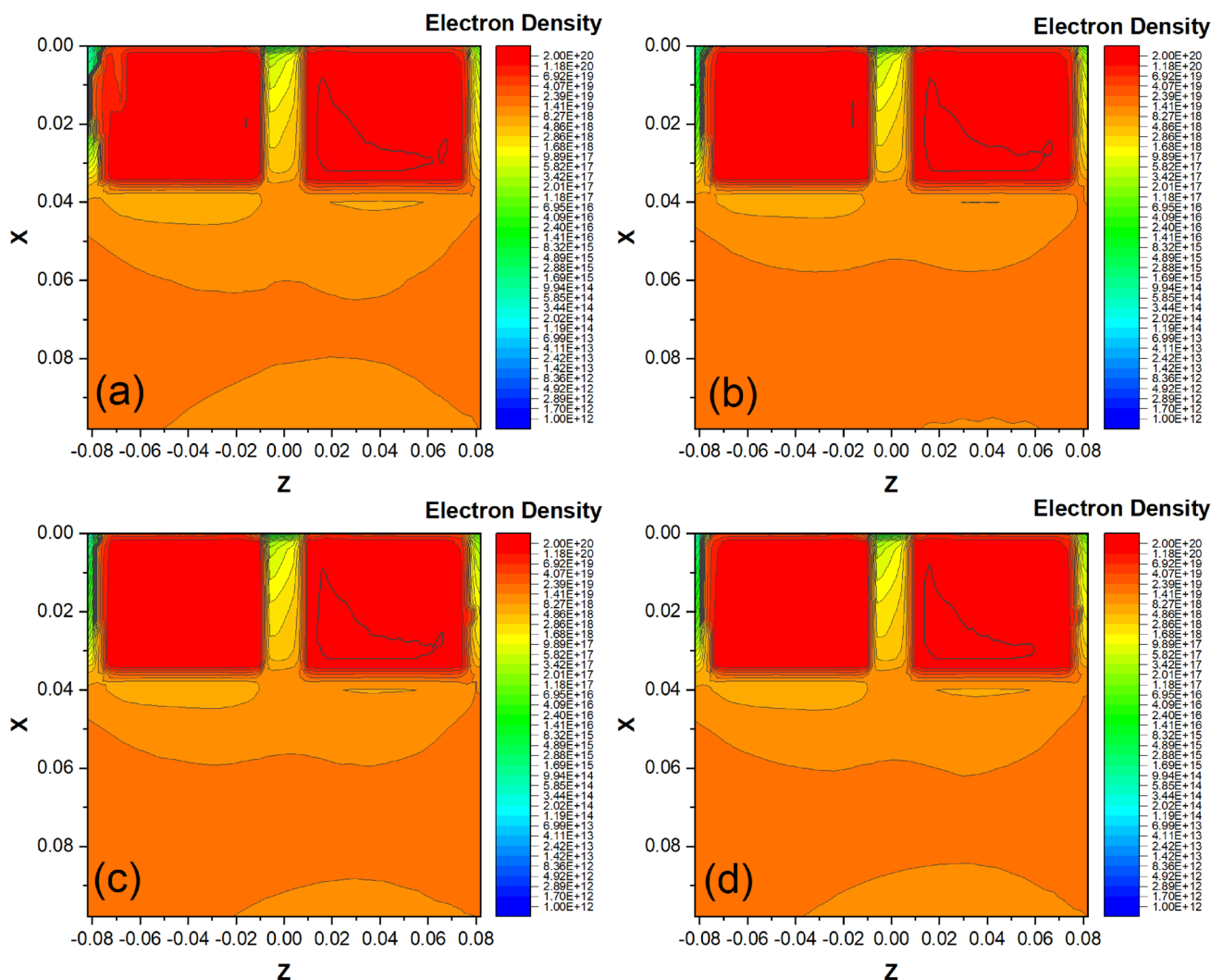
**Fig. 9** (Color online) The TCAD heavy ion simulation results in 1  $\mu\text{m}$  to 12  $\mu\text{m}$  well contact distance. **a** the drain voltage in NMOS Hit (N-HIT) condition. **b** the drain voltage in PMOS Hit (P-HIT) condi-

tion. **c** the source current in N-HIT condition. **d** the source current in P-HIT condition. **e** the drain current in N-HIT condition. **f** the drain current in P-HIT condition

the device, regardless of the contact distance. This phenomenon indicates that bipolar amplification is the major charge sharing mechanism in FinFET NMOS hits. However, the mechanism of PMOS hit is different. After a short period of bipolar amplification, the source current reverts its direction, which is the same as the drain direction. This implies that drift & diffusion is the major charge sharing mechanism in the FinFET PMOS hit. Meanwhile, the SET pulse width caused by the bipolar amplification increases as the well contact distance increases, similar to the bulk planar CMOS process [18]. However, the amplitude of the plateau in the SET pulse is lower than 0.1 V, which does not affect the digital circuit and cannot be sampled by the measurement circuits. This implies that the SET pulse width growth caused by bipolar amplification becomes limited, which is completely different from the bulk planar CMOS device. Therefore, it can be concluded that the maximum SET pulse

width occurs at the center of the well contact distance in the NMOS hit, which plays a major role in FinFET SET.

To determine the detailed mechanism that causes the nonlinear SET pulse width to vary with the well contact distance, electron density contour maps were drawn, as illustrated in Fig. 10. Figure 10 shows a snapshot of the heavy ion striking. The cutline is at the center of the fin and parallel to the channel. It can be observed that the case with a 3  $\mu\text{m}$  well contact distance has the highest electron density because of the ionized electron–hole pairs below the channel. The high electron density below the channel indicates the strength of bipolar amplification. A higher potential below the channel induces a larger bipolar amplification current in the NMOS device. In contrast, the other well contact distances have an electron density lower than 3  $\mu\text{m}$ . Lower SET pulse widths are also observed. In the traditional methodology, dense and close well contact can inhibit bipolar

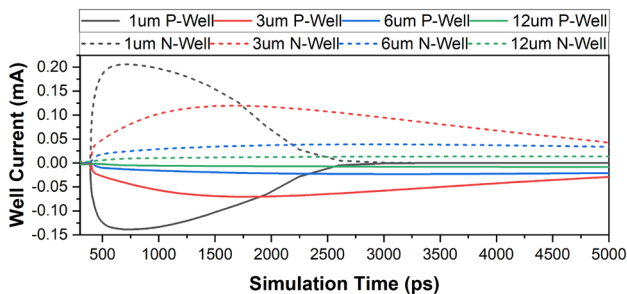


**Fig. 10** (Color online) NMOS electron density simulation result after 40 ps heavy ion injection when the well contact distance is 1  $\mu\text{m}$  (a), 3  $\mu\text{m}$  (b), 6  $\mu\text{m}$  (c), and 12  $\mu\text{m}$  (d). The maximum electron density distribution is observed under the 3  $\mu\text{m}$  condition

amplification by absorbing the charge below the device so that the electrons can be recovered rapidly. Therefore, the electron density contour maps indicate that the factors that can influence the electron distribution on the fin are key to the nonlinear SET pulse width.

Considering the contour map above, the well current distribution should be considered. Figure 11 shows the N-Well and P-Well current variations under the N-Hit condition. The simulation results show that the largest peak current is observed at the 1  $\mu\text{m}$  well contact distance, which is the shortest, while it has the shortest charge collection time. In contrast, the lowest peak current is observed at the 12  $\mu\text{m}$  well contact distance, which is the longest, while it has the longest charge collection time. The current simulation is inconsistent with the bulk planar CMOS. However, it was noticed that the N-Well involves charge collection, whereas heavy ions are injected into the P-Well. The N-Well contact current shuts down when the P-Well current reaches zero. This phenomenon indicates that the current from the N-well contact influences the charge collection and charge sharing in the NMOS. The ionized charges destroy the P-N junction between the N-Well and P-Well at the hit NMOS device. The charges are then injected into the P-Well, leading to a higher potential below the FinFET device. The existence of N-Well complicates the discussion of well influence on the N-Hit. Thus, it is essential to effectively remove the impact of N-Well. The major factor causing abnormal SET distribution can be revealed.

To eliminate the impact of the N-Well, a mix-mode TCAD simulation was established. Based on the inverter TCAD model applied above, the PMOS in the inverter is replaced by the SPICE model, which is the same as the TCAD PMOS in terms of electric performance. The replacement of the PMOS implies that the N-Well is at an infinite distance from the P-Well. This excludes the influence of N-Well on NMOS hit. The other settings were the same as those used in the TCAD simulation. If the SET pulse width distribution with the well contact distance becomes linear, the nonlinear phenomenon is caused by the N-Well. The LET in mix-mode simulation was  $70 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ ,



**Fig. 11** (Color online) Well current simulation result after heavy ion injection when the well contact distance is 1–12  $\mu\text{m}$

which is the same as that in the full device simulation. The TCAD simulation results are shown in Fig. 12. Compared with the simulation results of the full TCAD model, the SET pulse widths increase, meaning that the adjacent N-Well can inhibit the SET pulse. However, the maximum SET pulse width position is still at 3  $\mu\text{m}$ , which is the midpoint of the well contact distance. Thus, the adjacent N-Well is not the major factor causing the abnormal SET distribution.

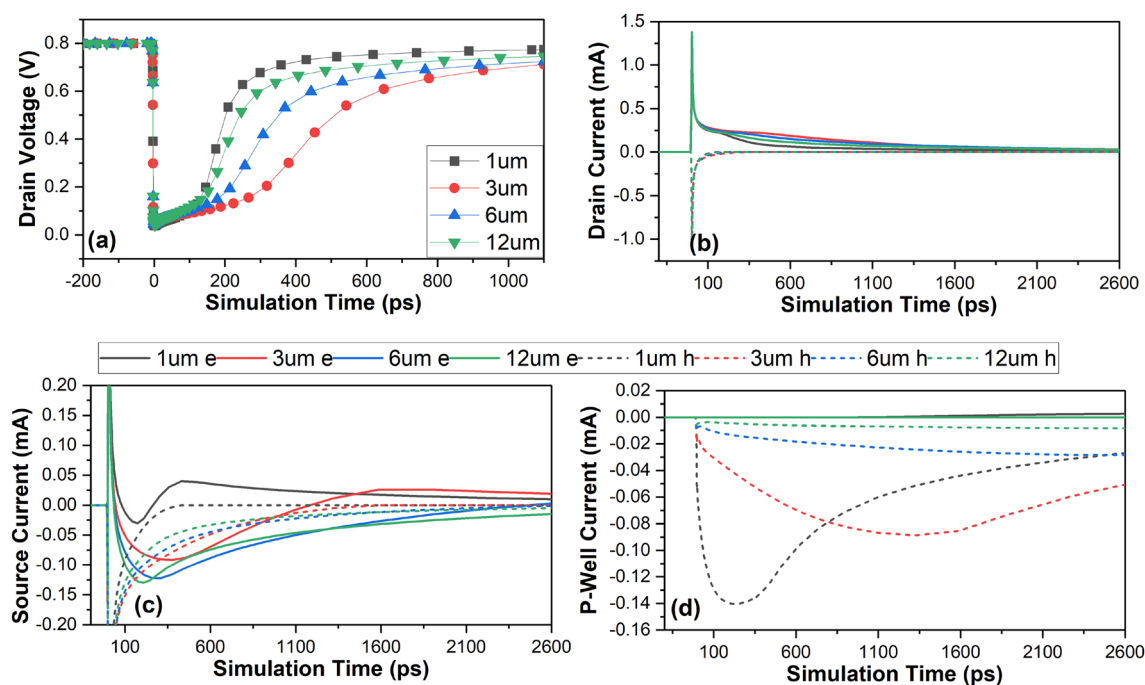
However, the phenomenon becomes more significant after stripping the influence of N-Well. With the help of electron and hole current curves, we can determine what happens after the heavy ion is injected into the NMOS, leading to an abnormal SET distribution. Figure 12 shows the electron currents of the NMOS drain and source and the hole current of P-Well contact. The positive current direction of the electron means the electrons move out of the TCAD device, whereas that of the hole means the hole moves into the TCAD device. Based on the current variation curves, the charge sharing and collection mechanisms of well contact distance lower and larger than 3  $\mu\text{m}$  were different, which causes an abnormal SET distribution on the FinFET device. When the well contact distance is lower than 3  $\mu\text{m}$ , the well contact can inhibit bipolar amplification by absorbing the hole under the device channel. The well contact collects almost all the ionized holes, except for the recombined holes. The electron and hole current relationship between source, drain, and P-Well contact can be specified by Eq. (1), based on the simulation results.  $I_{h, \text{P-Well}}$  is the hole current at the P-Well contact distance,  $I_{e, \text{drain}}$  is the electron current at the drain, and  $I_{e, \text{source}}$  is the electron current at the source.

$$|I_{h, \text{P-Well}}| = |I_{e, \text{drain}} + I_{e, \text{source}}| \quad (1)$$

As the well contact distance increased, the resistance between the well and device increased. This resistance mitigates the charge collection ability from P-Well to the NMOS. The SET pulse width grows with as well contact distance increases, which is similar to the case bulk planar CMOS. When the well contact distance reaches 3  $\mu\text{m}$ , the P-Well contact cannot inhibit the charge collection on the device effectively. The hole current decreases from a maximum of  $1.5 \times 10^{-4} \text{ A}$  at 1  $\mu\text{m}$  to  $5 \times 10^{-6} \text{ A}$  at 12  $\mu\text{m}$ . The charge collection below the channel relies on hole absorption by the source and drain. Thus, we can observe that the source and drain absorb ionized holes more than at 1  $\mu\text{m}$ . However, bipolar amplification can also occur. The electrons used for recombination move to the drain. The electron and hole current relationship between the source, drain, and P-Well contact is specified by Eq. (2).

$$Q_{e, \text{Ionized}}/\Delta t - |I_{h, \text{P-Well}}| = |I_{e, \text{drain}} + I_{e, \text{source}}| \quad (2)$$

When the well contact distance is larger than 3  $\mu\text{m}$ , it is interesting that the source becomes the major mechanism



**Fig. 12** (Color online) Mixed model simulation results when heavy ion hits NMOS. **a** NMOS drain voltage. **b** NMOS drain electron and hole current. **c** NMOS source electron and hole current. **d** P-Well

electron and hole current. The positive direction of the hole current is the holes moved into the device, while the positive direction of the electron is the direction electrons moved out of the device

for purging ionized charges. As the well contact distance increases, the hole density below the channel also increases, leading to higher potential below the device channel. However, the source transfers massive amounts of electrons to the device toward the break P/N junction, inhibiting the potential below the channel. A longer well contact distance leads to higher source electron current due to more holes below the channel. The SET pulse altitude decreases rapidly, leading to a lower pulse width. However, after the P/N junction between channel and source is recovered, charge transfer becomes slower. Thus, despite the SET pulse altitude being too small to disturb the digital circuit, bipolar amplification still broadens the SET pulse width, leading to the longest pulse width in 12  $\mu\text{m}$ , objectively.

Concluding the experiments and simulation, the phenomenon of the maximum SET pulse width occurring at the midpoint of the well contact distance becomes clear in the sub-20 nm FinFET. The SET occurring in NMOS contributes the major factor on the SET on the inverter. When a heavy ion hits the NMOS near the P-Well contact, the well contact distance plays a major role by directly accumulating ionized holes. The SET pulse width increases as the well contact distance increases owing to the higher well resistance. When the heavy ion hits the NMOS, which is far from P-Well contact, the P-Well contact cannot collect the ionized holes effectively. The NMOS source plays a major role in charge collection. The NMOS source transfers electrons

toward the break P/N junction, leading to a lower potential below the channel. However, as the well contact distance increases, the holes below the channel are more dense. The electrons transferred from the source increase, leading to a lower SET pulse width. The peak SET pulse width at the midpoint represents the two mechanisms that change the threshold position.

## 5 Conclusion

In this study, we found a new phenomenon by pulsed laser experiment irradiation on the SET capture and measurement circuitry in the sub-20 nm FinFET process: the distance between well contact and the device plays a smaller role in SET in the sub-20 nm FinFET process. To uncover the underlying mechanism of this phenomenon, a high-precision TCAD model within  $\pm 10\%$  error of the I-V feature at all threshold voltage ranges compared with the foundry process was established. Major physical models were considered for the TCAD FinFET devices. The parameters were calibrated carefully based on the data provided by the foundry and publications. Finally, based on experimental and simulation results, it is revealed that the well contact plays the major role in charge collection at the near-well contact distance, while the source plays the major role at the far distance. The SET pulse width increased with increasing well contact

distance when the well contact was the primary charge collector, whereas it decreased when the source became the major charge collector. The maximum SET pulse width point represents the threshold position at which the influence of these two factors transitions.

The SET influence of well contact distance is completely different from that of the bulk planar CMOS process. This indicates that the SET mechanism in FinFET becomes more complex. This study demonstrated that the traditional SET hardening method, particularly the guard ring, may not be effective in the FinFET process. Therefore, a more specific SET hardening method for FinFET should be considered. Meanwhile, targeted research on SET simulation methods, including precise three-dimensional TCAD and SPICE SET models, should be conducted to ensure that new phenomena and SET hardening performance can be precisely characterized in FinFET.

**Author contributions** All authors contributed to the study conception and design. Conceptualization was performed by Bin Liang, Yang Guo, and Qian Sun. Material preparation and data collection were performed by Qian Sun, Ming Tao, Ya-Hao Fang, Yu-Lin Gao, and Ming-Yan Ma. Data validation was performed by Ming Tao, Zhen-Yu Wu, Wang-Yong Chen, and Peng-Cheng Huang. Funding acquisition was performed by Yang Guo, Bin Liang, Hong-Xia Guo, Ya-Qing Chi, Jian-Jun Chen, and Deng Luo. Writing was performed by Qian Sun, Ming Tao, Han-Han Sun, Zhen-Yu Wu, Wang-Yong Chen, and Peng-Cheng Huang. The first draft of the manuscript was written by Qian Sun, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

**Data availability** The data that support the findings of this study are openly available in Science Data Bank at <https://cstr.cn/31253.11.sciencedb.j00186.00824> and <https://www.doi.org/10.57760/sciencedb.j00186.00824>.

## Declarations

**Conflict of interest** The authors declare that they have no conflict of interest.

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