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Prototype of front-end electronics based on FPGA-ADC for TOF PET detector applications

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Abstract

Traditional digitizers for signal readout of PET detectors are based on commercial analog-to-digital converters (ADC). However, the cost and power consumption of an entire electronic readout system based on digitizers for a PET scanner are high. To address this problem, a soft-core ADC based on a field-programmable gate array (FPGA) was proposed. An FPGA-based ADC (FPGA-ADC) combines low loss and high performance. To achieve good performance, the FPGA-ADC requires three calibrations: time-to-digital converter (TDC) length calibration, TDC alignment calibration, and TDC-to-ADC calibration. A prototype front-end electronics based on FPGA-ADC was built to evaluate the performance of time-of-flight positron emission tomography (TOF PET) detectors. Each PET detector consists of a LYSO crystal single-ended coupled to a silicon photomultiplier (SiPM). The experimental results show that the full-width at half-maximum (FWHM) energy resolution for 511 keV gamma photons after saturation correction of the SiPM was 12.3%. The FWHM coincidence timing resolution (CTR) of the TOF PET detector with the readout of the front-end electronic prototype is 385.2 ps. FPGA-ADC-based front-end electronics are very promising for multichannel, low-cost, highly integrated, and power-efficient readout electronic systems for radiation detector applications.

Keywords Front-end electronics · Analog-to-digital converter · Radiation detector · PET · FPGA

1 Introduction

Positron emission tomography (PET) is widely used in medical imaging and plays a pivotal role in preclinical in vivo research, cancer detection, staging, and treatment [1–3]. In the development of PET detectors, the light-sharing method is commonly employed to discriminate between crystal bars when multiple crystal bars are coupled to a photodetector [4–6]. The time-of-flight (TOF) capability of PET scanners is an advanced technique for improving image quality in PET reconstruction [7, 8]. In addition, good energy resolution is essential for rejecting scatter events and selecting 511 keV gamma photons. To achieve good energy and time resolutions, a linear measurement—where energy is proportional to the digitized code—is typically used, as in commercial ADCs [9–11]. However, these circuits are costly when scaling up to a full imaging system [12]. The time-over-threshold (ToT) [13] offers a simpler alternative by measuring the digital pulse width after the energy signal is compared with a preset threshold V_{th}. Due to its simplicity, cost-effectiveness, and power efficiency, ToT has been implemented in various application-specific integrated

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circuits (ASICs) for PET detector applications [14, 15]. However, the ToT method often suffers from nonlinearity, as the pulse width is not strictly proportional to the energy deposited in the radiation detector. Some ASICs are designed to produce a digital output proportional to the charge collected by the detector [16]. Numerous approaches have been explored to improve the linearity between the digital pulse and the deposited energy, including the multi-voltage threshold (MVT) method [17–19] and the dynamic time-over-threshold (DToT) method [20–22]. The MVT method uses comparators and TDCs to capture pulse information at multiple preset voltage thresholds; the pulse is then reconstructed using a predefined model [17]. The energy resolution (ER) can be significantly improved by selecting appropriate thresholds. In contrast to the ToT method, DToT superimposes a delayed exponential rising voltage waveform on a fixed preset threshold. This dynamically changing threshold is compared with the input pulse to generate a pulse width more closely proportional to the deposited energy [21].

Another readout approach for extracting energy and timing information from a PET detector is the linear discharge scheme [23–25]. In this scheme, the analog circuit requires only one capacitor, two resistors, and an operational amplifier (op amp). In the digital domain, all functions are implemented using a single FPGA. Compared with the ToT method, the linear discharge scheme offers improved linearity between the deposited energy and the digitized codes. Due to its simple circuit structure, it is feasible to design a front-end electronic system with hundreds of channels based on this scheme [26]. Traditional ADC-based front-end electronics suffer from high power consumption and high cost in PET scanner development. In contrast, the field-programmable gate array-based ADC (FPGA-ADC) [27–29] has the potential to address the above problems. In a previous study, we implemented a highly sampling rate (100 MHz & 200 MHz) FPGA-ADC [29] using a multi-chain merged scheme. In this article, we build a PET detector evaluation system based on the designed FPGA-ADC. This system consists of two main components: PET detectors and a readout electronic system based on FPGA-ADC. The hardware design of the system is described in detail. To the best of our knowledge, this is the first investigation of FPGA-ADC technology applied in TOF PET detector applications, which we believe will be highly valuable to developers of TOF PET scanners.

2 Schematic of FPGA-ADC

A basic schematic of the FPGA-ADC is shown in Fig. 1. It consists of an FPGA and an external resistor R. Together, R and the parasitic input capacitance C_{INT} of the Low-Voltage Differential Signaling (LVDS) receiver in the FPGA form an RC_{INT} filter network. This network is driven by an output from the global PLL inside the FPGA. A ramp-like reference waveform is generated at the inverting port of the LVDS receiver. In the FPGA-ADC architecture, the LVDS receiver functions as a voltage comparator. The logic levels are sampled when the input voltage signal $V_{\mathrm{in}}(t)$ is compared with the ramp-like waveform.

The width of V_{out} is proportional to the sampled voltage if V_{ref} is a sawtooth waveform as shown in Fig. 2. The formula is as follows:

$$\frac{V_{\mathrm{BA}}}{V_{\mathrm{Ba}}} = \frac{W_{\mathrm{AC}}}{W_{\mathrm{ab}}}, \tag{1}$$

where V is the voltage, and W is the time width.

In this experiment, V_{ref} was generated using the RC network and exhibited exponential characteristics. Therefore, the resulting time pulse width is approximately proportional to the sampled voltage. If these pulse widths and voltage values are converted into a lookup table, the functionality of an ADC can be implemented directly on the FPGA. A delay line (TDL)-based TDC [30–32] was used to measure the time pulse in real time. To increase the effective number of bits (ENOB) of the FPGA-ADC, the multi-chain merged method [32] was integrated to the TDC delay line. The sampling rates of 100 MHz & 200 MHz were achieved in our previous study [29]. In the following experimental setup, only the 200 MHz sampling rate was used. The TDC delay line was interpolated using two carry chains. To achieve optimum performance, the FPGA-ADC requires three types of calibration: TDC length calibration, TDC alignment calibration, and TDC-to-ADC calibration [28]. TDC length and alignment calibrations were performed prior to sampling. Subsequently, the TDC-to-ADC calibration, conducted offline, is used to convert TDC codes into ADC codes.

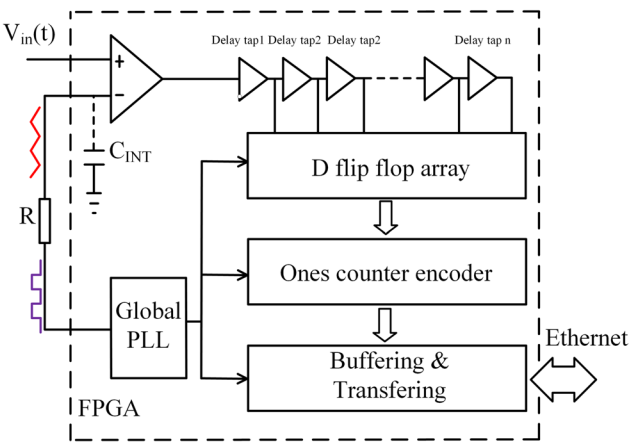

Fig. 1 (Color online) Schematic of the FPGA-ADC

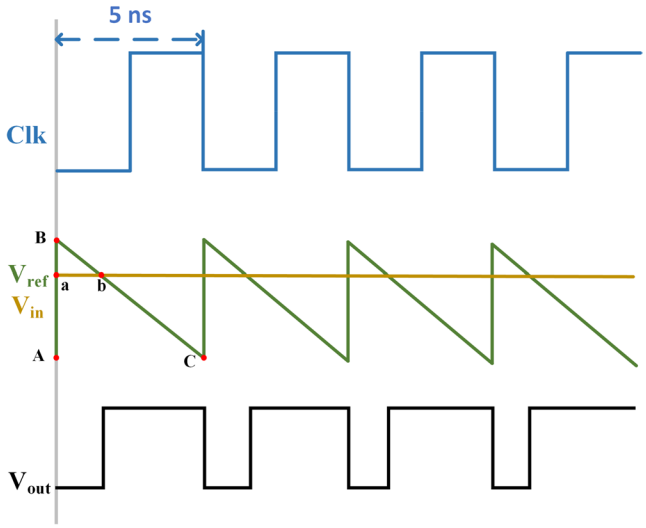

Fig. 2 (Color online) The timing diagram of the FPGA-ADC. The sampling clock at 200 MHz (blue); the referenced ramp signal (green); the input signal (orange); the digital signal through LVDS receiver (black)

(1) TDC length calibration: The TDC delay taps were implemented using carry logic in a Kintex-7 FPGA. The sampling clock frequency was synchronized with the reference waveform, and sampling had to be completed before the next rising edge of the clock. Therefore, the total delay introduced by the carry chain must match the clock period. If the carry chain is too long, overlapping occurs between adjacent sampling points, as illustrated in Fig. 3(b).

A clock signal with a period identical to that of the reference waveform was generated externally and fed into the input port of the FPGA-ADC. Theoretically, the measured duty cycle will remain constant, approximately 50%, as long as the time span of the TDC delay line equals the period of the external clock signal, regardless of the clock's phase.

(2) TDC alignment calibration: Due to the transmission delay introduced by the RC_{INT} filter network, the phase of the TDC clock is not aligned with the ramp-like reference waveform. The clock phase driving the RC_{INT} filter network can be adjusted by modifying the phase parameter of the PLL. Experimentally, a direct current (DC) signal with a voltage value close to the minimum of the FPGA-ADC dynamic range was injected into the FPGA-ADC input. When the TDC clock phase is properly aligned with the reference waveform, two bunches of logic '1' values appear at both ends of the output.

(3) TDC-to-ADC calibration: After performing TDC length and alignment calibrations, the FPGA-ADC can, in principle, convert analog signals into digital signals. However, due to nonlinearity in the TDC bins, such as differential nonlinearity (DNL) and integral nonlinearity (INL), its dynamic performance remains limited. Several techniques exist for TDC-to-ADC calibration, including the 'dithering' method [33]. The transfer curve from input voltage to TDC code can be obtained by applying a low-frequency sawtooth waveform to the FPGA-ADC input. The least significant bit (LSB) of the FPGA-ADC is then

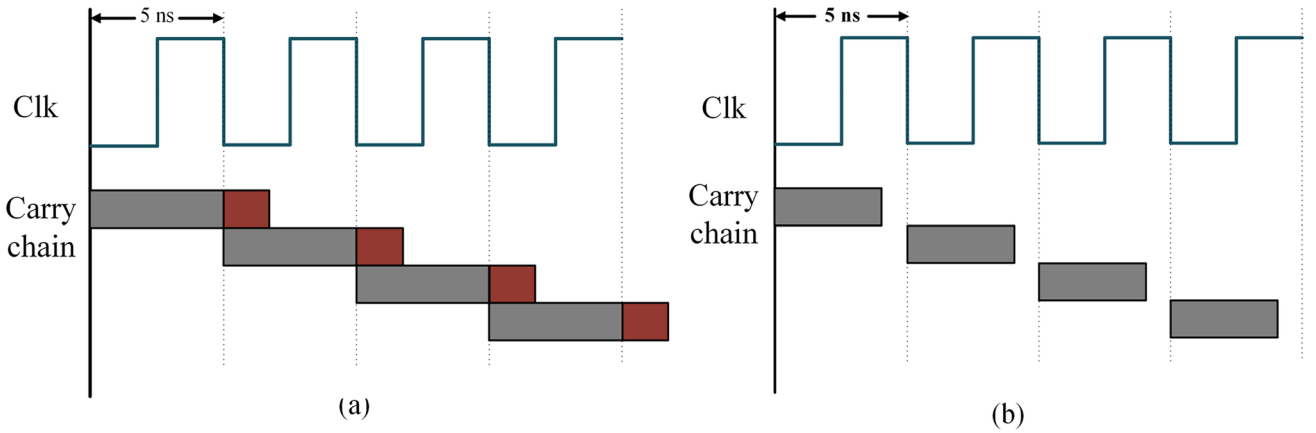

Fig. 3 (Color online) TDC length calibration. **a** Short carry chain. **b** Long carry chain

defined by the relationship between the voltage span and the TDC code span. Using the defined LSB, the calibration process can be performed offline. Further details on the calibration method are provided in [29].

3 Experimental setup

The TOF PET evaluation setup consisted of TOF PET detectors and readout electronics based on FPGA-ADC (Fig. 4). The details are as follows:

3.1 TOF PET detector

Two identical TOF PET detectors were used in the detector evaluation system. Each detector consists of a LYSO crystal bar measuring 3 mm × 3 mm × 10 mm, single-ended and coupled to a SensL J-series silicon photomultiplier (SiPM). The SiPM has an active area of 3 mm × 3 mm, enabling a one-to-one coupling configuration that facilitates optimized timing performance. All surfaces of the crystal bars were polished. One 3 mm × 3 mm end face was coupled to the SiPM, while the remaining five surfaces were wrapped with enhanced specular reflectors (ESR) of thickness 0.065 mm. The coupled SiPM was mounted on a customized adapter board, as shown in Fig. 5. A 3D-printed holder was designed to secure the LYSO crystal bar and SiPM detector. The two TOF PET detectors were mounted on a stainless-steel translation rack, allowing relative positional adjustment between them. To improve light-coupling performance, optical grease (BC-640, Saint-Gobain) was applied between the LYSO bar and the SiPM.

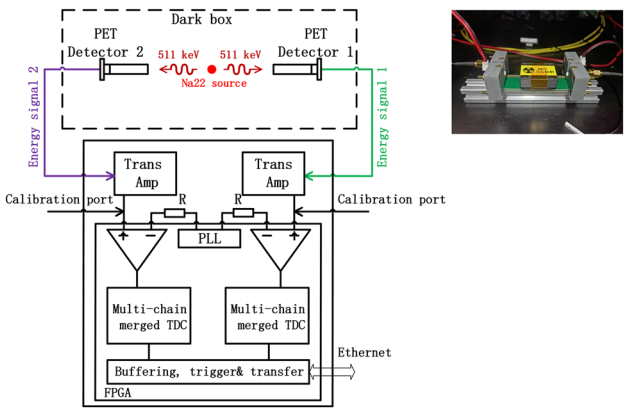

Fig. 4 (Color online) Simplified block diagram of the PET detector evaluation setup

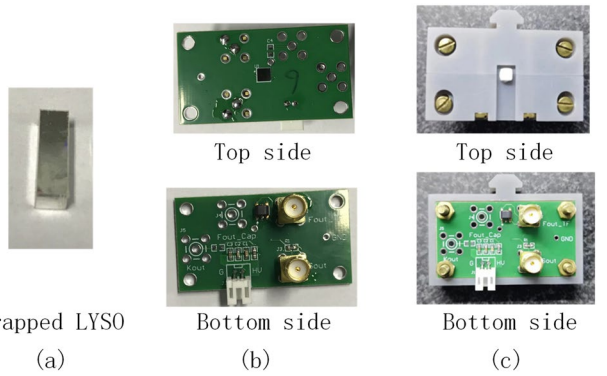

Fig. 5 (Color online) A snapshot of the LYSO crystal bar: **a** adapter board (**b**) and integrated TOF PET detector with a 3D-printed holder (**c**)

3.2 The FPGA-ADC front-end electronics

The current pulses from the detectors were first amplified using a transimpedance amplifier (TIA), which converts the current signals into output voltages. The amplifier used in these experiments was the AD8000. Because the FPGA-ADC can only process positive pulse waveforms, an offset voltage was applied to the noninverting port of the op amp in the TIA to raise the baseline of the input voltage V_{in} (t). This offset voltage was generated using a signal generator.

The amplified voltage signals were then sent directly to the FPGA-ADCs for full-waveform digitization. Additionally, a calibrated port was reserved to allow the injection of a low-frequency signal for calibration purposes. The FPGA-ADCs were implemented on a KC705 development board. The TIA circuits were assembled on a customized PCB, which was connected to the KC705 board via an FMC connector, as shown in Fig. 6.

A block diagram of the firmware design of the FPGA is shown in Fig. 7. Two FPGA-ADCs were implemented in the FPGA based on a multichain merged TDC.

According to our previous research, FPGA-ADCs utilizing two carry chains can achieve good performance at a sampling rate of 200 mega samples per second (MSPS). Only 200 MSPS FPGA-ADCs have been developed and tested experimentally. The implemented FPGA-ADC supports two operational modes: calibration mode (Mode 1) and acquisition mode (Mode 2). In Mode 1, the input waveforms used for calibration such as DC and low-frequency reference voltages are continuously recorded without the need for a trigger. In Mode 2, the input waveform is directed to a first-in-first-out (FIFO) buffer for baseline storage. The number of baseline sampling points in the FIFO was set to 128, which is sufficient for accurate baseline calculation. A multiplexer (Mux) was designed to select data between the two modes. In Mode 2, a global trigger is issued when the waveform data

Fig. 6 (Color online) FPGA-ADC system

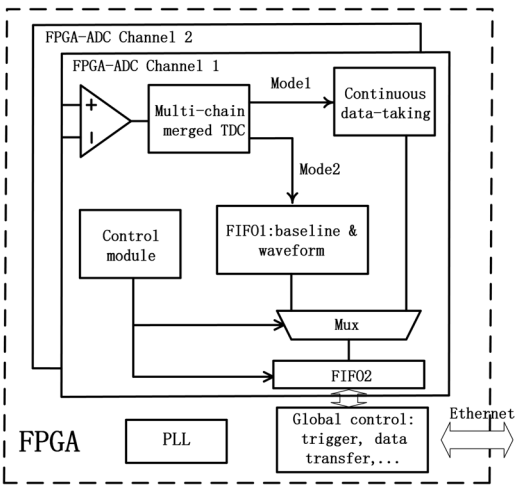

Fig. 7 Block diagram of the firmware design in the FPGA

in both channels cross a user-defined threshold. Coincident waveform data are then transferred to a personal computer (PC) via a previously developed Ethernet interface [34].

A total of 512 samples were collected for each gamma event, and more than 50000 events were used for energy spectrum calculations.

4 Results

In the evaluation experiment, a Na-22 point source was placed at the center between the two TOF PET detectors to irradiate them symmetrically. The back-to-back 511 keV gamma photons resulting from positron annihilation were detected using two LYSO crystal bars. The generated visible light was converted into electrical signals through the photoelectric effect at the entrance of the SiPM detectors. The resulting charge signal, after undergoing avalanche amplification in the SiPM, was fed into a transimpedance amplifier. The nonlinearity between the incident gamma-ray energy and the output charge at the SiPM electrode is primarily due to the SiPM saturation effect [35, 36]. This saturation issue can be corrected by using two measured photopeaks—namely, the 511 keV and 1274 keV gamma rays emitted by the Na22 source—which are given by

$$y = a(1 - e^{-bx}), \tag{2}$$

where x denotes the energies of the two gamma rays, y is the quantized amplitude with arbitrary units according to the specific readout electronics, and a and b are fitting parameters.

Figure 8(a) shows the measured energy spectrum of a TOF PET detector without SiPM saturation correction, obtained using the designed front-end electronics based on FPGA-ADC. A second-to-first peak ratio of less than 1.0 is observed, whereas the theoretical value is 2.49 (1275 keV/511 keV). This deviation indicates significant nonlinearity, with spectral compression becoming more severe at higher energies [37]. Figure 8(b) presents the energy spectrum after applying the saturation correction using Eq. (2). The FWHM energy resolution after fitting and calculation was 13.8%. In the FPGA firmware, a coincident trigger was implemented, which filtered out the 1274 keV gamma photon events. The coincidence timing window was set to 15 ns. Figure 9(a) shows the initial coincident energy spectrum of one TOF PET detector without saturation correction. Figure 9(b) shows the corresponding spectrum with saturation correction. The FWHM energy resolution after correction was 12.3%.

The CTR performance of both TOF PET detectors was evaluated with the SiPM overvoltage set to VOVER_VOLTAGE = 6.5 V ($V_{\mathrm{BIAS}} = 31$ V). In the coincidence energy spectra, over 20,000 events fell within an energy window defined as twice the FWHM of the 511 keV gamma peak. The distribution of the arrival time difference of 511 keV gamma photons in the two detectors was plotted. Figure 10 depicts the coincident time-difference spectrum of the two TOF PET detectors. The FWHM CTR value of the evaluation setup after Gaussian fitting is 385.2 ps. The performance summary and comparison with previous work [38] are shown in Table 1.

5 Discussion

Overall, the FPGA-ADC-based front-end electronics demonstrated performance comparable to that of commercially available off-the-shelf ADC chips. While the soft-core FPGA-ADC cannot fully replace all ASIC-based ADCs, it

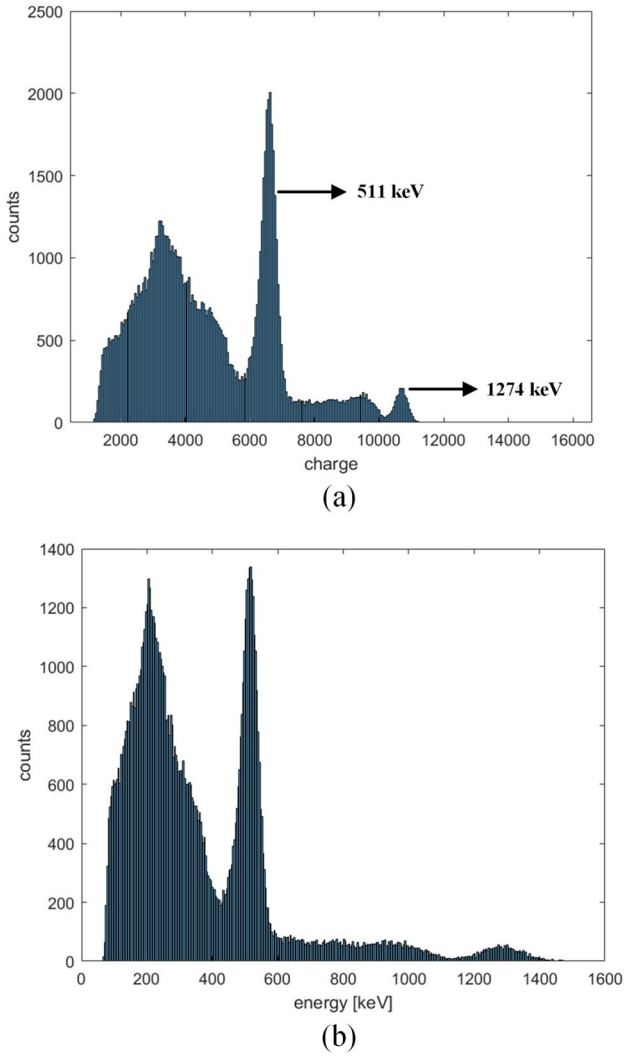

Fig. 8 (Color online) Energy spectra without (**a**) and with (**b**) SiPM saturation corrections

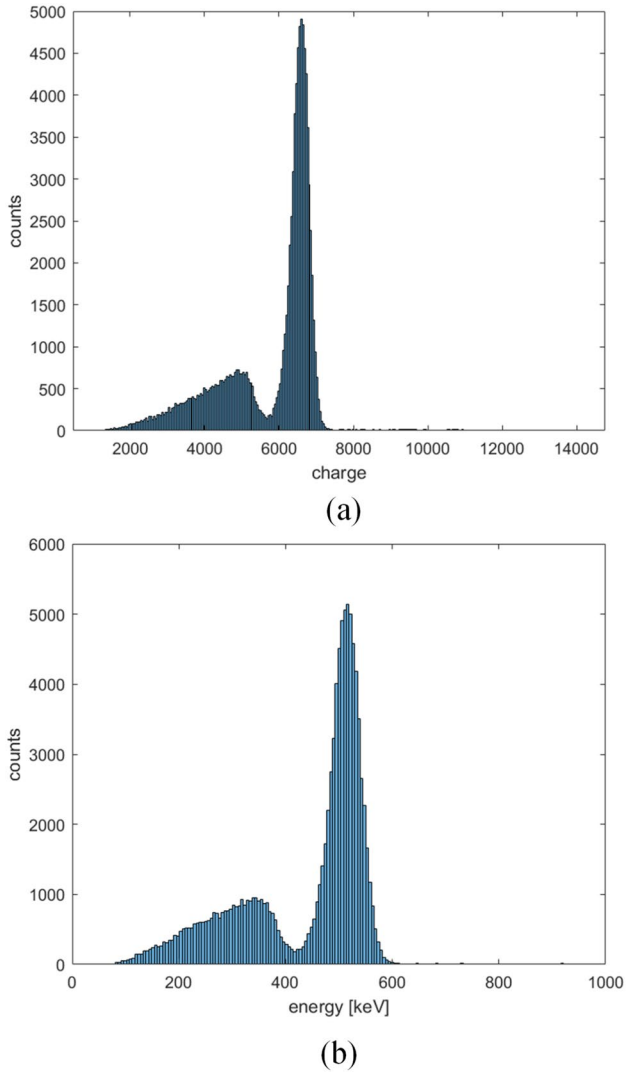

Fig. 9 (Color online) Coincident energy spectrum of one TOF PET detector without (**a**) and with (**b**) SiPM saturation corrections

significantly extends the functionality of FPGAs with minimal hardware modification in current physics experiments. In our previous work [39], the intrinsic CTR performance of TOF PET detectors was evaluated using a high-performance oscilloscope with a 1-GHz bandwidth and a 5-GSPS sampling rate. The SensL SiPM detector provides two outputs: a standard output (S_{out}) and a capacitively coupled fast output (F_{out}). The S_{out} signal, characterized by a slow rise time, is typically used for energy calculations. In contrast, the F_{out} signal exhibits a rise time of less than 2 ns and is primarily used for timing performance evaluation. When measured using the F_{out} signals and a high sampling rate oscilloscope, the CTR performance can reach ~200 ps. In the current FPGA-ADC design, the sampling rate is limited to 200 MSPS, and only the S_{out} signal can be processed. Therefore, a higher sampling rate (> 1 GSPS) FPGA-ADC based on clock phase interpolation technique [28] is under development. With this enhanced FPGA-ADC, it is expected that better timing performance can be achieved by directly sampling the F_{out} signal.

In the intrinsic timing experiment, a pulse with a rising edge of 10 ns was split into two identical signals and sent to the two-channel FPGA-ADCs. The resulting time-difference spectrum is shown in Fig. 11.

The raw data were interpolated in the processing software. The sigma value obtained from Gaussian fitting was approximately 107.0 ps.

In FPGA-ADC systems, power consumption primarily depends on the utilization of FPGA resources. A customized PCB was designed to evaluate the power consumption of the system. A trade-off must be considered between ADC performance and resource utilization. To enhance the effective number of bits (ENOB) of the ADC, the multi-chain merged

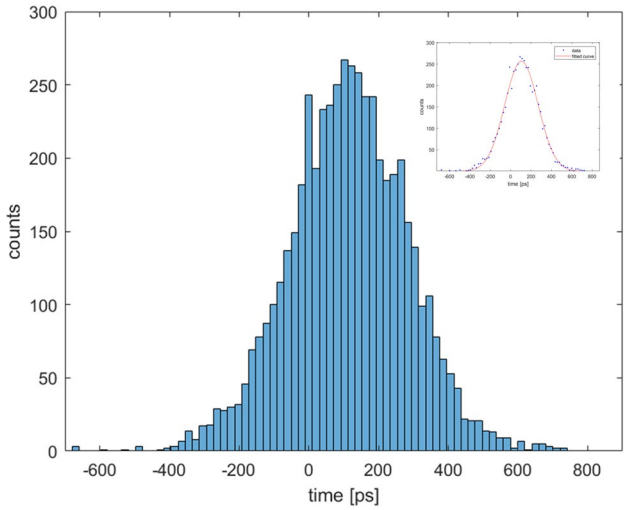

Fig. 10 (Color online) Coincidence timing spectrum of TOF PET evaluation setup

Table 1 Comparison of our work with previous FPGA-ADC prototypes for PET

	Sampling rate (MS/s)	Time resolution (ps)	Energy resolution (%)
This work	200	385.2	12.3
Previous work [38]	25	437.0	13.2

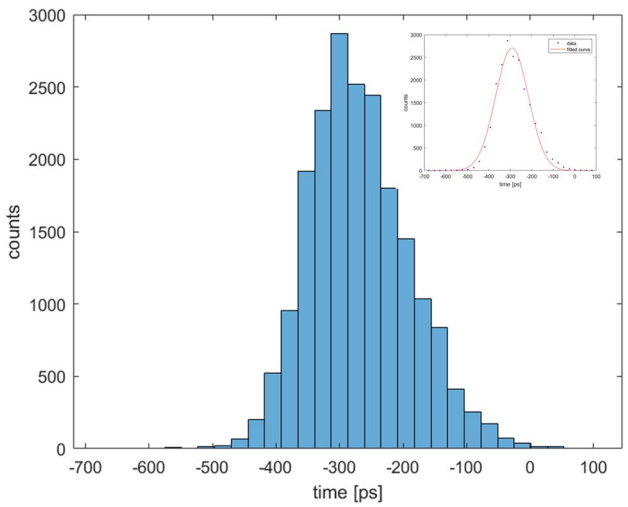

Fig. 11 (Color online) Timing performance of FPGA-ADC

method was employed in the TDC module, with two carry chains used for interpolation.

The available carry chain and other FPGA resources were sufficient to support multiple channels. A customized multichannel FPGA-ADC PCB was developed to optimize the use of these resources. However, designers must remain aware of potential timing issues as FPGA resources are increasingly utilized. For applications requiring a large number of FPGA-ADC channels, multiple FPGA devices may be necessary. Gigabit Transceivers (GTs) can be employed to support higher data transmission rates [40]. In general, the parasitic capacitance C_{INT} at the LVDS receiver is on the order of tens of picofarads. The dynamic range of the FPGA-ADC is determined by the external resistor R. A smaller R allows for a larger dynamic range. In our design, the value of R is 50 Ohm. For front-end electronics involving more channels, additional calibration is required due to variations in C_{INT} across different channels.

6 Conclusion

In this study, a TOF PET evaluation setup incorporating FPGA-ADC technology was developed. A prototype front-end electronics system based on the KC705 development board was designed, featuring two-channel FPGA-ADCs. To enhance the dynamic performance of the FPGA-ADC, the TDC module was interpolated using two carry chains. The TOF PET detector consisted of an LYSO crystal bar wrapped with ESRs and coupled to a SiPM detector. A one-to-one coupling between the LYSO crystal and the SiPM was implemented to optimize performance. The FWHM energy resolution of the TOF PET detector with the FPGA-ADC-based front-end electronics prototype was 12.3 %. The FWHM CTR of the evaluation setup was 385.2 ps. Although the current prototype includes only two channels, additional FPGA-ADC channels can be developed and validated on resource-rich FPGAs without requiring hardware modifications. Therefore, this FPGA-ADC technology shows great promise for front-end readout electronics in modern particle physics experiments.

Author contributions All authors contributed to the study conception and design. Material preparation, data collection, and analysis were performed by S-QL, BW, W-WX, X-SW, and KH. The first draft of the manuscript was written by S-QL, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data availability The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.j00186.00860 and https://www.doi.org/10.57760/sciencedb.j00186.00860.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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