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Back-gate bias and supply voltage dependency on the single-event upset susceptibility of 6 T CSOI-SRAM

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Abstract

This paper explores the impact of back-gate bias (V_{soi}) and supply voltage (V_{DD}) on the single-event upset (SEU) cross section of 0.18 μm configurable silicon-on-insulator static random-access memory (SRAM) under high linear energy transfer heavy-ion experimentation. The experimental findings demonstrate that applying a negative back-gate bias to NMOS and a positive back-gate bias to PMOS enhances the SEU resistance of SRAM. Specifically, as the back-gate bias for N-type transistors (V_{nsoi}) decreases from 0 to −10 V, the SEU cross section decreases by 93.23%, whereas an increase in the back-gate bias for P-type transistors (V_{psoi}) from 0 to 10 V correlates with an 83.7% reduction in SEU cross section. Furthermore, a significant increase in the SEU cross section was observed with increase in supply voltage, as evidenced by a 159% surge at V_{DD} = 1.98 V compared with the nominal voltage of 1.8 V. To explore the physical mechanisms underlying these experimental data, we analyzed the dependence of the critical charge of the circuit and the collected charge on the bias voltage by simulating SEUs using technology computer-aided design.

Keywords Single-event upset (SEU) · Static random-access memory (SRAM) · Back-gate voltage · Supply voltage

1 Introduction

With advancements in space science and technology, an array of spacecraft has been deployed to fulfill various functions in space. However, the integrated circuits in these spacecraft are susceptible to cosmic rays, resulting in single-event effects (SEEs) and total ionizing dose effects (TIDs) [1]. Previous studies have indicated that the single-event upset (SEU) cross section of static random-access memory (SRAM) cells increases as the number of process nodes decreases [2, 3]. To mitigate the increasing severity of SEEs, researchers have proposed radiation-resistant reinforcement designs such as dual interlocked storage cell (DICE), which notably decrease the SEU cross section of the device [4–7]. Nonetheless, circuit-level reinforcement typically results in adverse ramifications, such as

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heightened power consumption, performance deterioration, and increased footprint [8, 9]. Silicon-on-insulator (SOI) technology has been introduced to minimize circuit area and power consumption while attenuating the sensitivity of integrated circuits to SEEs. This technology involves the introduction of a buried oxide (BOX) layer between the silicon film and substrate. This strategic placement mitigates the parasitic capacitance and short-channel effect of the device, thereby achieving comprehensive dielectric isolation of electronic components [10–13].

Although SOI technology can significantly reduce the cross section of transient irradiation effects, such as single-event transients (SETs), single-event latch-ups (SELs), and SEUs [14, 15], SOI devices exhibit decreased resistance to TIDs owing to the introduction of the BOX layer [16–19]. Cosmic rays can introduce trapped charges in the gate oxide, isolation oxide, and BOX layers, resulting in device parameter drift and degradation of electrical performance [20]. As technology nodes scale, the fully depleted silicon-on-insulator (FDSOI) process enhances the susceptibility to SEEs and the gate-control resistance by thinning the gate oxide and BOX layers [21]. However, the presence of a dopant trap region beneath the BOX layer constrains FDSOI back-gate bias and decreases circuit design flexibility. Furthermore, the shallow trench isolation and BOX layer of FDSOI are highly susceptible to TIDs, resulting in the formation of source–drain parasitic paths and a reduction in channel width [22, 23].

Previous studies have indicated that a novel configurable silicon-on-insulator (CSOI) structure can effectively mitigate the irradiation damage caused by TIDs and extend the back-gate bias range of the device [24, 25]. The CSOI process introduces two silicon layers: the top silicon film (SOI1) and underlying SOI2 layer located beneath the conventional BOX layer. In the CSOI device, back-gate biasing is achieved using independent electrodes. This approach not only hinders back-channel formation during irradiation, reduces the threshold voltage drift, and minimizes the leakage current [26, 27] but also efficiently regulates the electric field within the BOX layer. Through the reduction of the threshold voltage drift and leakage current, and by effectively regulating the internal electric field of the BOX layer, independent dynamic compensation of the TID [28] is achieved. CSOI implementation can regulate the drain region potential, thus suppressing SEEs.

The experimental validation and simulation analysis regarding the mitigation of TID through CSOI back-gate bias have been comprehensive. However, experiments and analyses on the dependence of CSOI-SRAM SEUs on the bias voltage when subjected to heavy-ion incidence at high linear energy transfer (LET) values are lacking. This study aimed to investigate the influence of the back-gate bias and supply voltage on the SEU of CSOI-SRAM through a combination of experiments and technology computer-aided design (TCAD) simulations. Additionally, in this paper, we propose a physical mechanism wherein the trend of variation in the SEU cross section with the supply voltage is opposite at high and low LET values. This exploration has significant implications for the understanding and reinforcement of CSOI-SRAM against SEUs.

Sections 2 and 3 describe the experimental setup and discuss the experimental results, respectively. In Sect. 4, we describe the selection of the physical model for TCAD simulation and configuration of the simulation variables. We conducted qualitatively analysis to identify the sensitive state and sensitive region of the CSOI transistor, followed by simulations to explore the effects of back-gate bias and supply voltage on the SEU sensitivity of the CSOI-SRAM. Through simulations that capture variations in physical quantities such as the transient pulse, potential, and collected charge of the SRAM off-state transistor under experimental parameters, we scrutinize and derive the physical mechanism underlying the influence of back-gate bias and supply voltage on the SEU cross section. This analysis explains and validates the experimental findings. Finally, Sect. 5 presents the concluding remarks.

2 Experimental setup

2.1 Experimental device description

The CSOI devices utilized in the experiments were fabricated using the 0.18 μm FDSOI process, and the primary parameters and transistor sizes are listed in Table 1. The overall structure comprised two silicon layers (SOI1 and SOI2) and two oxygen-embedded layers (BOX1 and BOX2). Electronic components were fabricated on the top silicon film, whereas the intermediate silicon layer, SOI2, was positioned between the two oxygen-embedded layers to serve as a back-gate electrode. This electrode enabled adjustment of the electrical performance and resistance of the device to SEUs by modifying the voltage applied to SOI2. Consequently, both the electrical characteristics of the device and

Table 1 Device parameters for CSOI process

Parameters	Value (nm)
Thickness of the top silicon film (TSOI1)	65
Thickness of oxygen-embedded Layer 1 (TBOX1)	145
SOI2 layer thickness (TSOI2)	150
Thickness of oxygen-embedded layer 2 (TBOX2)	145
INV_P channel length	320
INV_N channel length	200
Transfer_N channel length	200

SEU resistance could be tailored by varying the voltage of SOI2. The presence of the BOX layer mitigated the parasitic bipolar amplification effect and decreased leakage currents.

A 4k-bit 6T-SRAM provided by the Institute of Microelectronics of the Chinese Academy of Sciences (IMCAS) was employed to explore the SEU resistance of SRAM fabricated using the CSOI process under varying back-gate biases. The chip package, which houses a 64 × 64-bit memory array with dimensions of approximately 1.45 mm × 1.45 mm, features a bit cell footprint of 10 µm × 8 µm. Within the memory cell, N-type transistors share an NSOI electrode, denoted by V_{nsoi}, whereas P-type transistors share a PSOI electrode, denoted by V_{psoi}. The back-gate biasing of the SRAM ranges from −10 to 10 V. The circuits were encapsulated in DIP-28 packages. Considering the utilization of high-LET heavy ions in the experiment, the devices were decapped to ensure adequate penetration of the heavy ions.

2.2 Experimental setup for heavy-ion irradiation

For the experiments, Ta ions were selected from the TR5 terminal at the Heavy Ion Research Facility in Lanzhou (HIRFL) and the High Energy Heavy Ion Radiation Terminal (HERT) at the Space Environment Simulation and Research Infrastructure (SESRI) at Harbin Institute of Technology. The ion parameters are listed in Table 2, with the fluence set to 5×10^6 ions/cm^2 for each experimental group. To achieve a uniform heavy-ion beam within the irradiated area, we adjusted the scanning current and frequency, coupled with precise control of the irradiated area by manipulating the slit size. Ta-ion irradiation was conducted in air, which was facilitated by the ability of the heavy-ion beam to reach the sensitive region of the device even after passing through a Ti window and traveling several microns in the atmosphere. The heavy ions traversed through a vacuum/air transition foil before impinging on the device. To detect the injection, we positioned an injection detector along the ray trajectory before the device under test. The LET of the ions from the device surface to the detector was adjusted by either inserting an energy attenuator (aluminum foil) into the trajectory of heavy-ion incidence or employing angled ion impingement.

Table 2 Heavy-ion parameters

Heavy-ion parameters	TR5 Terminal	HERT
Ion type	Ta	Ta
Range (µm)	60	51
LET (MeV · cm^2/mg)	86.1	87.3
Fluence (ions/cm^2)	5×10^6	5×10^6
Energy (MeV)	942	759

Experiments were conducted to investigate the impact of NSOI and PSOI electrodes, as well as the power supply voltage, on the SRAM SEUs. Before irradiation, 55+AA-type data were pre-written into the SRAM memory cells with a dynamic reading of the SRAM memory content during irradiation. Any discrepancies between the read and write results were recorded by the test system as either a 0-1 or 1-0 upset, depending on the type of upset observed. These experiments were performed at room temperature while maintaining a flux of approximately 15000 ions/(cm^2 · s) to negate flux effects. A nominal supply voltage of 1.8 V was applied to the test system to simulate the normal operating state of the device. Back-gate biases were uniformly set to zero to assess the effect of the supply voltage on SRAM SEU. Six supply voltage biases were selected: pull-down 20% (1.44 V), pull-down 10% (1.62 V), pull-down 5% (1.71 V), nominal voltage (1.80 V), pull-up 10% (1.98 V), and pull-up 20% (2.16 V). These biases were selected to examine the effect of the supply voltage on SEU.

The SEU overturning cross section is calculated as

$$\sigma_{seu} = \frac{N_{event}}{\text{fluence} \times N_{bit}} \quad (1)$$

where N_{event} is the total number of SEUs, and N_{bit} and fluence are the SRAM memory cell capacity and experimental injection, respectively [29].

3 Discussion of experimental results

The analysis revealed that the total number of SEEs observed in this experiment solely comprised single-bit upsets, with no occurrences of errors, such as multiple-bit upsets or single-event functional interrupts. Figure 1a depicts the dependence of the SEU cross section on V_{nsoi} at LET =86.1 MeV · cm^2/mg, where V_{psoi} was set to zero for all experiments. Notably, the SEU cross section experienced decreases of 47.31%, 87.82%, and 93.23% at V_{nsoi} =–2, − 6, and − 10 V, respectively, compared with the scenario with zero back-gate bias. Conversely, Fig. 1b shows the dependency of the SEU cross section on V_{psoi} under the same LET conditions, with V_{nsoi} set to zero across all experiments. Here, the SEU cross section had decreases of 40.50%, 78.79%, and 83.77% at V_{psoi} =2, 6, and 10V, respectively, compared with the scenario with zero back-gate bias.

Table 3 presents the impact of various back-gate bias combinations on the SEU cross section for LET = 87.3 MeV · cm^2/mg. It demonstrates that the application of negative V_{nsoi} and positive V_{psoi} can effectively mitigate the SEU cross section. Notably, when the sum of the absolute values of the back-gate bias applied to the N-type and P-type transistors of the SRAM was equal, a larger ratio of $|V_{nsoi}|$

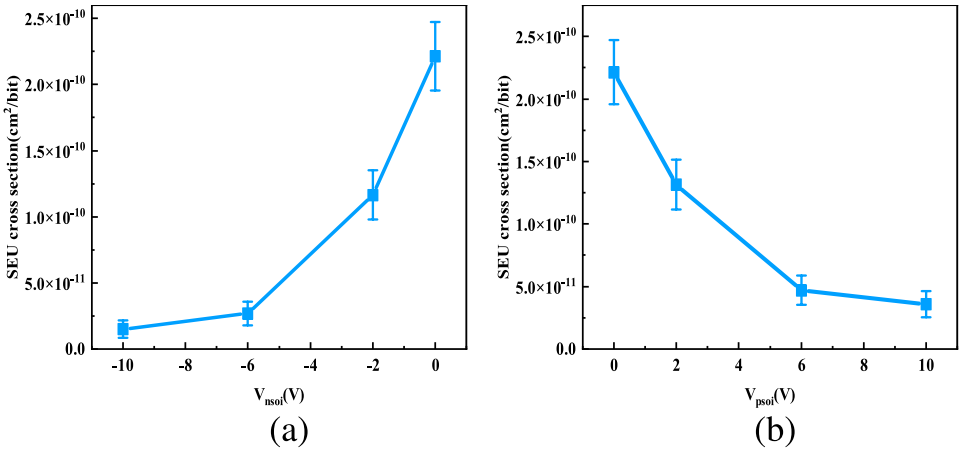

Fig. 1 (Color online) **a** Variation in SEU cross section with back-gate bias V_{nsoi} for LET = 86.1 MeV · cm^2/mg. **b** Variation in SEU cross section with back-gate bias V_{psoi} for LET =86.1 MeV · cm^2/mg

Table 3 Effect of back-gate bias combinations on SEU sensitivity

$V_{psoi}(V)$	$V_{nsoi}(V)$	Number of SEUs	SEU cross section (cm^2/bit)
2	0	51	1.5×10^{-10}
1	−1	47	1.4×10^{-10}
0	−2	43	1.3×10^{-10}
3	−1	24	7.2×10^{-11}
2	−2	19	5.7×10^{-11}
1	−3	19	5.7×10^{-11}
3	−3	2	6.0×10^{-12}

$|V_{psoi}|$ resulted in lower sensitivity of the SRAM to SEU. Moreover, under identical magnitudes of back-gate bias, the negative bias applied to the NSOI electrode of the N-type transistor exhibited superior effectiveness against SEU compared with the positive bias applied to the PSOI electrode of the P-type transistor.

Figure 2a shows the relationship between the SEU cross section and supply voltage at LET = 86.1 MeV · cm^2/mg. Notably, at the nominal applied circuit voltage of 1.8 V, 61 single-bit upsets were recorded, whereas only one single-bit upset occurred at V_{DD} = 1.62 V, and 158 single-bit upsets were observed at V_{DD} = 1.98 V. Furthermore, a 10% increase in the supply voltage resulted in a significant increase in the SEU cross section of 161.67%. This observation suggested that the variation in the thickness of the drain-depletion region with changes in V_{DD} contributed to the escalation of the SEU cross section. Further analysis of this mechanism is provided in detail in Sect. 4.

Figure 2b depicts the relationship between the SEU cross section and supply voltage at LET = 87.3 MeV · cm^2/mg. Compared with the SEU cross section of 3.3×10^{-10} cm^2/bit at nominal voltage, the SEU cross section decreased by 95.40% and 96.30% for a pull-down V_{DD} of 10% and 20%, respectively, and increased by 125.93% and 165.74% for pull-up V_{DD} of 10% and 20%, respectively.

When V_{DD} was below 1.62 V, the resultant drain voltage did not enable the CSOI to establish an effective drain-depletion region capable of efficiently collecting the charge excited by heavy ions. Consequently, the SEU cross section exhibited minimal variation with the supply voltage and

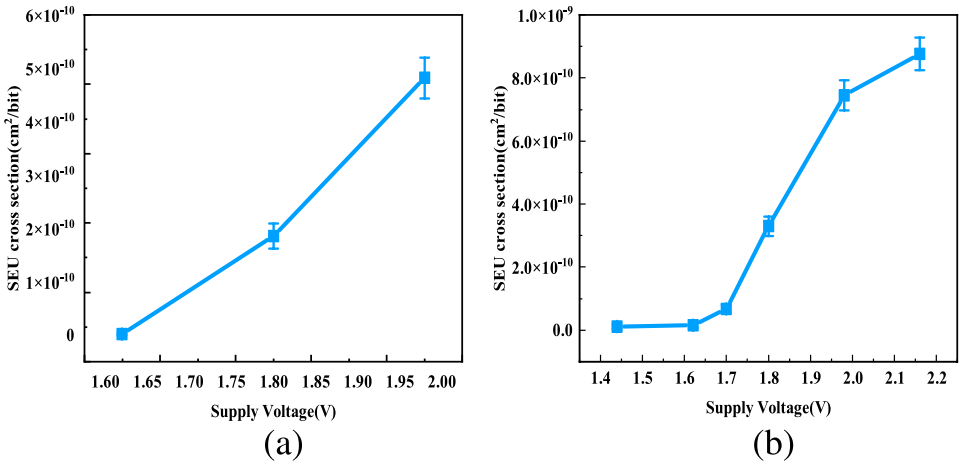

Fig. 2 (Color online) **a** Variation in the SEU cross section with supply voltage for LET = 86.1 MeV · cm^2/mg. **b** Variation in SEU cross section with supply voltage for LET = 87.3 MeV · cm^2/mg

remained significantly lower than the SEU cross section observed at the nominal voltage.

For V_{DD} exceeding 1.71 V, the SEU cross section experienced a rapid escalation with increase in supply voltage, reaching a plateau after a pull-up of 10%. We posit that the supply voltage range from a 5% pull-down to a 10% pull-up constituted the interval in which the width of the space-charge region underwent a significant variation in response to voltage changes. Within this range, any alteration in the supply voltage significantly affected the capability of the device to collect unbalanced carriers. However, when V_{DD} surpassed 1.98 V, the width of the space-charge region ceased to vary significantly. This stabilization was attributed to the power function relationship governing the width of the space-charge region with a reverse bias voltage.

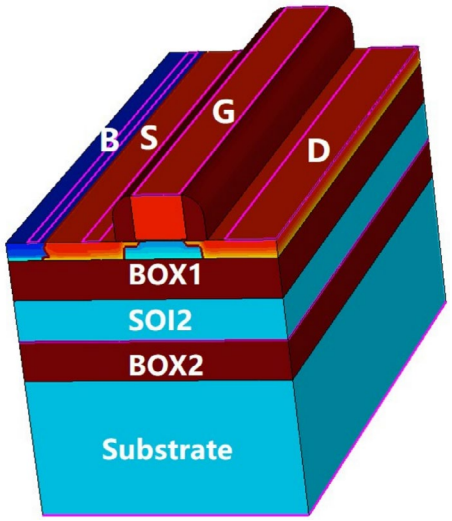

Fig. 3 (Color online) CSOI Device Models

4 SEU simulation and discussion

4.1 TCAD physical model setting

To achieve a comprehensive understanding of the mechanisms driving the observed experimental phenomena, we employed TCAD semiconductor device-simulation software to develop a CSOI model. After parameter calibration, we utilized SDEVICE to construct a 6T-SRAM for the CSOI process. This section presents an investigation of the relationship between the SEE and parameters such as the heavy-ion incidence position, back-gate voltage, and supply voltage to elucidate the phenomena detailed in Sect. 3.

Figure 3 depicts the CSOI device model developed for this simulation. The SRAM core memory cell comprised two pairs of input and output cross-coupled inverters (N1, P1; N2, P2). In the stable storage state of the cell, the word line was maintained at a low level, causing the transmission transistors N3 and N4 to be in the off state. Consequently, the n0 node stored datum "1", whereas the n1 node stored data "0".

Heavy-ion incidence was modeled by incorporating lateral diffusion via a Gaussian distribution with a trajectory radius of 0.015 μm. Given the significant generation of carriers due to SEEs, mechanisms, including Fermi–Dirac statistics [30] as well as Shockley–Read–Hall (SRH) and Auger recombinations [31] (indirect and Russo–Cherese composites), were incorporated into the simulation.

$$R_{\text{net}}^{\text{SRH}} = \frac{np - n_{i,\text{eff}}^2}{\tau_{\text{p}}(n + n_1) + \tau_{\text{n}}(p + p_1)} \tag{2}$$

Carrier transport was resolved through the application of a hydrodynamic model, which entails the concurrent coupling of the electron and hole temperature equations. The Philips unified model (PhuMob) was employed to consider the collective influence of phonon scattering, inter-carrier scattering, and ionizing impurity scattering on mobility [32].

$$\frac{1}{\mu_{i,\text{b}}} = \frac{1}{\mu_{i,\text{L}}} + \frac{1}{\mu_{i,\text{D}}} \tag{3}$$

The Enormal model incorporates the impact of the electric field perpendicular to the interface on mobility. The high-field velocity saturation mobility model (HighFieldSaturation model) integrates the correlation between the mobility and the electric field force, along with the saturation velocity [33]. Moreover, a resistive contact model was implemented at the source and drain terminals. Through introducing a distributed resistor (DistResist) between the contact and silicon surface of the device body, an external voltage induced a voltage drop across the resistive contact, thereby enhancing the realism of the device model.

4.2 Susceptibility of SEUs to the incidence position of heavy-ion

The simulation results indicated that the off-state transistor exhibited the highest sensitivity to SEUs, as shown in Fig. 4. In this state, electrons generated by heavy ions within the off-state NMOS channel swiftly migrated toward the drain owing to the carrier-collecting effect and bipolar amplification effect facilitated by the drain PN junctions. Consequently, the peak SET current reached its maximum magnitude. Conversely, in the transmission state, the source and drain terminals were biased, rendering them unable to establish a potential difference in the carrier drift. Consequently, only a minimal number of carriers migrated to

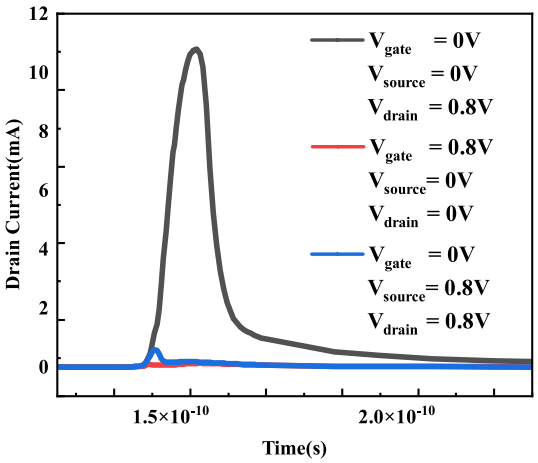

Fig. 4 (Color online) Dependence of SEEs on the device state. Supply voltage = 1.8 V, heavy-ion incidence location at the drain PN junction, LET = 86.1 MeV · cm^2/mg

the source and drain terminals concurrently owing to the diffusion motion, resulting in a significantly reduced SET current compared with the off state. In the open state, the electric potential difference between the source and drain was zero, impeding the drain from efficiently collecting the electron–hole pairs generated by the channel. Hence, the on-state NMOS transistor exhibited the lowest sensitivity to SEUs.

Figure 5a depicts the charge collected at the drain end of the device when heavy ions impinged vertically on the off-state NMOS and PMOS of the SRAM at various positions. The findings indicated that the sensitive region of the SRAM was at the drain–gate PN (D-G) junction of the off-state transistor. Given the similarity in the physical mechanism of triggering SEEs for both off-state transistors, this study exclusively analyzed the NMOS transistor.

As depicted in Fig. 5b, compared with other regions within the body area, the depletion region of the D-G junction in the off-state MOS exhibited the highest electric field strength. Consequently, the device achieved the highest efficiency in collecting carriers generated by heavy ions incident on the D-G junction. Consequently, the resulting current pulse from the heavy ions impacting this region demonstrated the shortest peaking time and accumulated the most charge. Conversely, when the incident position lay within the source region, the carrier drift motion was required to overcome the potential barriers of both the source–gate (S-G) and D-G junctions for collection by the drain electrode. Consequently, the source electrode exhibited the lowest sensitivity to SEEs, with only a fraction of carriers generated by heavy-ion ionization undergoing drift motion. Instead, the majority contributed to a diffusion current driven by concentration gradients, characterized by an SET pulse current featuring a small peak but a significant tail current.

Conversely, owing to their higher electron mobility compared with that of holes, electrons are more readily collected by the drain, resulting in the generation of a pulse current. Consequently, the SEE sensitivity of NMOS, in which electrons constitute the majority carriers in the source–drain, surpasses that of PMOS. This discrepancy is evident in Fig. 5(a), where the peak charge collected by NMOS exceeded that collected by the PMOS.

Furthermore, as depicted in Fig. 6a, to elucidate the mechanism of heavy-ion impact on transistor-level devices and subsequently analyze the effect of back-gate voltage on the SEU cross section, we simulated the electrostatic potential of the devices at three distinct moments: before (T1), during (T2), and after (T3) heavy-ion incidence. Figure 6b shows that heavy ions with sufficient LET striking the sensitive region of an NMOS transistor generated a significant number of carriers within the device. Electrons were predominantly collected by the drain, thereby reducing the drain potential, whereas the accumulation of holes after electron excitation increased the body potential. This reduction in the

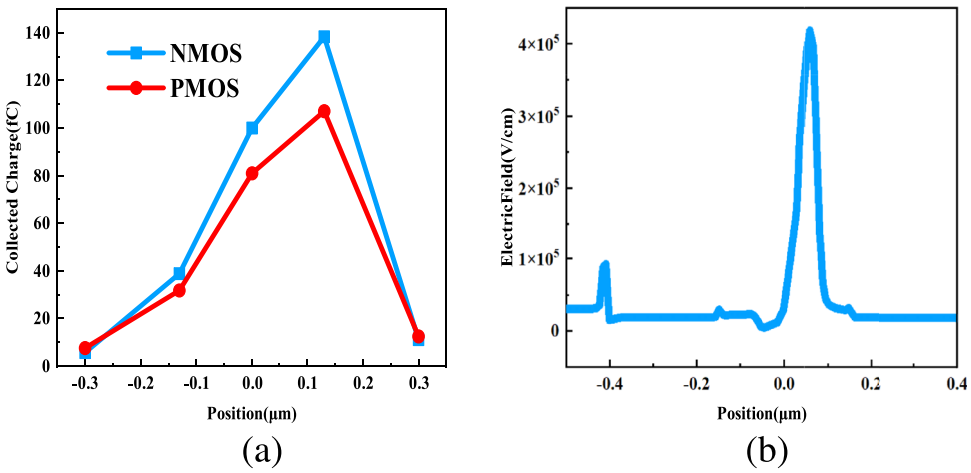

Fig. 5 (Color online) **a** Number of charges collected by the device when heavy ions hit different locations of the CSOI NMOS and PMOS. Supply voltage = 1.8 V, heavy-ion LET = 86.1 MeV · cm^2/mg. **b** Electric field strength at different positions of CSOI NMOS before heavy-ion incidence

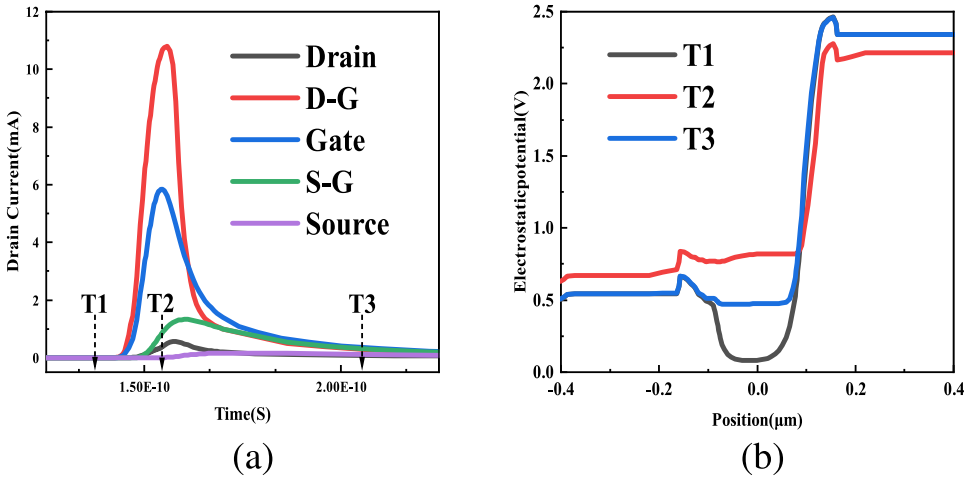

Fig. 6 (Color online) **a** Dependence of SET on particle incidence position. Supply voltage 1.8 V, heavy ions were all vertically incident, LET = 86.1 MeV · cm^2/mg. **b** Simulated electrostatic potentials at different times in Figure (**a**); the results are shown in a one-dimensional cross section along the source–drain axis of the device

potential barrier between the body and source–drain induced a zero or even positive bias in the base–emitter junction of the parasitic bipolar transistor, thereby instigating a bipolar amplification effect that augmented the pulse current.

4.3 Relationship between SEU occurrence and back-gate bias

Figure 7a and b illustrates the variations in the cross-sectional potential distributions with the back-gate bias for NMOS and PMOS transistors after heavy-ion incidence, respectively. As $|V_{nsoi}|$ and $|V_{psoi}|$ increased, the drain barrier height increased, making it more challenging for electrons to traverse the D-G barrier and reach the drain. Consequently, fewer carriers were collected at the drain of the off-state MOS, thereby attenuating the parasitic bipolar amplification effect and decreasing the SEE sensitivity of the device. This augmented the self-recovery capability of the SRAM and elevated the LET threshold.

Figure 8 shows the relationship between the collected charge and back-gate bias. As $|V_{soi}|$ increased from 0 to 10 V, the NMOS collected charge decreased by 2.22%, and the number of SEUs in the experiment decreased by 94.24%. The PMOS collected charge decreased by 0.43%, and the number of SEU in the experiment decreased by 83.78%. This observation supported the experimental finding that the inhibition of SEUs was more pronounced with V_{nsoi} than with V_{psoi}.

In addition, when analyzing the experimental data, we observed that the device exhibited the most significant charge reduction when the absolute value of $|V_{soi}|$ increased from 0 to 2 V. The slopes of the curves in Fig. 1a and b are 5.24×10^{-11} $cm^2/(bit \cdot V)$ and 4.48×10^{-11} $cm^2/(bit \cdot V)$, respectively, which were the highest among all the ranges. This suggests that this voltage level offered the highest

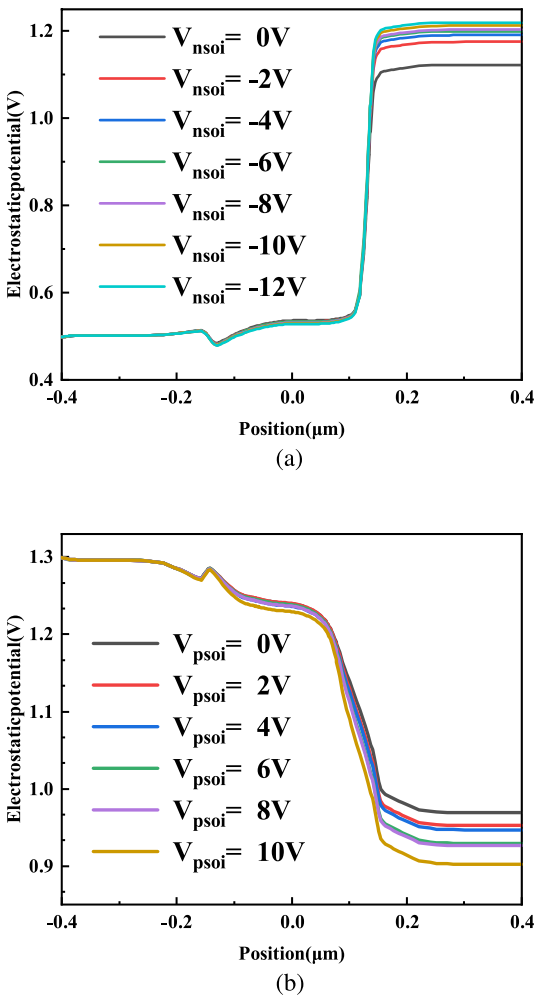

Fig. 7 (Color online) **a** NMOS potential distribution after heavy-ion incidence. **b** PMOS potential distribution after heavy-ion incidence. The supply voltage was 1.8 V. The heavy ions were all incident perpendicularly on the drain junction with LET = 86.1 MeV · cm^2/mg

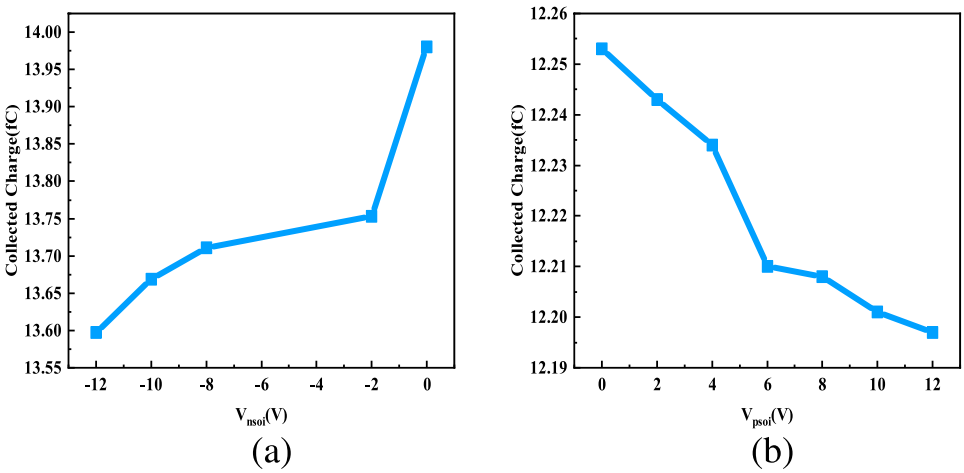

Fig. 8 (Color online) **a** Collected charge of off-state NMOS in SRAM cells at different V_{nsoi} values. **b** Collected charge of off-state PMOS at different V_{psoi} values. The supply voltage was 1.8 V. The heavy ions were all incident perpendicularly on the drain junction with LET = 86.1 MeV $\cdot$ cm^2/mg

rejection efficiency for SEU occurrences. Considering both the circuit power and SEU cross section, the back-gate bias combination of $V_{nsoi} = -2$ V and V_{psoi}=2 V was considered more suitable.

4.4 Impact of supply voltage on SEUs

Because the semiconductor power consumption is directly proportional to the square of the supply voltage, a viable strategy for minimizing power usage involves lowering the supply voltage. However, note that the susceptibility of the SRAM to SEUs is influenced by the supply voltage. Consequently, a comprehensive examination of the SEU sensitivity of CSOI-SRAM across various supply voltage levels must be conducted. The SRAM soft error rate is described by the following model [34]:

$$\mathrm{SER} \propto F \times A \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{Coll}}}\right) \tag{4}$$

where F is the particle fluence in particles/(cm^2 $\cdot$ s), A is the area of the sensitive region of the particle incidence circuit in cm^2, and Q_{crit} and Q_{Coll} are the critical and collected charges in fC, respectively [35–37].

According to formula $Q_{\mathrm{crit}} \approx C_{\mathrm{n}} \cdot V_{\mathrm{DD}}$, as referenced in [38], the critical charge depends on the specific circuit and device attributes and is primarily influenced by the node capacitance and supply voltage. The minimum charge necessary for SEUs increases with higher supply voltages, reducing the transistor-sensitive volume owing to the augmented critical charge. This phenomenon, where an increase in the supply voltage results in a decrease in the SEU cross section by elevating the critical charge, is denoted as mechanism I in this paper.

In contrast, the collected charge (Q_{Coll}) is a strong function of the particle LET value and supply voltage, which characterizes the number of carriers collected at the drain during heavy-ion incidence [39]. For MOSFET devices, the depletion region thickness can be calculated using the following equation:

$$W = \left[\frac{2K_{\mathrm{s}}\varepsilon_0}{q}\left(\frac{N_{\mathrm{A}}+N_{\mathrm{D}}}{N_{\mathrm{A}}N_{\mathrm{D}}}\right)(V_{\mathrm{bi}}+V_{\mathrm{A}})\right]^{\frac{1}{2}} \tag{5}$$

where K_{s}denotes the semiconductor dielectric constant, ε_0 denotes the vacuum dielectric constant, q denotes the electronic charge, V_{A} and V_{D} denote the acceptor and donor doping concentrations, respectively, and V_{bi} and V_{A} denote the semiconductor built-in and applied voltages at the drain junction, respectively. V_{bi} is calculated as follows:

$$V_{\mathrm{bi}} = \frac{kT}{q}\ln\left(\frac{N_{\mathrm{A}}N_{\mathrm{D}}}{n_i^2}\right) \tag{6}$$

The thickness of the depletion region is directly proportional to the supply voltage. This relationship implies that as the supply voltage increases, both the electric field density within the transistor and the volume susceptible to depletion increase. Consequently, the charge collected by the nodes increases. Figure 9 presents the current density in the NMOS drain region at various bias voltages. The supply voltage plays a significant role in shaping the characteristics of the PN junction depletion layer. Specifically, a higher voltage bias in the off-state NMOS drain results in a more pronounced electric field within the depletion region, enhancing the ability of the drain to collect drifting carriers. The peak node pulse current is primarily determined by the carrier drift. Therefore, an increase in the supply voltage intensifies the drift motion, resulting in an increase in the peak pulse current.

In the low-core voltage state, the limited number of holes generated in the body region by low-LET heavy ions fails to effectively diminish the source–body potential

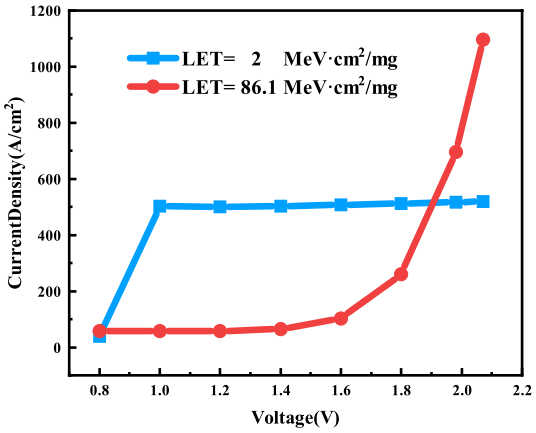

Fig. 9 (Color online) Effect of supply voltage on the depletion-layer current density. Supply voltage 1.8 V, heavy-ion incidence location at the drain PN junction of the off-state NMOS in SRAM cells

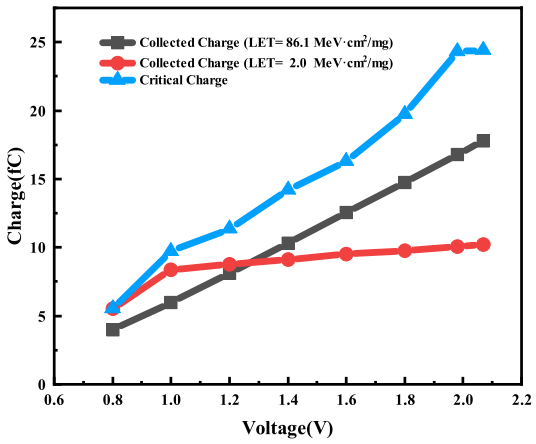

Fig. 10 (Color online) Variation in collected charge and critical charge with supply voltage was investigated for different LET values for heavy ions vertically incident on the drain junction of off-state NMOS in SRAM cells

barrier. Consequently, these holes are unable to traverse the depletion region between the source and body and are released through the ground. The accumulation of holes in the body region elevates the electric potential, prompting a significant flow of electrons to be collected by the drain through the depletion region between the drain and body. Conversely, heavy ions with high LET values generate a significant number of carriers, which significantly reduces the potential barriers between the source and body. Thus, most of the holes generated in the body region by these heavy ions cross the depletion region between the source and body and are released to the ground. This lowers the electric potential of the body region, suppresses the bipolar amplification effect, and results in partial electron collection by the drain. Therefore, in the low-voltage state, the current density produced by heavy ions with high LET values is lower than that produced by heavy ions with low LET values.

In the high-core-voltage state, the drain-depletion region extends sufficiently to collect almost all the electrons generated by the low-LET heavy ions, causing the current density from these ions to saturate after the core voltage increases to 1.0 V. As the core voltage increases, the width of the drain–body depletion region expands, enhancing the electron collection efficiency of the drain. Simultaneously, the elevated drain voltage increased the electric potential of the body region, thereby strengthening the bipolar amplification effect. Consequently, the current density from heavy ions with high LET values increases rapidly with core voltage. In the high-voltage state, the current density from high-LET heavy ions surpasses that from low-LET heavy ions.

The physical process of widening the drain-junction depletion region owing to an increase in the supply voltage, as discussed in [40], results in the enlargement of the SEU cross section. This phenomenon is referred to as mechanism II in this paper.

Figure 10 shows that for low-LET heavy-ion incidence, Q_{crit} and Q_{Coll} increased with the supply voltage. However, the number of carriers generated by heavy ions of a specific LET value remained constant and was unaffected by variations in V_{DD}. The depletion region expanded sufficiently to capture the excited carriers when the supply voltage exceeded 1 V. Therefore, when the increase in V_{DD} allowed the drain-depletion region to gather the majority of carriers, the magnitude of the change in Q_{crit} and Q_{Coll} with respect to V_{DD} resulted in a notable disparity. This was evidenced by the increase in Q_{crit} surpassing the increase in Q_{Coll}. During this phase, mechanism I prevailed, resulting in a decrease in the SEU cross section with an increase in the supply voltage.

However, for high-LET heavy-ion incidence, as shown in Fig. 10, because of its capacity to deposit a greater amount of energy in the sensitive region of the device, the excitation carriers were not entirely collected by the depletion layer at a voltage of V_{DD} of 1.98 V. The collected charge increased rapidly with increase in V_{DD}. At this juncture, mechanism II was dominant.

During the competition between the two mechanisms mentioned above, the notable increase in the SEU cross section of CSOI-SRAM under Ta-ion irradiation with increase in supply voltage can be attributed to the increase in the depletion-layer thickness and the parasitic bipolar current induced by the increasing V_{DD}. Although mechanism II prevailed in this 0.18 μm node test and simulation, the conflicting influences of mechanisms I and II in small-node technology and low-core voltage scenarios merit further comprehensive investigation.

5 Conclusion

The experimental results demonstrated that both negative N-type and positive P-type transistor back-gate biases can effectively enhance the SEU resistance of an SRAM memory cell. Moreover, we observed that the impact of V_{nsoi} is superior to that of V_{psoi} when subjected to the same bias voltage magnitude. Maintaining the absolute value of $|V_{soi}|$ between 2 and 6 V not only ensures low power consumption of the circuit but also aids in suppressing SEU occurrences. Through TCAD simulations, this study investigates the sensitive location of the CSOI-SRAM and explored the influence of back-gate bias and supply voltage on the SEE sensitivity of the SRAM. For a specific range and LET value of heavy-ion incidence, we observed that the drain–body potential difference of the NMOS device increased with back-gate bias. This increase results in an increase in the barrier height between the body and source–drain, consequently suppressing the parasitic bipolar amplification effect and reducing the SEU cross section of the CSOI-SRAM.

In the context of SRAM, we observed that two competing mechanisms exist for SEU occurrence. First, an increase in the supply voltage results in an escalation of the critical charge and a reduction in the circuit-sensitive volume. Second, an increase in the supply voltage widens the depletion region, resulting in an augmentation in the device's collected charge and sensitive volume. In most cases, these two mechanisms coexist and compete, potentially resulting in varying competitive outcomes. Specific process nodes and LET values have crucial roles in determining the nature of the competition. Thoroughly evaluating the SEU cross section at various LET values and core voltages and conducting bias experiments to determine the worst-case scenario for SRAM performance during ground testing are crucial. Neglecting to consider these factors may result in an underestimation of the circuit SEU cross section.

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Author contributions All authors contributed to the study conception and design. Material preparation, data collection, and analysis were performed by Li-Wen Yao, Jin-Hu Yang, and Pei-Xiong Zhao. The first draft of the manuscript was written by Li-Wen Yao and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data availability The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.j00186.00657 and https://www.doi.org/10.57760/sciencedb.j00186.00657.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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