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Low-noise and high-rate front-end ASIC for APD detectors in STCF ECAL

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Abstract

This study presents a low-noise, high-rate front-end readout application-specific integrated circuit (ASIC) designed for the electromagnetic calorimeter (ECAL) of the Super Tau-Charm Facility (STCF). To address the high background-count rate in the STCF ECAL, the temporal features of signals are analyzed node-by-node along the chain of the analog front-end circuit. Then, the system is optimized to mitigate the pile-up effects and elevate the count rate to megahertz levels. First, a charge-sensitive amplifier (CSA) with a fast reset path is developed, enabling quick resetting when the output reaches the maximum amplitude. This prevents the CSA from entering a pulse-dead zone owing to amplifier saturation caused by the pile-up. Second, a high-order shaper with baseline holder circuits is improved to enhance the anti-pile-up capability while maintaining an effective noise-filtering performance. Third, a high-speed peak-detection and hold circuit with an asynchronous first-input-first-output buffer function is proposed to hold and read the piled-up signals of the shaper. The ASIC is designed and manufactured using a standard commercial 1P6M 0.18 μm mixed-signal CMOS process with a chip area of 2.4 mm × 1.6 mm. The measurement results demonstrate a dynamic range of 4–500 fC with a nonlinearity error below 1.5%. For periodically distributed input signals, a count rate of 1.5 MHz/Ch is achieved with a peak time of 360 ns, resulting in an equivalent noise charge (ENC) of 2500 e^-. The maximum count rate is 4 MHz/Ch at a peak time of 120 ns. At a peak time of 1.68 μs with a 270 pF external capacitance, the minimum ENC is 1966 e^-, and the noise slope is 3.08 e^-/pF. The timing resolution is better than 125 ps at an input charge of 200 fC. The power consumption is 35 mW/Ch.

Keywords Readout electronics · APD · Charge measurement · High count rate · STCF

1 Introduction

The Super Tau-Charm Facility (STCF) is important for accelerator-based particle physics, after the Beijing electron–positron collider II (BEPC-II) in China, and it has been proposed for the search for new physics beyond the standard model (SM) in the tau-charm energy region with a luminosity higher than 0.5×10^{35} $cm^{-2}s^{-1}$ [1]. Compared to BEPC-II, the luminosity of the STCF experiment is 100 times higher, resulting in a proportional increase in the event rate of its physical processes. An electromagnetic calorimeter (ECAL), an important component of STCF detectors, is utilized to measure the energy of particles with high efficiency and resolution. Based on related studies and simulation results, the physical-event rate incident on the STCF ECAL is expected to reach 400 kHz. Moreover, owing to the high luminosity and narrow beam design of STCFs, the estimation and suppression of background events have become

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critical issues. The background events encountered by the STCF ECAL were studied using Monte Carlo simulations, and the simulation results indicated that the background-count rate measured by the ECAL was as high as 1 MHz [2]. In response to the high count rates resulting from the ultrahigh luminosity of the STCF experiment, pure cesium iodide (pCsI) was chosen as the scintillation crystal for the ECAL because of its fast response and excellent radiation resistance. To compensate for the lower yield of pCsI, large-area avalanche photodiodes (APDs) with internal gains have been selected as photodetector devices for the ECAL [3, 4]. The detection unit, composed of pCsI and the APD, cannot inherently distinguish between the particles produced by the background and those produced by the targeted physical processes. Therefore, the count rate of the front-end readout circuit needs to account for the background events.

A charge-sensitive amplifier (CSA) is the most accurate preamplifier structure for charge measurements; thus, it is particularly well suited for calorimeters aiming for high-energy resolution [5–14]. The structure of analog readout circuits based on the low-noise CSA is shown in Fig. 1, where the detectors and readout circuits are AC coupled. The accumulation of signals presents a significant challenge for analog front-end readout circuits operating at high event rates. The factors limiting the circuit count rate include the decay time (T_d) of the detector output-pulse current, rise time (t_{rise}) and reset time (t_{rst}) of the CSA, type and peak time (PT) of the filtering shaper, storage depth and dead time of the peak detect and hold circuit (PDH), and sampling rate of the analog-to-digital converter (ADC). For a selected detector, the pulse-current signal decay time is determined; for example, the luminous decay time of the pCsI scintillator selected for the STCF ECAL is approximately 30ns. Therefore, the targeted optimization of the CSA, shaper, and PDH circuits is essential in the design of a high-rate analog front-end readout ASIC to reduce the probability and impact of pulse pile-up, thereby increasing the event throughput of the front-end readout circuit [15–21].

In our previous work, we developed two low-noise readout ASICs, SECALROC1 and SECALROC2, to achieve high-precision energy and time measurements [12, 13]. The ASICs were optimized for a count rate of 400 kHz. However, the count rate of the front-end readout circuit must be further improved considering the background events. In this study, we present SECALROC3, a low-noise and high-rate front-end readout ASIC specifically designed for the STCF ECAL. Leveraging the characteristics of signals that can be piled up to a certain extent, we devised a CSA with a fast reset path, high-order shaper with a baseline holder circuit, and high-speed PDH circuit with asynchronous first-input-first-output buffering capability. This circuit enables the detection of piled-up signals from the shaper output, ensuring accurate identification, even in situations with signals that are moderately piled-up. The proposed ASIC minimizes the effect of piled-up signals and achieves a counting rate of several megahertz per channel.

The remainder of this paper is organized as follows. In Sect. 2, details of the ASIC architecture and circuit design are reviewed. Experimental results are presented and discussed in Sect. 3. Finally, a summary of the study is provided in Sect. 4.

2 ASIC architecture and circuit design

A block diagram of SECALROC3 is shown in Fig. 2. The proposed ASIC comprises six readout channels, including two dummy channels, a bandgap reference, bias circuits, a multiplexer, a single-ended to differential drive buffer, and a time-triggered signal buffer. Each channel is composed of a low-noise CSA, a saturation-detection circuit, a fast-reset control circuit, an energy branch for measuring the input charge, and a time branch for measuring the time of arrival (TOA). The energy branch includes a pole-zero cancellation circuit, high-order shaper with a baseline holder (BLH) circuit, and PDH circuit. A pole-zero cancellation circuit can eliminate the undershoot of the shaper output and decrease the signal width [16, 22]. The BLH is used to stabilize the output baseline by establishing a low-frequency feedback loop for the shaping circuits without introducing extra noise or instabilities. The PDH circuit is used to detect the peak value of the output signal and obtain a nearly flat-topped signal, which preserves the peak-amplitude information for a longer duration, enabling the ADC to perform its conversion with a more relaxed timing performance or perform multiple readings on the same input signal. The time branch is composed of a fast shaper, discriminator,

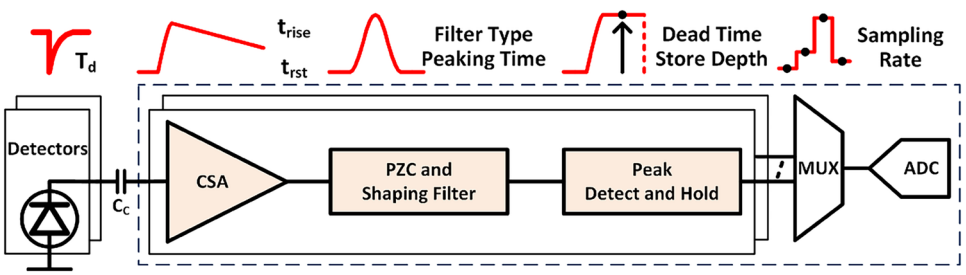


Fig. 1 (Color online) Block diagram of the analog front-end readout electronics

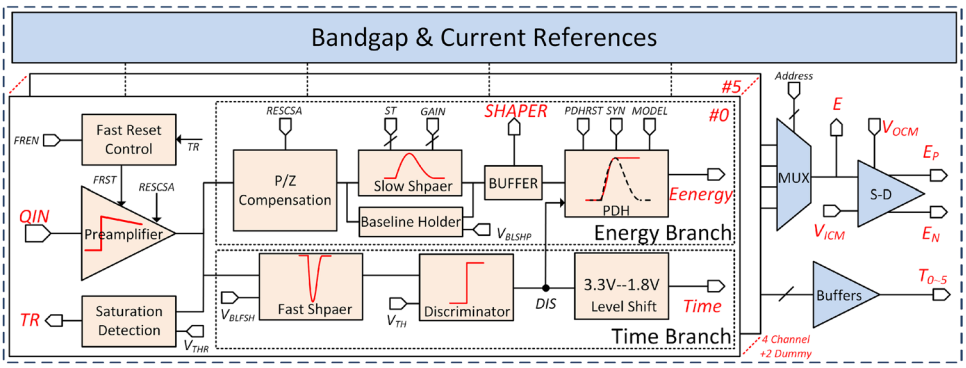


Fig. 2 (Color online) Block diagram illustrating the ASIC architecture

and level shifter. The fast shaper is used to decrease the signal width and increase the count rate of the time channel [23, 24]. A hysteresis comparator is used to generate a pulse signal, and the output pulse leading-edge indicates the TOA. The level shifter can shift the 3.3 V pulse signal to 1.8 V to match the power supply of the time-to-digital converter [12].

2.1 Charge-sensitive amplifier with fast-reset circuit

To maximize the coverage of the outer surface of the pCsI crystal and capture more fluorescence, the STCF ECAL used APD detectors (S8664-1010, Hamamatsu, Japan) with a large sensitive area of 10 mm × 10 mm. However, the substantial sensitive area of the APD introduces challenges to the front-end readout circuit in terms of noise and speed-performance optimization, because of its large detector capacitance (typically $C_D = 270$ pF) and leakage current (typically $I_D = 10$ nA). The equivalent noise charge (ENC) was calculated using Eq. (1). The ENC contributions due to the current parallel, thermal, and flicker noises are expressed in (2), (3), and (4), respectively [25].

$$ENC_t = \sqrt{ENC_i^2 + ENC_w^2 + ENC_f^2} \tag{1}$$

$$ENC_i^2 = \left(\frac{4kT}{R_f} + 2qI_D\right) \cdot \frac{t_p}{q^2} \cdot N_s \tag{2}$$

$$ENC_w^2 = \frac{4kT\gamma}{g_{m0}} \cdot \frac{(C_D + C_f + C_P)^2}{q^2 t_p} \cdot N_w \tag{3}$$

$$ENC_f^2 = \frac{K_{1/f}}{C_{ox}WL} \cdot \frac{(C_D + C_f + C_P)^2}{q^2} \cdot N_f, \tag{4}$$

where R_f is the feedback resistance of the CSA (implemented by an n-MOSFET working in the subthreshold region), I_D is the leakage current of the APD, t_p is the peaking time of the shaper, g_{m0} is the transconductance of the input transistor M_0, W and L are the width and length of the input transistor M_0, respectively, C_D is the capacitance of the APD detector, C_f is the feedback capacitor of the CSA, and C_P is the parasitic capacitance excluding C_D at the CSA input node. The parasitic capacitance C_P is proportional to W and L. γ and $K_{1/f}$ are the thermal and flicker noise coefficients, respectively. N_s, N_w, and N_f are constants for parameter n of the shaper. To mitigate the impact of a large capacitance on the readout circuit, a high-gain, wide-bandwidth, low-noise, single-ended input split-leg cascade amplifier with dual common-gate stages is proposed [12, 13]. The input NMOS is optimized to operate in the moderate-inversion region (between strong and weak inversion) with a gate length (L) of 1 μm, gate width (W) of 16 mm (20 μm × 800 fingers), and bias current of 8.2 mA to achieve a high transconductance ($g_{m0} = 125$ mS) for reduced thermal noise [26].

As the input-current pulses accumulate charge on feedback capacitor C_f, the output voltage of the CSA gradually increases, eventually leading to saturation. To prevent the saturation of the amplifier and provide a stable DC operating point, a reset block must be connected in parallel to the feedback capacitor C_f. Two basic techniques have been implemented to discharge the feedback capacitance: switch reset and continuous discharge [15, 27]. The switch-reset technique discharges the feedback capacitor by periodically opening a switch. The disadvantages of this solution are sampled noise and charge injection from the switch transistor. Additionally, each reset of the CSA introduces a negative signal to the shaper, thereby increasing the dead time of the readout circuits. Although a resettable shaper structure can overcome this negative signal, it increases the complexity of the system [17].

The continuous-discharge technique can be applied using a resistor (or an equivalent circuit) parallel to C_f to achieve continuous discharge of the accumulated charge [28]. The output waveform of the CSA in this mode is shown in Fig. 3. The rise time t_{rise} is affected by two factors: T_d and T_{GBP}. The time constant T_{GBP} depends on the gain-bandwidth product (GBP) of the core amplifier [13]. The value of the feedback resistor (R_f) must be sufficiently large to reduce ballistic

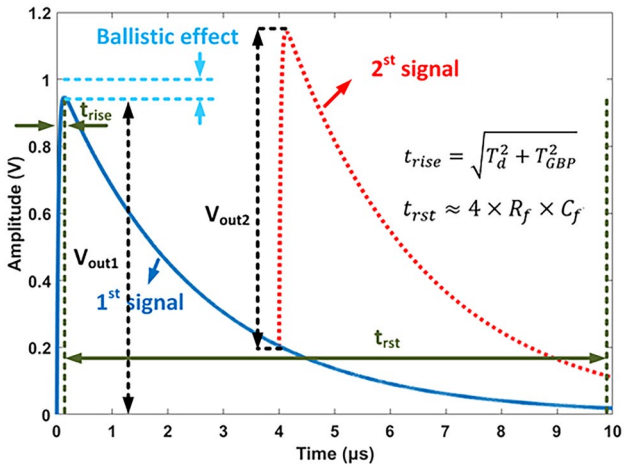


Fig. 3 (Color online) Charge-sensitive amplifier output-signal waveforms and associated time parameters

deficit effects and simultaneously minimize the impact of its parallel noise. Typically, an MOS transistor operating in a triode or saturation region is employed as the feedback resistor. This is a compact solution that may enable the control of feedback resistance; however, nonlinear effects must be considered. The long decay-time constant ($\tau_f = R_f \times C_f$) of the preamplifier output signal imposes limitations on the count rate owing to pulse pile-ups. When the resistance value of the feedback resistor R_f is reduced to decrease the CSA reset time t_{rst} (approximately $4\tau_f$), the impact of the ballistic deficit and noise contribution from the feedback resistor R_f becomes non-negligible, affecting the overall noise performance of the circuit. Therefore, a compromise between noise and count rate is necessary in the design of R_f.

The energy distribution of the background events for the STCF ECAL is predominantly concentrated in the low-energy region below 1 MeV [2]. The magnitude of the event pulses was comparable to the equivalent noise of the front-end readout circuit. Thus, the influence of these background events manifests as an increase in the CSA output baseline, and the readout circuit cannot effectively detect these events. The event rate for higher-energy background events (≥ 10 MeV) is significantly reduced [2]. According to the energy distribution and average event rate (Poisson distribution) of the background events, the probability that background events of different energies occur in a 700 ns signal waveform can be estimated. For a barrel ECAL, the probability of more than one event greater than a 10 MeV background event within a 700 ns waveform width is only approximately 0.6%. Therefore, we can assume that a physical event will have only one larger background signal piled-up with it. As shown in Fig. 3, the output signals of the CSA can be piled up to a certain extent; thus, the circuit-receivable event rate can be increased. In this design, we added a saturation-detection circuit and fast-reset circuit for the CSA. When the CSA output reaches a preset saturation level owing to the event pile-up, a fast reset is launched to prevent the circuit from entering dead time.

A block diagram of the proposed CSA is presented in Fig. 4a. The core amplifier comprises two output branches formed by two source followers. One output (EOUT) is connected to the energy-measurement channel. The other output (TOUT) is connected to the time-measurement channel. The continuous-reset feedback resistor R_f is positioned between the input and EOUT, interfacing with the subsequent pole-zero cancellation circuit. The feedback resistor R_f implemented using the NMOS transistor M_1 has a resistance value controlled by the voltage RESCSA, with an adjustable equivalent resistance ranging from approximately 0.3 MΩ to 60 MΩ. Under the condition $C_f = 500$ fF, the decay time required for the CSA to recover to the baseline ranges from approximately 0.6 μs to 120 μs.

The fast-reset feedback circuit is positioned between the input and TOUT to minimize its effect on the energy-channel signal. This circuit includes switch transistors M_2 and M_3, controlled by the FRST and NFRST (inverted signal of FRST) signals, along with a current-limiting resistor R_{sw}. The M_3 transistor is utilized to suppress the clock feedthrough and charge-injection effects induced by M_2. The resistor R_{sw} restricts the reset current during the fast-reset process, ensuring the stability of the CSA [15].

The saturation-detection circuit employs a hysteresis comparator that generates a corresponding pulse signal when the CSA output voltage exceeds a certain threshold (near the saturation level). The circuit for generating FRST is shown in Fig. 4b, incorporating the FREN signal to control the operation of the fast-reset circuit. When FREN=1, the TR is buffered and fed into a monostable circuit, producing a fixed-width (40 ns) pulse signal FRST (as well as NFRST) and completing the fast reset of the CSA. The fast-reset circuit operates only when the CSA is piled up near its maximum, and any detected events during the fast-reset operation are discarded to guarantee the noise performance of the circuit.

2.2 High-order shaper with baseline holder circuit

In high-count-rate applications, the theoretically optimal peak time often falls short of meeting the count-rate requirements. In such scenarios, the noise performance with the count rate must be compromised by employing a small adjustable peak time. For example, in our study, the theoretically optimal peak time ranges from 0.51 μs to 2.58 μs (varying with the detector-leakage current and noise contribution from the feedback resistor R_f). However, to satisfy the count-rate requirement of 1.5 MHz, the maximum peak time is set to 204 ns (choosing a shaper order of $n = 6$). In addition to

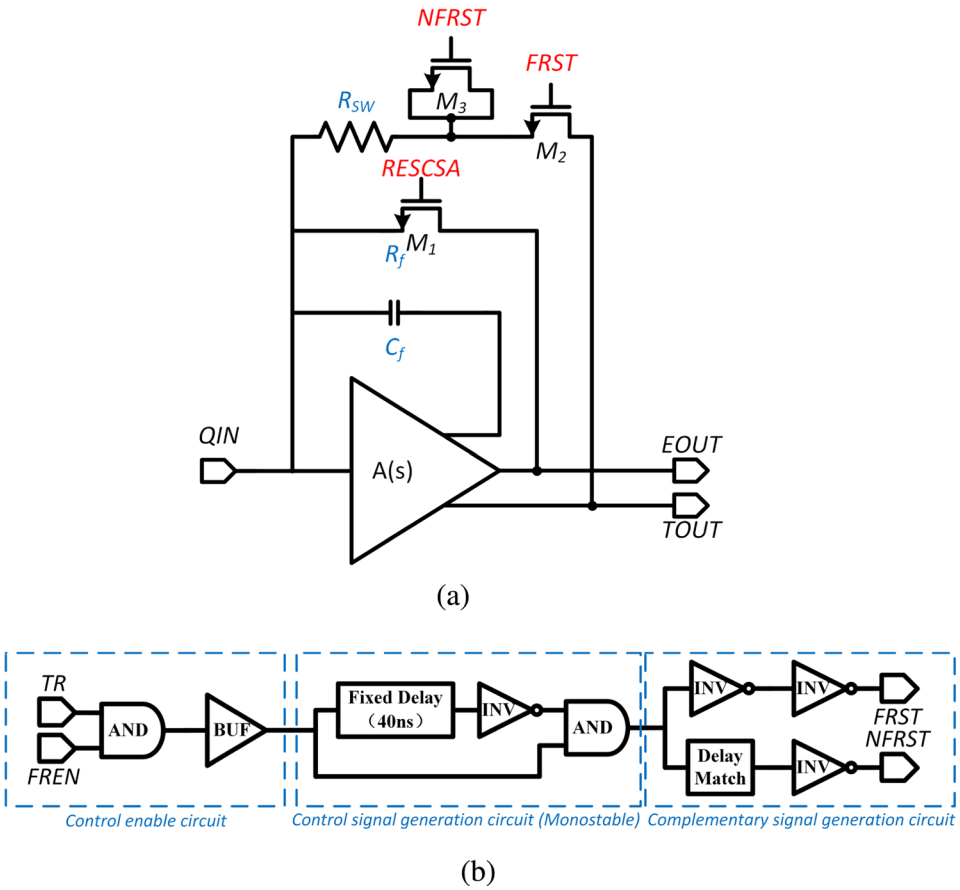
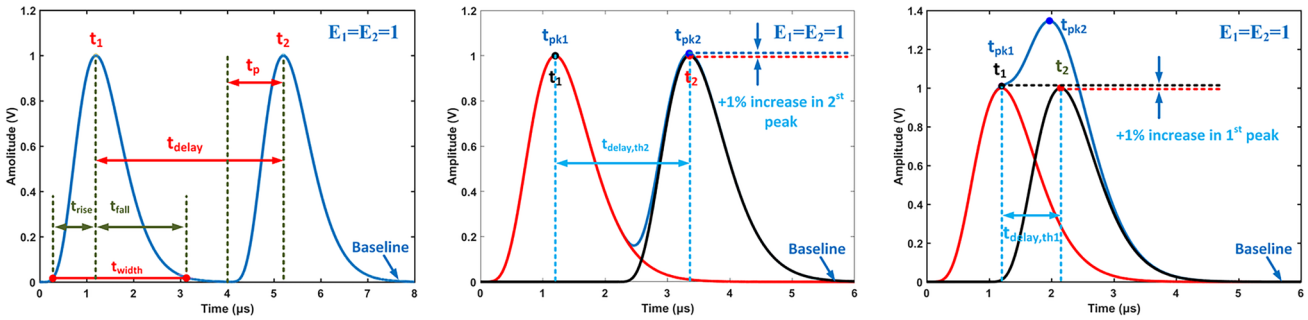


Fig. 4 (Color online) (**a**) Block diagram of the proposed charge-sensitive amplifier, (**b**) block diagram illustrating the fast-reset control circuit

reducing the peak time, similar to the output signals of the CSA, the shaper-output signals can also pile-up to a certain extent. Thus, the detection of piled-up signals offers a solution for meeting the higher count-rate requirements.

As depicted in Fig. 5a, the width of the shaper-output signal t_{width} is defined as the time range encompassing 1% to 1% of the maximum signal amplitude. The rise time t_{rise} represents the time required for the signal amplitude to increase from 1% to its peak, whereas the fall time t_{fall} represents the time required for the signal amplitude to decrease from its peak value to 1%. The rise t_{rise} and fall t_{fall} times primarily depend on the peak time t_{p} and the characteristics of the shaper (such as the number of real or complex poles). The peak-time points of the two signals are t_1 and t_2, respectively, and the time interval between them is denoted as t_{delay}.

Conventionally, readout circuits operate with $t_{\text{delay}} \geq t_{\text{width}}$, as shown in Fig. 5a. When $t_{\text{delay}} < t_{\text{width}}$, the phenomenon of signal pile-up can be observed. Two typical pile-up scenarios for shaper-output signals are illustrated in Fig. 5b and c. In both cases, the two input signals have equal charges



(a)Timing parameters of shaping amplifier (b)The condition in which both of two signals are valid (c)The condition in which the first signal is valid

Fig. 5 (Color online) Shaping-amplifier output-signal waveforms and associated time parameters

($E_1 = E_2$). t_1 and t_2 represent the peak time points when the two signals are inputted individually. t_{pk1} and t_{pk1} are the peak time points for the piled-up signal. Signals can still be considered effective when they increase by only 1% compared to the ideal peak-voltage amplitude. Thus, as shown in Fig. 5b, when $t_{delay} \geq t_{delay,th2} \approx t_{fall}$, the voltage amplitude of the piled-up signal at the peak point t_{pk1} is equal to the ideal peak-voltage amplitude. Additionally, the voltage amplitude of the piled-up signal at the peak point t_{pk1} increases by only 1% compared to the ideal peak-voltage amplitude because the tailing part of the first signal does not overlap with the peak of the second signal; both of the signals are considered effective. As shown in Fig. 5c, when $t_{delay} > t_{delay,th1} \approx t_{rise}$, the voltage amplitude of the piled-up signal at the peak point t_{pk1} increases by only 1% compared with the ideal peak-voltage amplitude because the leading part of the second signal does not overlap with the peak of the first signal, and the first signal can still be considered an effective signal. Note that when the two input signals have different charges, $t_{delay,th2}$ and $t_{delay,th1}$ change according to E_1/E_2 ratio [19]. Event timestamps can be obtained from the time channel; thus, t_{delay} between each signal is available. According to the time information, pile-up rejection (PUR) can be applied effectively in the back-end data-processing program to accept undistorted amplitudes and reject distorted amplitudes.

As shown in Fig. 6, the ratios of t_{width} to t_p and $t_{delay,th2}$ to t_p at $E_1 = E_2$ are depicted for different shaper orders. The values of t_{width}/t_p and $t_{delay,th2}/t_p$ decrease significantly as the order n of the shaper increases. However, for $n \geq 5$, the decreasing trend gradually slows, and the improvement is insignificant. This illustrates that higher-order shaper circuits are more suitable for high-count-rate applications. However, considering the noise performance, with a fixed shaper-output signal width of $t_{width} = 667$ ns corresponding to a count rate of

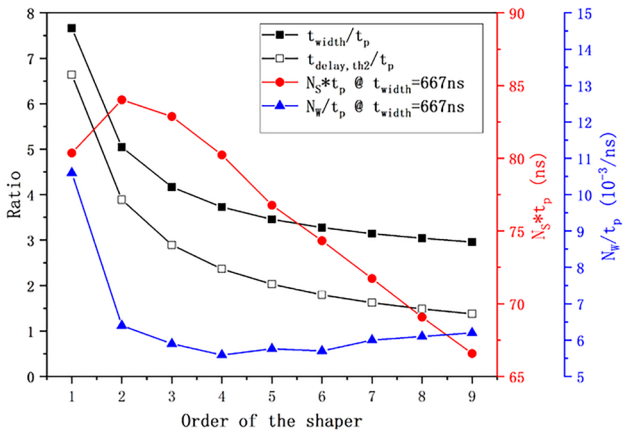
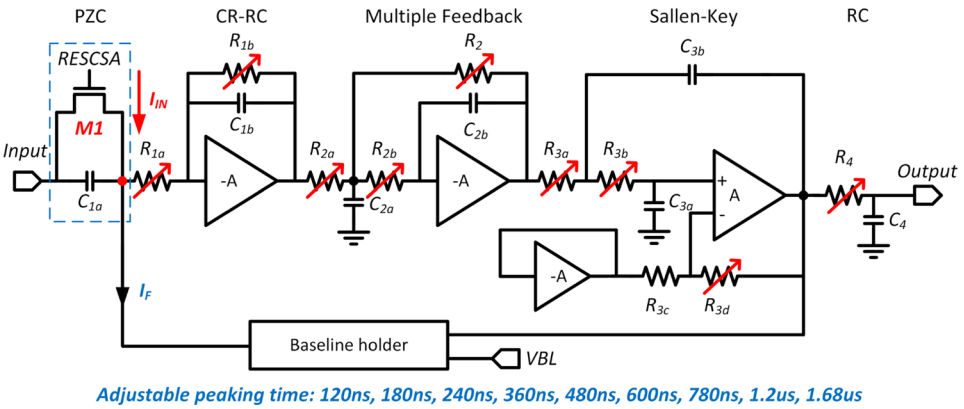


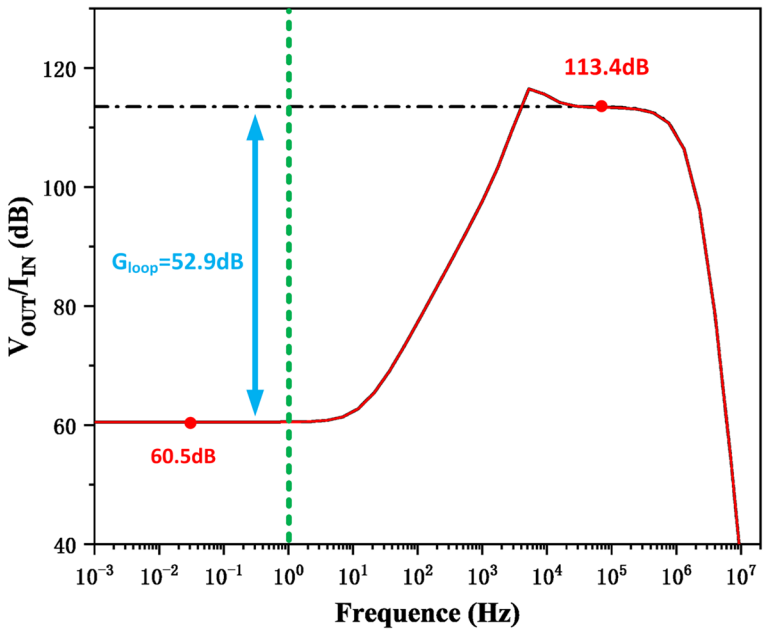
Fig. 6 (Color online) Ratio of output-signal width t_{width} to peak time t_p and ratio of input-signal interval t_{delay} to peak time t_p for different filter orders

1.5 MHz (periodically distributed input signals), the thermal-noise coefficient N_w/t_p exhibits a smaller value in the range $4 \leq n \leq 6$. The shot-noise coefficient $N_s \times t_p$ gradually decreases after $n \geq 2$. Thus, selecting a sixth-order shaper achieves noise optimization while meeting the high count-rate requirement. In this configuration, the ratio of the signal width to the peak time is approximately 3.28, and the ratio of the time interval between the input signals and peak time is approximately 1.8. For the count-rate requirement of 1.5 MHz, without considering the piling up of shaper-output signals, the maximum peak time is only 200 ns. However, allowing for the piling up of output signals, this shaper can extend the maximum peak time to 370 ns, thereby mitigating the degradation of noise performance.

The proposed CR − $(RC)^6$ semi-Gaussian high-order shaper is shown in Fig. 7a. The shaper is composed of a CR-RC filter, multiple feedback (MFB) filter, Sallen–Key (SK) filter, and an RC filter. The front-end readout circuit collects electrons, resulting in a positive output signal from the CSA, and subsequently produces a negative output signal in the CR-RC circuit. To guarantee a positive output signal and broaden the output range (with the baseline voltage established by the CSA and maintained at approximately 0.8 V), the second stage is identified as an MFB filter structure aimed at converting the signal output into a positive format. The SK filter is chosen for the third stage because of its properties as an in-phase proportional amplifier and its capacity for gain adjustment. The amplifiers for the CR-RC and MFB filters employ a single-ended input–output cascade structure similar to that of the CSA core amplifier, and the sizes of the individual transistors in the amplifier are carefully tailored to guarantee that the DC voltages of both the CSA and filters are nearly identical. In addition, utilizing an amplifier with an identical construction to supply a bias voltage at the negative terminal of the SK ensures that the DC voltages at both ends of the SK stage amplifier are balanced, thereby guaranteeing that the final output baseline remains stable around 0.8 V. The peak time is adjustable in this design and ranges from 120 ns to 1680 ns. A pole-zero cancellation (PZC) circuit is used to eliminate the undershoot of the shaper output and increase the event rate. The pole-zero cancellation resistor ($M1$) forms a DC path between the CSA and shaper. In the event of a pile-up of CSA output signals, a DC current I_{IN} flowing through the resistor network of the shaper induces a baseline drift in the output, impacting the amplitude-detection accuracy of the readout system. To address this issue, a BLH circuit is used to generate I_F to compensate for I_{IN}, thereby suppressing the baseline drift [29]. Figure 7b shows the transfer function of the BLH circuit during the operation (excluding M1 and C_{1a}). For effective signal frequencies, the gain is approximately 113.4 dB. For low-frequency signals (below 1 Hz), the gain is approximately 60.5 dB, representing a



(a)



(b)

Fig. 7 (Color online) (**a**) Simplified schematic of the CR – $(RC)^6$ shaper with baseline holder circuit. (**b**) Simulation results of the transfer function of the BLH-shaper closed-loop system (excluding M1 and C_{1a})

reduction of 52.9 dB in the low-frequency loop gain by the BLH circuit.

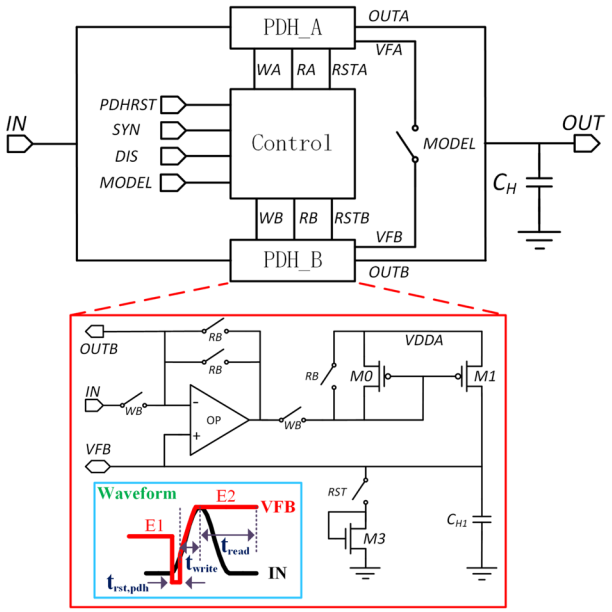
2.3 Peak-detection and holding circuit

The output signal of the shaper is connected to the PDH, which detects and holds the peak voltage of the signal. The choice and operation of the PDH influence the count rate and relate it to the operation of the PUR. Traditionally, the width of a PDH output signal consists of three parts: the writing time t_{write}, reading time t_{read}, and reset time $t_{\text{rst,pdh}}$. When only one PDH circuit is used, if a second signal with a higher (or lower) amplitude occurs in the same channel during the readout by the ADC, the first (or second) amplitude will be lost; therefore, at least two levels of storage depth are required for high-count-rate applications. Two different approaches are commonly used: resetting the PDH for a fixed time after peak detection, or keeping the PDH reset until the output of the shaper falls below a fixed threshold again. Both approaches have the probability to lose events, especially the piled-up signals of the shaper.

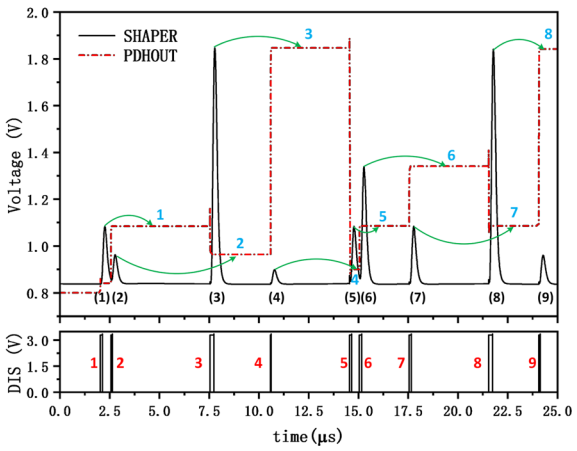
To enhance the event rate received by the PDH circuit, the storage depth must be increased and the dead time must be reduced. This study employs three strategies to minimize the dead time. First, two PDH submodules are employed to increase the storage depth. While one module operates during the writing interval, another operates during the reading interval. This ensures that one module is always waiting for the signal and the dead time introduced by the reading time t_{read} is eliminated. Second, the reset time $t_{\text{rst,pdh}}$ is concealed

within the peak time of the shaper, effectively eliminating the dead time caused by $t_{rst,pdh}$. Finally, the trigger signal from the time channel is utilized as a control signal, creating an event-driven analog memory. In this configuration, the PDH circuit exhibits minimal dead time for each detectable signal.

The proposed high-speed PDH circuit based on the aforementioned principles is illustrated in Fig. 8a. The circuit comprises two submodules, PDHA and PDHB, a control module, and a holding capacitor C_H. The PDHA and PDHB submodules employ peak-detection and holding circuits with a two-phase (read and write) configuration [30]. A folded cascade amplifier with a rail-to-rail input dynamic range is used in the PDH. The DC gain A_0 and DC common-mode rejection ratio (CMRR) and common-mode output reference $V_{o,cm}$ of the amplifier are optimized to improve the accuracy of the peak-height measurement of the PDH [31, 32]. PDHRST serves as an external reset signal, DIS represents the trigger signal from the time channel, and WA (WB), RA (RB), and RSTA (RSTB) denote the write, read, and reset signals for PDHA (PDHB), respectively. In addition, MODEL and SYN serve as the mode-control signals. In the case of MODEL=1, the PDHA and PDHB submodules collaborate, where the amplifier of PDHA serves as the write amplifier, and the amplifier of PDHB functions as a buffer (read amplifier), forming a continuous peak-detection and holding circuit [13]. The reset signal in this mode is supplied externally by the PDHRST, enabling the observation of the entire peak-sampling and holding process. This configuration is instrumental in testing the functionality and precision of the circuits. The experimental results indicate that the proposed PDH operates within an input-signal range of 10 mV to 2 V with a percentage error below 7% and nonlinearity error of less than 1%.



(a)



(b)

Fig. 8 (Color online) (**a**) Block diagram illustrating the peak-detection and holding circuit. (**b**) Simulation results of the peak-detection and holding circuit

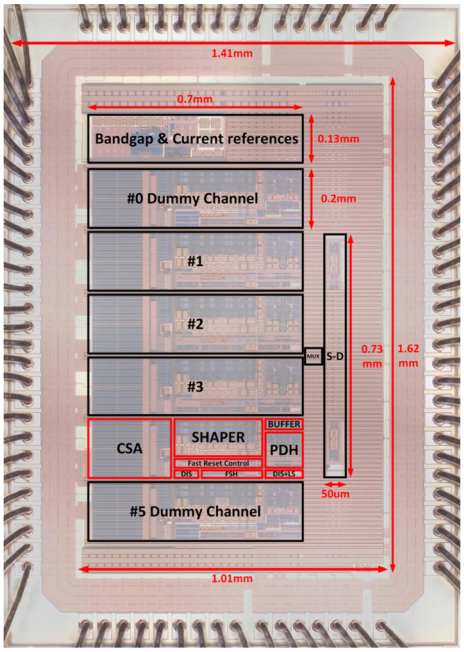
When MODEL=0, the PDHA and PDHB submodules operate alternately and are controlled by a reset signal that transitions between their states. The reset signal is determined by the SYN signal, which provides the flexibility to select either an external input PDHRST (SYN=1) or the trigger signal DIS from the time channel (SYN = 0). The simulation results for the high-speed PDH circuit with SYN=0 are shown in Fig. 8b. Each rising edge of the DIS signal corresponds to the arrival of an event, generating a control signal that triggers one submodule to enter the writing state (whereas the other enters the reading state). The submodule in the writing state has a 45 ns reset process, followed by the completion of peak sampling and the holding of the current event. Simultaneously, the submodule in the reading state reads out the held voltage from the previous event, and the duration of the reading state depends on when the next signal arrives, that is, the time interval between the two signals t_{delay}. The entire PDH circuit functions as an event-driven, first-in-first-out analog memory. If the input signal is detectable by the time channel, the PDH circuit can successfully capture and store the peak values of the shaper-output signals. In this mode, the PDH circuit can detect piled-up signals from the shaper output, reducing the time interval between the input signals from $3.28t_p$ to $1.8t_p$, resulting in an 82% increase in the count rate.

3 Experimental results

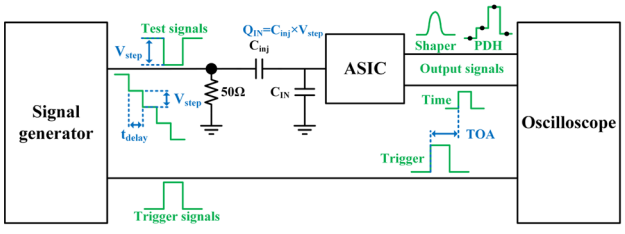
A prototype ASIC chip, SECALROC3, was designed using a standard 0.18 μm CMOS process. Figure 9a presents a microphotograph of the fabricated ASIC. The chip

size is 2.02 mm × 1.41 mm. Each channel has an area of 0.2 mm × 0.7 mm. The power consumption is approximately 35 mW/Ch with a power supply of 3.3 V. The chip-measurement setup is illustrated in Fig. 9b. The ASIC performance is evaluated using electrical tests. The input charges (Q_{IN}) are generated by coupling the step voltages and the capacitance (C_{inj} = 1 pF), and the capacitance value is calibrated using a high-precision LCR meter. An input capacitor (C_{IN}) is placed on the test board to simulate the capacitance of the APD detector. The signal generator generates differential signals; the negative signal is connected to C_{inj}, and the positive signal is inverted by the oscilloscope as the trigger signal.

First, a staircase step voltage with ten steps is generated by the signal generator, adjusting the time intervals (t_{delay}) between steps to simulate input signals of different frequencies and adjusting the step amplitudes (V_{step}) to simulate different input signals. We performed tests on the output waveforms of the shaper and PDH circuits as well as on the piled-up signal to validate the functionality of the proposed



(a)



(b)

Fig. 9 (Color online) (**a**) Microphotograph of the SECALROC3 ASIC. (**b**) Structure of the setup for chip measurement

circuits and verify the ability of the chip to handle event rates. Second, differential square waves with a frequency of 10 kHz are generated to evaluate the dynamic range, linearity, noise, and time performance of the ASIC. Measurements are performed at different step-voltage amplitudes, and the output signals of the shaper and PDH are acquired using an oscilloscope. The data are collected more than 1000 times, and the mean values are recorded and analyzed to indicate the dynamic range and linearity of the circuits. The noise voltage is characterized by measuring the RMS value of the pedestal voltage at the shaper output. The ENC is used to evaluate the noise performance of the ASIC. The rise/fall times (10%–90%) of the step-voltage signals are approximately 1 ns. The time difference between the leading edges of the trigger and time signals from each channel is defined as the TOA. At various voltage amplitudes, over 1000 TOA measurements are recorded and analyzed using an oscilloscope. These measurements are fitted to a Gaussian-distribution curve, and the standard deviation is used to assess the time resolution.

The fast-reset functionality of the CSA is tested, as shown in Fig. 10a. To simulate the pile-up of CSA output signals, the control voltage for the feedback resistor is set to RESCSA = 2.0 V (resulting in a CSA output-signal fall time of approximately 10 µs). The input-signal frequency is set to 1 MHz with a peak time of 240 ns. The test results shown in Fig. 10a reveal that without the fast-reset function, as the CSA signals are piled up for the same input-charge signal, the output signal of the shaper (red color) responds incorrectly and disappears quickly. This occurs until the CSA piles up to its maximum, causing the circuit to enter a pulse dead zone. With the fast-reset function enabled, a reverse signal is observed in the output signal of the shaper (blue), indicating that a fast-reset process occurs at this point. After the fast-reset process, the circuit responds normally to subsequent input signals, and the CSA escapes the pulse dead zone caused by the pile-up. The test results indicate that the proposed CSA enables the controlled accumulation of its output signals, thereby preventing the circuit from piling up to a pulse dead zone and enhancing the circuit event-reception rate. However, compared to a traditional CSA, the feedback resistor R_f of the proposed CSA can be increased to reduce the impact of the ballistic deficit and noise contribution for the same count-rate requirement. Moreover, the output baseline of the shaper is monitored during the test, and no significant change in the baseline occurs, which indicates that the BLH circuit works properly and maintains baseline stability even under high count rates.

Figure 10b illustrates the measurement results for the time parameters of the shaper-output signals. With a peak time (t_p) of 240 ns, the overall width of the signal (t_{width}) is approximately 800 ns. The ratio of t_{width} to t_p is approximately 3.33, which is consistent with the expected

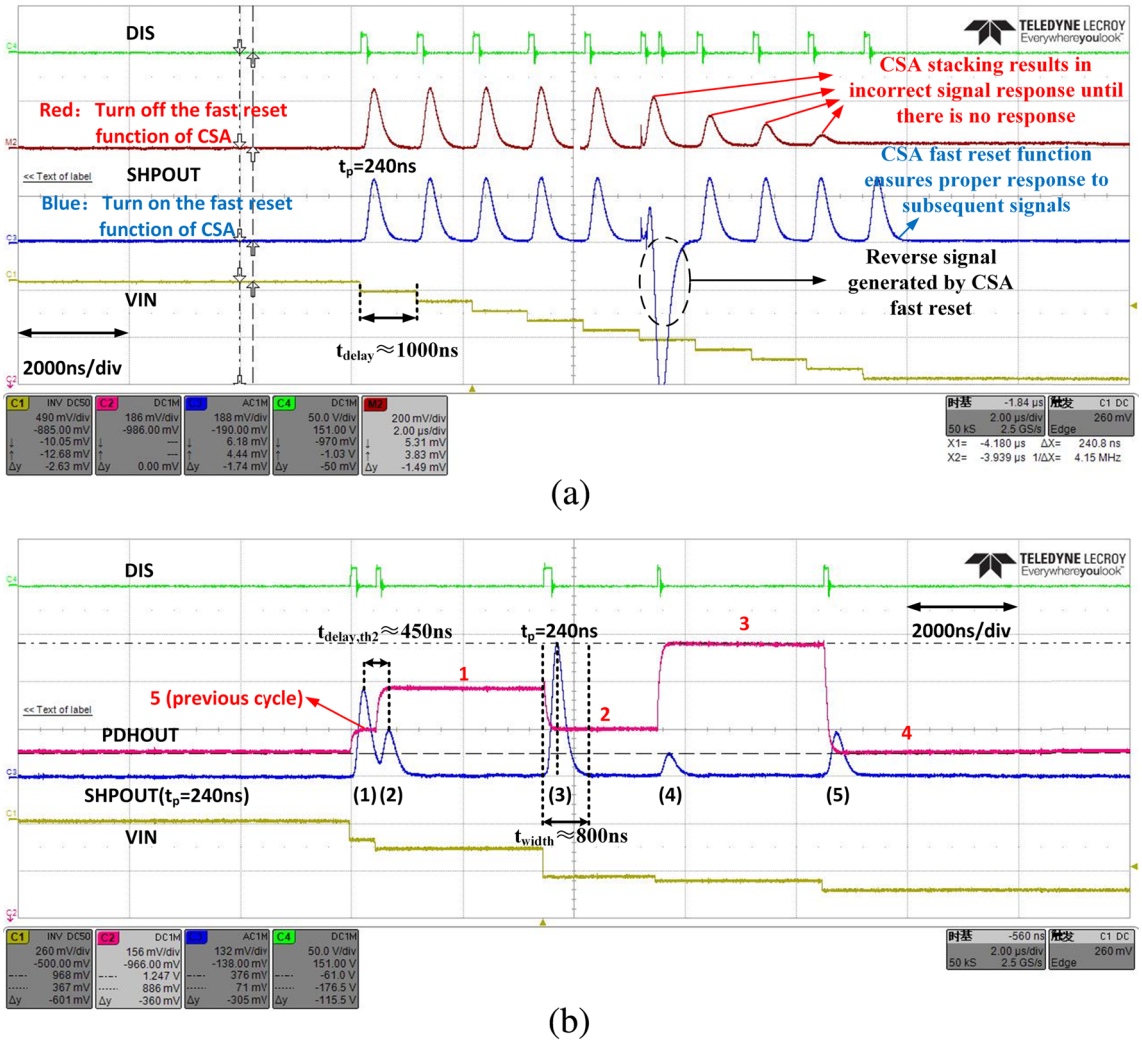


Fig. 10 (Color online) (**a**) CSA fast-reset function test results. (**b**) Shaper and PDH-circuit test results with output piled-up signal

value of 3.28. The measurement results show that piled-up signals with time intervals of no less than 450 ns can be correctly processed by the proposed shaper. The ratio of the time-interval threshold $t_{\mathrm{delay,th2}}$ to the peak time is approximately 1.875, which is in good agreement with the expected value of 1.8. As shown in Fig. 10b, the PDH circuit can effectively capture and hold the peak values of the output signals with varying amplitudes from the shaper, as long as the signals are detectable in the time channel. The proposed PDH circuit can detect piled-up signals from the shaper and hold them until the arrival of the next signal. The overall functionality of the PDH circuit works as an event-driven analog memory that follows the first-in-first-out principle. Consequently, the designed high-speed PDH circuit in conjunction with a high-order shaper reduces the time interval between the input signals from 3.33 t_{p} to 1.875 t_{p}. This enhancement results in a 77.6% increase in the count rate of the front-end readout circuit, allowing the entire circuit to operate at megahertz count rates.

As illustrated in Fig. 11a, the gain of the shaper-output signal is approximately 2.85 mV/fC with a peak time of 600 ns, and the nonlinearity error is less than 1.2%. Concurrently, the PDH output signal demonstrates a gain of approximately 2.72 mV/fC with a nonlinear error below 1.4%. The measured ENC of the ASIC at room temperature under varying input capacitances (0 pF and 270 pF) and different peak times is presented in Fig. 11b, where the test results are generally consistent with the post-simulation results. When $C_{\mathrm{IN}} = 0$ pF, the ENC remains below 1500 e^- across all peak times. In this case, $C_{\mathrm{D}} = 0$ pF in Eq. (3) and Eq. (4), the thermal and flicker noises are small, and increasing the peak time causes the current parallel noise to contribute more significantly to the overall noise. Consequently, an optimal ENC value of 1101 e^- is obtained at a peak time of 480 ns.

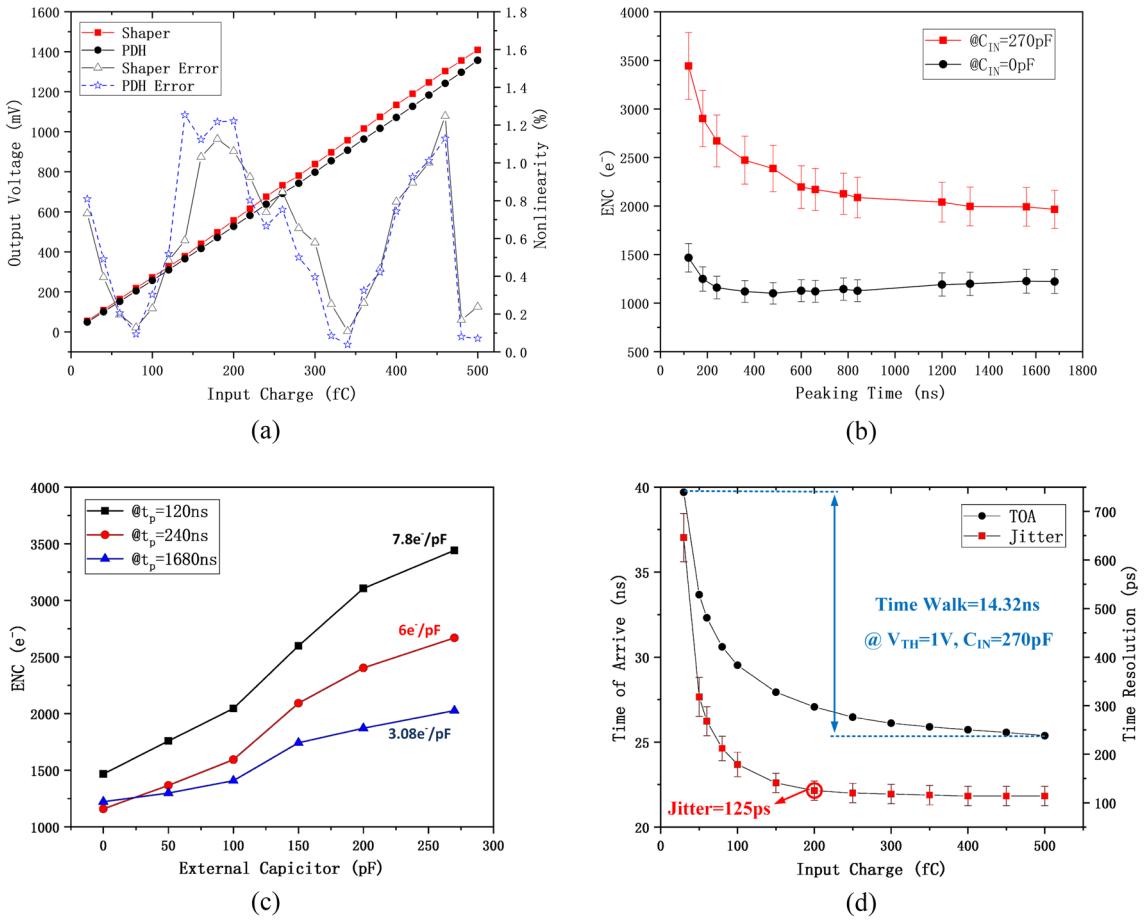


Fig. 11 (Color online) (**a**) Linearity error measured at a 600 ns peak time. (**b**) Measured ENC versus peak time at room temperature. (**c**) Measured ENC versus external capacitance. (**d**) Measured TOA and time resolution versus input charge with a threshold of 20 fC

When the APD detector capacitance is added to the input ($C_{\mathrm{IN}} = 270$ pF), the ENC remains below 3500 e^- for all peak times. The ENC stabilizes at values below 2500 e^- for peak times equal to or greater than 360 ns, reaching a minimum of 1966 e^- at a 1.68 μs peak time. Because the thermal noise of the input MOSFET M_0 is inversely proportional to the peak time of the shaper, ENC decreases with an increase in the peak time. However, the current parallel noise associated with the feedback resistance of the CSA (M_1) and leakage current is proportional to the peak time, and the percentage of flicker noise gradually increases as the peak time increases; thus, the ENC does not decrease significantly with the peak time from 600 ns to 1680 ns. Figure 11c illustrates the test results of the ENC variation with input capacitance under different peak times, demonstrating a linear increase in ENC with augmented input capacitance. The thermal and flicker noises of M_0 are proportional to the input capacitance of the CSA, and the parallel noise is independent of the input capacitance. Thus, the noise slope of ENC versus the external input capacitance is inversely proportional to the peak time. The noise slopes range from 7.8 e^-/pF at 120 ns to 3.08 e^-/pF at 1680 ns. The low-noise-slope performance of this ASIC enables its potential for use in other applications in which detectors have a large output capacitance (several tens to several hundreds of pF) [33, 34].

The TOA and time resolution are measured at thresholds of 20 fC and $C_{\mathrm{IN}} = 270$ pF, as shown in Fig. 11d. The time walk is approximately 14.32 ns for input charges ranging from 30 to 500 fC. Higher input-charge signals exhibit better time resolution than lower input-charge signals. The time resolution is better than 125 ps at an input charge of 200 fC. Table 1 presents a comparison between SECALROC3 and other ASIC chips for ECAL applications. This ASIC provides low-noise and a high count-rate performance with reasonable power consumption. Additionally, subnanosecond time-measurement accuracy is realized for subtrigger systems of ECAL [35], and the precision timestamp measurement allows the ECAL to improve the performance of shower reconstruction, energy correction, and particle identification [36]. Compared with the waveform-recording processing method [5], the peak-detection and holding method can significantly reduce the amount of recorded data, the

Table 1 Comparison of SECALROC3 and other ASIC chips for ECAL applications

Name	Channel	ENC (e^-)	Count rate (kcps)	Time resolution (ps)	DR (fC)	INL	Power consumption (mW/ch)	Process (nm)
SECALROC3 (2023)	4	≤ 3500 @ C_{IN} = 270 pF	4 MHz @ t_p = 120 ns	≤ 125 @ Q_{IN} ≥ 200 fC	500	≤ 1.5%	35	180
SECALROC2 [13] (2022)	1	≤ 4520 @ C_{IN} = 270 pF	400 kHz @ t_p=800 ns	≤ 540 @ Q_{IN} ≥ 160 fC	400	≤ 2.5%	70	180
ANUINDRA [15] (2022)	16	≤ 1812.5 @ C_{IN}=40 pF	200 kHz @ t_p=1180 ns	/	2600	≤ 1%	25	350
HGCROC [5] (2020)	72	≤ 2500 @ C_{IN}=50 pF	/	≤ 25 @ Q_{IN} ≥ 100 fC	320 (TOT: 10000)	≤ 1%	15	65
APFEL [8] (2010)	2	≤ 3906 @ C_{IN}=300 pF	350 kHz @ t_p=250 ns	/	6300	≤ 1%	56.5	350

difficulty of designing the data output interface in the system, and the hardware resource consumption of the data-processing circuitry. One limitation of this method is that it does not record complete signal information, potentially leading to certain events being discarded.

4 Conclusion

This study presents a low-noise, high-rate front-end readout ASIC designed for an STCF ECAL. To address the challenge of high background-event rates in the STCF ECAL, we analyzed the time parameters of the output signals at various nodes in the analog front-end readout circuit. By leveraging the pile-up capability to a certain extent at different nodes, the circuit was optimized and improved to increase the count rate to the MHz/Ch scale. The experimental results indicated that the circuit successfully detected piled-up signals from the shaper output and that the maximum count rate of the proposed ASIC can reach 4 MHz/Ch at a peak time of 120 ns. For a count rate that meets the requirements of 1.5 MHz/Ch (periodically distributed input signals), the maximum peak time of the shaper increased from 203 ns to 360 ns compared with a traditional readout circuit, resulting in an approximately 200 e^- reduction in ENC, which was approximately 2500 e^-. Both energy and time measurements were implemented in this ASIC, which provided the possibility of achieving PUR and calibration in the back-end data-processing program to improve the measurement accuracy of the readout system.

Author's contribution All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by CL, RZ, JW, X-MW, F-FX, R-GZ, and YH. The first draft of the manuscript was written by CL, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data Availability The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.j00186.00315 and https://www.doi.org/10.57760/sciencedb.j00186.00315.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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