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Readout electronics for the gamma detector of the HIRFL-CSR external target facility

Xian-Qin Li[1,2] · Hai-Bo Yang[1,2] · Xiao-Meng Ma[1,2] · Chao-Jie Zou[1,2] · Tao Liu[1,3] · Xian-Cai Zhou[1,4] · Duo Yan[1,2] · Yang-Zhou Su[1,2] · Shu-Wen Tang[1,2] · Shi-Tao Wang[1,2] · Yu-Hong Yu[1,2] · Zhi-Yu Sun[1,2] · Cheng-Xin Zhao[1,2]

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Abstract

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) was constructed to study nuclear physics, atomic physics, interdisciplinary science, and related applications. The External Target Facility (ETF) is located in the main ring of the HIRFL-CSR. The gamma detector of the ETF is built to measure emitted gamma rays with energies below 5 MeV in the center-of-mass frame and is planned to measure light fragments with energies up to 300 MeV. The readout electronics for the gamma detector were designed and commissioned. The readout electronics consist of thirty-two front-end cards, thirty-two readout control units (RCUs), one common readout unit, one synchronization & clock unit, and one sub-trigger unit. By using the real-time peak-detection algorithm implemented in the RCU, the data volume can be significantly reduced. In addition, trigger logic selection algorithms are implemented to improve the selection of useful events and reduce the data size. The test results show that the integral nonlinearity of the readout electronics is less than 1%, and the energy resolution for measuring the ^{60}Co source is better than 5.5%. This study discusses the design and performance of the readout electronics.

Keywords HIRFL-CSR · Gamma detector · External target facility · Readout electronics · Readout control unit · Common readout unit · Peak-detection algorithm

1 Introduction

Technological advancements have made heavy-ion-science experimental facilities important platforms for nuclear physics experiments. The Large Hadron Collider (LHC) [1] at the European Organization for Nuclear Research is mainly used to search for new physics phenomena beyond the Standard Model of particle physics, such as evidence of new particles and dark matter, as well as further studies of particles that have already been discovered, such as the Higgs boson. The Relativistic Heavy-Ion Collider [2] at the Brookhaven National Laboratory in the US has provided physicists with the opportunity to explore multiple aspects of high-energy nuclear physics, including the properties of quark-gluon plasma. GSI [3] Helmholtz Centre for Heavy-Ion Research in Germany is renowned for discovering new elements and studying nuclear structures, reaction processes, and plasma physics. The Institute of Physical and Chemical Research [4] Nishina Center in Japan has made significant achievements in recent years in synthesizing and confirming

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✉ Cheng-Xin Zhao
chengxin.zhao@impcas.ac.cn

[1] Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China

[2] School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing 100049, China

[3] School of Physics and Electronic Engineering, Northwest Normal University, Lanzhou 730070, China

[4] School of Big Data and Information Engineering, Guizhou University, Guiyang 550025, China

new superheavy elements. The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) [5, 6] is constructed to study nuclear physics, atomic physics, interdisciplinary science, and related applications. The HIRFL-CSR has several experimental terminals, one of which is an External Target Facility (ETF) terminal. An ETF [7] is an experiment that studies the equations of the state of nuclear matter, radioactive ion beams, and hypernuclei. The accelerated heavy-ion beam bombards the primary target at the entrance of the Second Radioactive Ion Beam Line in Lanzhou (RIBLL2) [8]. The secondary beam, separated and purified by the RIBLL2, enters the ETF and bombards the secondary target. The detectors at the ETF record the reaction events and obtain information regarding the structure or nuclear reaction of the target nucleus. Figure 1a shows the layout of the ETF, which consists of the scintillator detector (SC2) [9], multiple sampling ionization chambers [10], multi-wire drift chambers [11], gamma detector(γ array) [12], neutron wall detector [13], time-of-flight wall detector [14], and high-acceptance dipole magnet.

A gamma detector was built to measure online gamma rays with energies below 5 MeV in the center-of-mass frame of the fast-moving reaction products [12]. Figure 1b shows a picture of the gamma detector. It comprises 1024 CsI (TI) crystals coupled with an avalanche photodiode (APD; S8664-1010X, Hamamatsu, Japan) [15, 16]. Each detector channel has a length of 110–180 mm, and the total weight of the gamma detector is approximately 1077 kg. An APD with an internal gain of 50 converts the scintillation light of the CsI (TI) crystals into an electrical signal. The outputs of the two pins of the APD are fed into micro-miniature coaxial (MMCX) [17] sockets through an adapter and then enter the electronic system through coaxial cables.

Notably, a readout electronic system must retain the intrinsic accuracy of the detector resolution. The current standard APD [18] readout electronic system methods employ separate signal-processing routes for signal measurements. These systems use application-specific integrated circuits (ASICs) [19] used to obtain an APD readout or charge-sensitive amplifier (CSA) for the readout [20]. The current version of the readout electronics for gamma detectors must be improved owing to the following new requirements. First, the gamma detector is expected to measure gamma rays and is planned to measure light fragments of up to 300 MeV. The current ASICs have a limited dynamic range that needs to be improved. In addition, the detector must participate in the system triggering at the channel level. Waveform digitization technology is expected to provide more information. Thus, the PXI backplane structure cannot satisfy increased data bandwidth requirements. This study presents the upgraded readout electronics for gamma detectors at the HIRFL-CSR ETF.

2 Architecture of readout electronics

Figure 2 shows the architecture of the readout electronics, which consists of thirty-two front-end cards (FECs), thirty-two readout control units (RCUs), one common readout unit (CRU), one synchronization & clock unit (SCU), and one sub-trigger unit (STU). The FEC amplifies and adjusts the electrical signal from the APD and transfers it to the RCU via a flexible PCB cable. In addition, the FEC provides high voltage to the APD. The RCU digitizes the analog signal from the FEC, extracts the energy and timing information from the digitized data using data-processing algorithms in its main field-programmable gate array (FPGA), packages the data, and transfers the data to the CRU via optical fibers. The CRU processes the data and transfers them to the host computer upon local triggers from the RCU or global triggers from the STU. The SCU receives the system clock from the ETF and fans out to the gamma electronics, synchronizing the gamma electronics with the ETF system.

The readout electronic system has two trigger schemes: the global and local trigger modes. In the global trigger mode, the RCU generates and transfers local triggers to the STU once the signal in any channel is higher than a certain threshold. The STU transfers 32 local triggers to the ETF trigger system and receives the global triggers. It sends valid data packets to the host computer only when the CRU

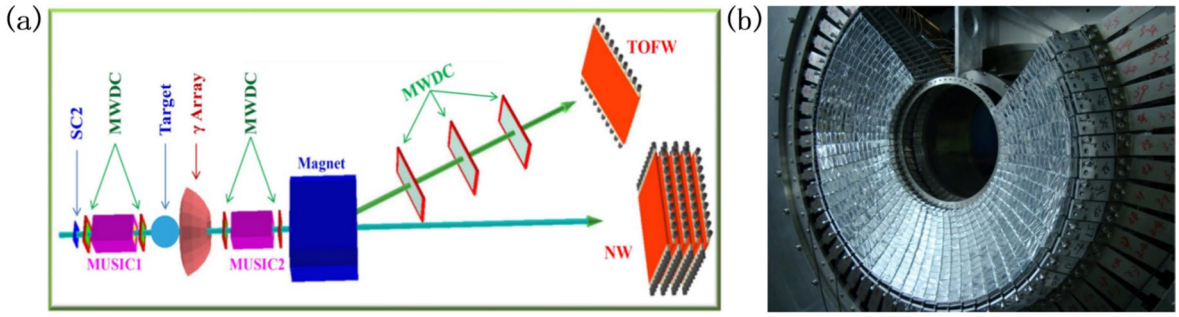

Fig. 1 (Color online) **a** Layout of the ETF experiment at HIRFL-CSR. **b** Picture of the gamma detector

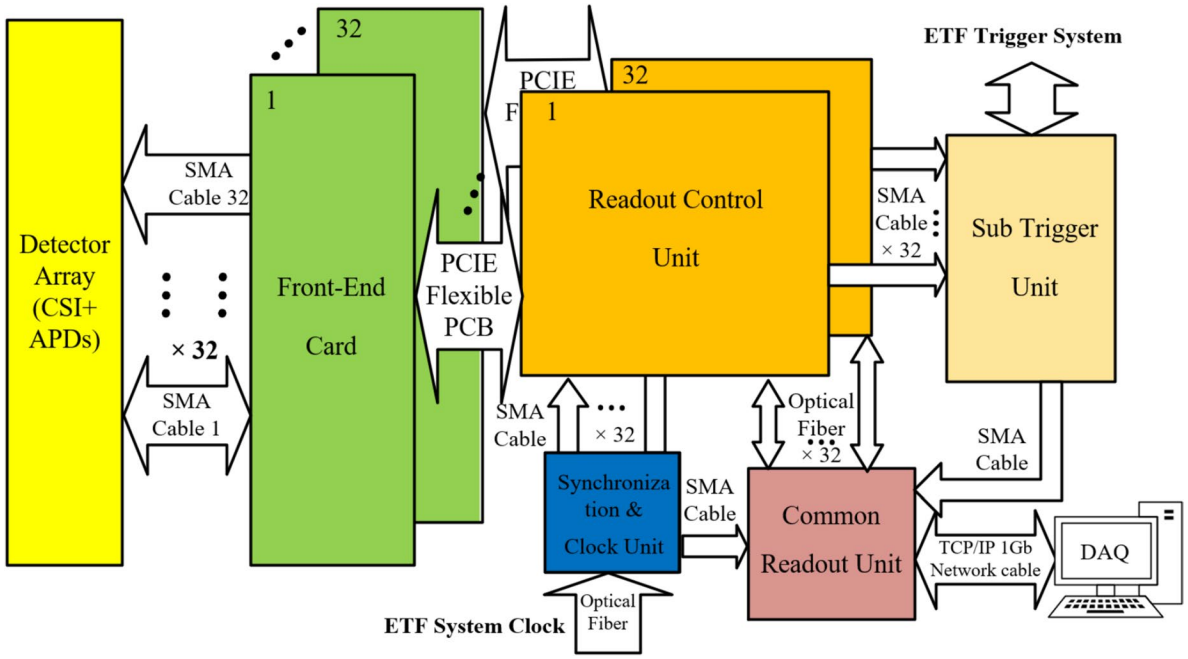

Fig. 2 Block diagram of the readout electronics

receives a valid signal from the STU. In the local trigger mode, the triggering scheme among RCUs is independent. If the RCU generates a local trigger signal, it transmits the collected data to the CRU, which then sends them to the host computer. The local trigger mode was used for debugging.

Figure 3 shows the signal-processing flow of the readout electronic system. First, the CSA amplifies the positive charge pulsed signal output from the detector unit to produce a negative voltage exponential decay signal. Subsequently, through an analog conditioning circuit, the voltage signal is inverted, filtered, fed to the ADC for waveform sampling, and converted into a discrete digital signal. Finally, the FPGA acquires the digital signals for subsequent digital signal processing.

In the electronic system, the only components close to the detector are FECs, which are around it. We added thicker aluminum alloy casings to the front-end cards to enhance protection against the total ionizing dose effects. In addition, current-limiting resistors were integrated into the power supply input of the front-end cards to mitigate the impact of single-event latch-up (SEL). Other system units are not close to the detector and have less impact on the radiation.

2.1 Front-end card

The FEC is a 32-channel CSA that converts a weak charge signal from the gamma detector output into a voltage signal with an acceptable dynamic range for the RCU. Each FEC is connected to 32 detector channels. Figure 4a shows the signal block diagram of the FEC. To reduce the size of the FEC, the FEC adopts a modular design idea, and each FEC consists of a motherboard and 32 daughter boards. The motherboard has connectors, including MMCX connectors for 32 detector signal inputs, one LEMO connector for high-voltage input, one high-density connector for connecting to the RCU, and 32 connectors for connecting to the daughter boards. The motherboard also has some filter capacitors. The daughter boards are single-channel CSAs. They primarily

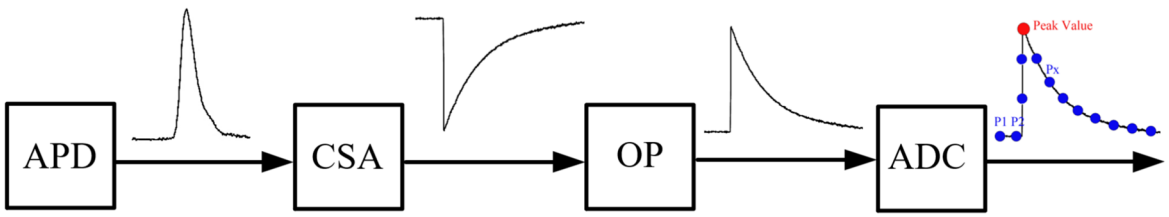

Fig. 3 Signal-processing flow of readout electronics system

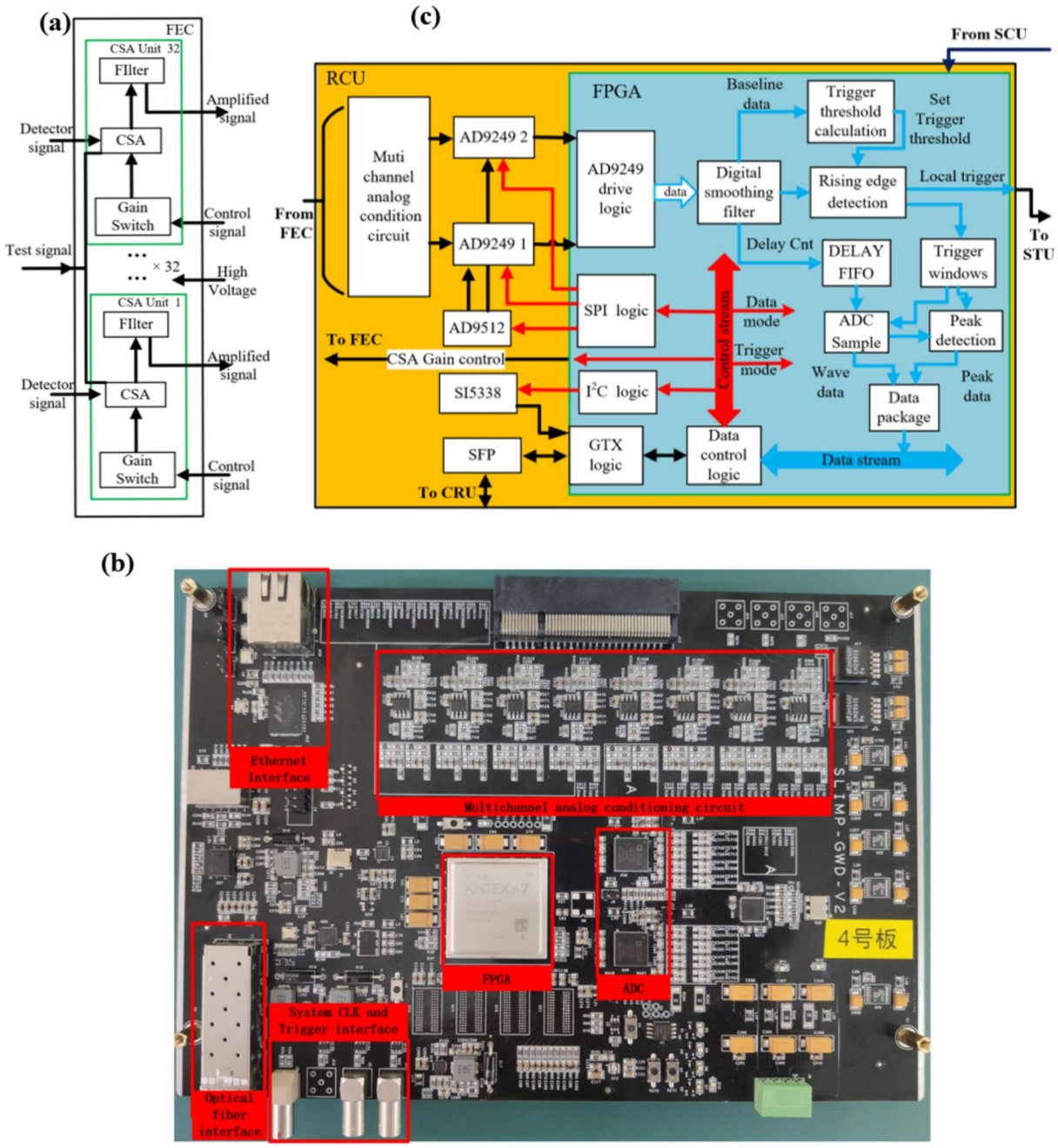

Fig. 4 (Color online) **a** Signal flow diagram of FEC. **b** Hardware design of RCU. **c** Logic design of RCU

consist of a junction field-effect transistor, an operational amplifier, an analog switch, resistors, and capacitors. A low-noise, high-precision, rail-to-rail OPA211 (Texas Instruments, USA) was selected as the operational amplifier. To measure the higher particle energy of the detector system, the daughter boards utilize an analog switch ADG619 to select the value of the feedback capacitor to change the CSA amplification factor. The values of the feedback capacitors are 1 pF and 10 pF. The amplified voltage signal is output to the RCU through an overvoltage protection circuit composed of 1N4148 diodes. The FEC is installed in an aluminum shielded box to prevent external interference, in which the aluminum shell provides a certain degree of radiation resistance. The assembled FEC module is installed on a detector bracket using metal earpieces.

2.2 Readout control unit

Figure 4b shows the RCU design, which mainly includes an analog conditioning circuit, two analog-to-digital converters

(ADCs), the main FPGA (Kintex-7-325T, Xilinx, USA) [21], the optical-fiber interface, and the clock and trigger interface. The analog conditioning circuit linearly transforms the detector signal into a differential input signal for the two ADCs. Each ADC (AD9249 [22]) has 16 channels and provides 14-bit resolution. An AD9512 chip [23] has an input reference clock of 100 MHz divided by two to produce a high-precision 50 MHz clock signal for the AD9249. A programmable signal generator SI5338 [24] chip has an input reference clock of 50 MHz and generates a high-precision 125 MHz clock signal for gigabit transceivers in the Xilinx (GTX) FPGA. The main FPGA configures the onboard chip, performs online data processing, and transmits data to the interfaces. The optic-fiber interface transferred data between the RCU and CRU using a small-form pluggable (SFP) module (FTLF8528P3BCV, Finisar, USA [25]). It can achieve a data-transmission rate of up to 8 Gbps. Through the clock and trigger interfaces, the RCU receives a reference-clock signal from the SCU as the FPGA global clock. This enables all the RCUs to work in the same clock domain. Additionally, the RCU sends local triggers to the STU through the clock and trigger interface. A gigabit ethernet interface is used for the data and control signal transmission during batch-production tests.

Figure 4c shows the FPGA design of the RCU. The logic design of the RCU is divided into control and data-processing parts, with the control part connected to the control stream and the data-processing part connected to the data stream. The control part receives and decodes the control instructions from the CRU through the optical-fiber interface and configures the FEC and RCU. It can switch the gain of the CSA on the FEC, configure the working status of the chip on the board through a specified communication protocol, and configure the working mode of the data-processing logic.

In the data-processing step, the AD9249 driver module converts the 32-channel 14-bit serial data into parallel data, which is output to the data-processing logic. The first data-processing logic is a digital smoothing filter, which eliminates high-frequency noise from the data to reduce its impact on the subsequent peak-detection algorithm. This design uses a moving smoothing method implemented with a minimum mean-square error polynomial function. The equation used is as follows:

$$y(n) = \frac{1}{5}[x(n-1) + 3x(n) + x(n+1)], \quad (1)$$

where $x(n-1)$, $x(n)$, and $x(n+1)$ represent the last, current, and subsequent samples of the ADC data, respectively, and $y(n)$ represents the digital-filter output.

The second data-processing logic is the trigger-threshold calculation logic. The trigger threshold can be configured remotely online or calculated using an FPGA. The trigger threshold logic is calculated by sampling 16 data points for each channel over a specific period and then calculating the average value of the sampled data ($data(i)$) plus the difference between the maximum ($data(max)$) and minimum ($data(min)$) values of the sampled data.

The third data-processing logic is rising-edge detection logic, which is designed to ensure that the signal is in the rising-edge process when it exceeds a threshold. When ADC data exceed the threshold, every two adjacent ADC samples in the following ten ADC samples are compared. If the previous ADC value is smaller than the subsequent ADC value by at least eight times in the 10 comparisons, the rising-edge condition is considered true. If the ADC data of any channel exceed the threshold and correspond to the rising edge of the detector signal, a local trigger is issued. To ensure the integrity of the waveform data after the rising-edge judgment, the ADC data are loaded into the delayed first input-first output (FIFO). The ADC data in the delayed FIFO are read 20 cycles later than the current time, whereas 15 cycles are required to trigger the judgment.

The local trigger starts a trigger window of 3 μs and data window of 60 μs. The channels that fulfill the requirement of issuing a local trigger within this trigger window are determined to be fired in the event, and the ADC data in the data window are processed using ADC sample logic. All ADC data are stored in the waveform mode. In peak mode, the peak value of each waveform is extracted.

Each channel has two data-taking options: the waveform and peak modes, which are implemented in the main FPGA on the RCU. In the waveform mode, all data exceeding the threshold are collected. In the peak mode, the online peak-detection algorithm extracts the peak value of the signal and the time at which it passes over the threshold. Peak-detection logic is achieved by reading the data from the delayed FIFO in the data window. The process of peak detection is as follows: The first ADC data are stored in the register; the second ADC data are read and compared with the first ADC data; the larger one is stored in the register again and compared sequentially until the last ADC data are compared in the data window; and the maximum value is stored in the peak register as the peak value. The ADC data are then packaged with the trigger time, board number, and channel number; transmitted to the data control logic; forwarded to the GTX logic; and sent to the CRU.

Once a trigger is issued, the rising-edge detection logic is suspended until the data processing for the current event is accomplished.

2.3 Common readout unit

Figure 5a shows the CRU design, which mainly includes the fiber-array interface, double data rate 3 (DDR3) interface, main FPGA (Vertex-7-485T, Xilinx, USA) [26],

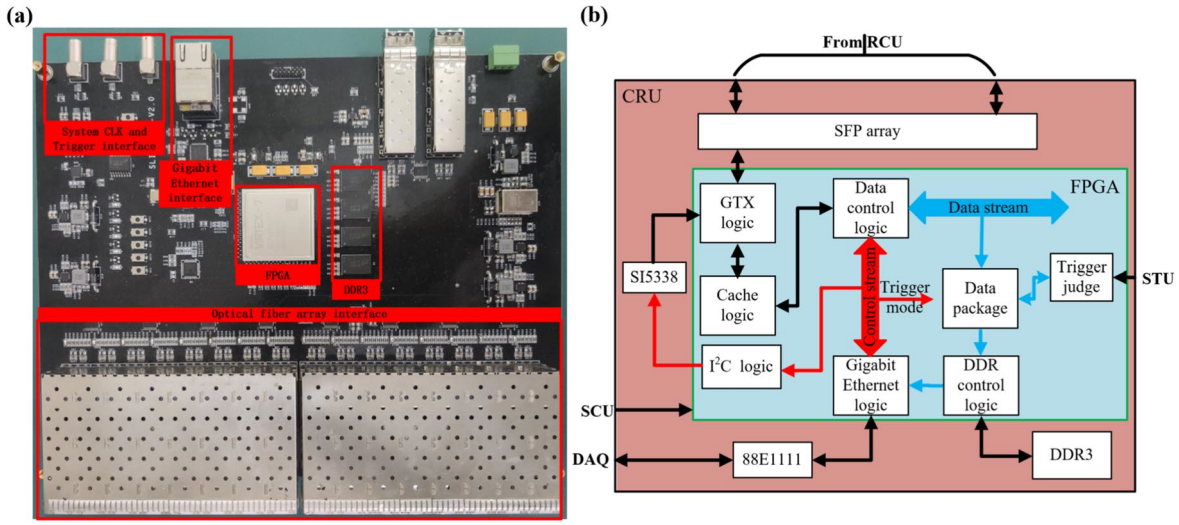

Fig. 5 **a** Hardware design of CRU. **b** Logic design of CRU

gigabit ethernet interface, and clock and trigger interface. The CRU receives data packets from the RCUs and sends control-flow signals to the RCUs through a fiber-array interface. The fiber-communication link uses the Aurora 8B/10B protocol (Aurora 8B/10B is an extensible lightweight link layer protocol provided by Xilinx Launcher for data transmission between point-to-point serial links). The link communication adopts a full-duplex streaming communication mode at a rate of 5 Gbps. To ensure that the multichannel data packets are sent to the ethernet at a stable and reliable transmission rate after being reassembled, a DDR3 interface is used as an intermediate buffer for the data packets. The main FPGA configures the onboard chip, performs online data processing, and transmits data to the interfaces. The gigabit ethernet interface consists of a three-mode ethernet media-access control internet protocol (IP) core in the FPGA and 88E1111 PHY, RJ45 interface on the board. The reconstructed data packets are sent to the host computer through a gigabit ethernet interface based on the transmission control protocol (TCP)/IP. The system-control flow information is received through the gigabit ethernet interface and forwarded to the RCUs. Through the system clock and trigger interface, the FPGA in the CRU operates at the same frequency and phase as the ETF system, and the CRU receives global trigger signals from the ETF trigger system.

The system event rate was < 10 kHz, according to the requirements of the ETF detector system. When the system operates in peak mode, the data for a single channel are 32 bits (including channel number, over-threshold time, and peak data), and the entire event packet header and footer are 128 bits (including data-packet identifier, event number, trigger time, board number, and number of channels). The system has two data modes: the waveform mode, which is only used for debugging, and the peak mode, which is used in actual experiments. We calculated the maximum data-transmission rate requirement by simulating the peak-mode data-transmission rate under the maximum triggering rate. The maximum transmission rate of valid data in the electronic system is 328.96 Mbps in peak mode; therefore, the gigabit ethernet interface can meet these requirements. Considering future compatibility with other detector systems, the interface with the host computer will be upgraded to 10 gigabit ethernet, with two reserved fiber-optic interfaces encapsulated in the SFP modules.

Figure 5b shows the FPGA design of the CRU. The logic design of the CRU is also divided into control and data-processing parts, with the control section connected to the control stream and data-processing section connected to the data stream. The control part receives and decodes control instructions from the host computer through the gigabit ethernet interface and issues instructions to a specific RCU through the board number. It can also batch configure all RCUs through the broadcast mode. In the data-processing part, after receiving the start command from the host computer, the GTX logic parses data packets from the 32 RCUs according to the data window interval set by CRU. The parsed data packets are sequentially packed and stored in the cache logic in chronological order. The data control logic separates the data and control information. The data package logic module is responsible for adding event identification (ID) and timestamps to the data packets read from the cache logic, removing zero-value channels, repackaging the data, and sending them to the host computer. The data-processing logic is divided into two scenarios according to the configured triggering mode of the electronic system. In the local trigger mode, packaged data packets are transmitted

directly. In the global trigger mode, the Trigger Judge logic starts a 60 μs trigger window to determine the validity of the data packet. Within this trigger window, if the CRU receives a global trigger from the STU, and the data package logic receives a valid signal, the packaged data packet is transmitted. If no valid signal is received, the data packet is discarded, and the system continues to wait for the next event. The packaged data are cached in DDR3 through DDR control logic and sent to the host computer after waiting for the gigabit ethernet logic to idle.

3 Performance characterization

Performance characterization was performed on one of the eight sectors of the gamma detector. As shown in Fig. 6a, the test setup consists of four FECs, four RCUs, one CRU, one STU, and one SCU. This setup covers 128 detector channels. First, electrical tests were performed using a signal source to provide an input to the electronic system. Subsequently, a system integration test was conducted on the detector and readout electronics with a ^{60}Co radiation source.

3.1 Electrical performance test

In a laboratory environment, electrical characterization aims to study the stability and functionality of readout electronics. A high-precision arbitrary waveform generator (AFG3252C, Tektronix, USA [27]) is used to inject the signal into the test port on the FEC, which is connected in series with a 10 pF capacitor to the CSA input, and the CSA selects a 10 pF feedback capacitor. The test utilizes exponentially decaying signals of different amplitudes with the frequency set to 1 kHz. The readout electronics operate in the local trigger and waveform modes. The four FECs and RCUs processed the input signal and transmitted the data to the CRU. Subsequently, the CRU packages and transfers the data to the host computer. The data were analyzed offline using Root [28] software to study the performance.

3.1.1 Stability

In the stability test, the electronic system is powered and maintained under working conditions for 720 h. Exponential test signals with slightly different peak voltages are applied to the test ports of the four FECs. The maximum deviation of the recorded peak value from the average value for each channel is extracted to represent stability. During the test period, the data are stored every 72 h. Figure 7a and b shows example results of the peak value and stability for four channels, one on each FEC. In our test, the maximum deviation of all 128 channels is small, at 0.09%.

3.1.2 Baseline and linearity

The baseline noise level of each channel without a signal input reflects the inherent noise of the electronics. The root-mean-square (RMS) [29] value of the baseline is used as an indicator. First, the electronic system is powered and operated for a certain period to maintain the temperature stability of each component. In the test, the equivalent capacitances are considered in actual applications, and the equivalent capacitance of the detector is approximately 280 pF during operation. An adapter board is designed, on which thirty-two 280 pF capacitors are soldered and connected to each input of the FEC via a coaxial cable. Then, 2.5 million ADC samples were continuously collected and analyzed offline for each channel. Figure 8a shows the test results. The RMS of the baseline of all 128 channels on the four FECs was <1.5 mV. This indicates that the electronic channels had relatively low baseline fluctuations.

The linearity of a channel is a critical parameter in electronics. The peak amplitude of the injected signal ranges from 50 mV to 2.4 V in steps of 400 mV. For each

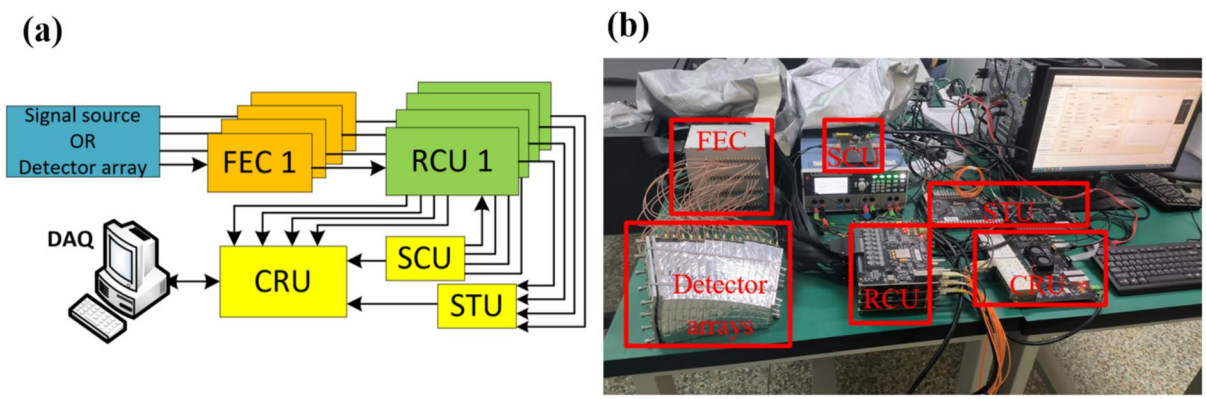

Fig. 6 **a** Architecture of the test setup. **b** Picture of the test setup

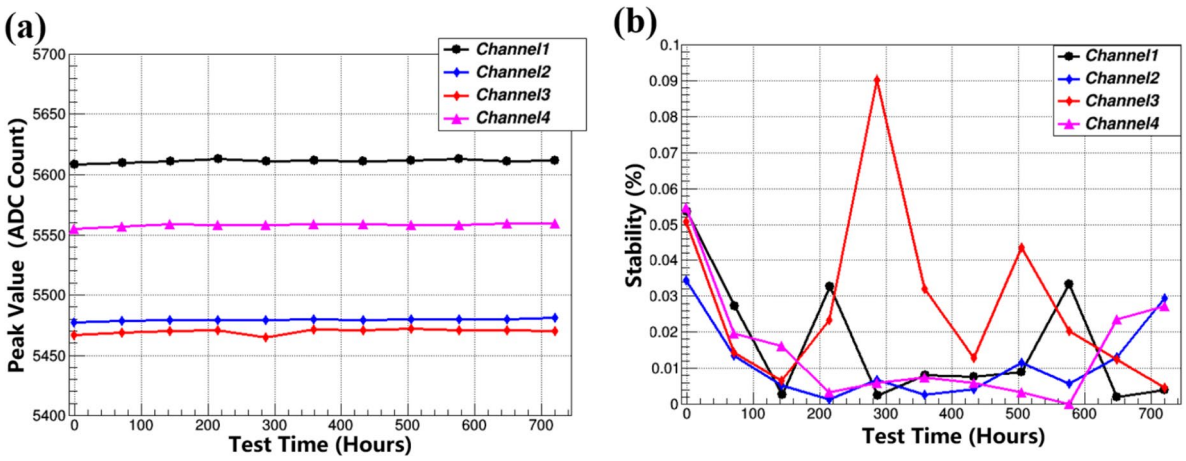

Fig. 7 Stability test of the example channels over long-term operation. **a** Peak value of four example channels versus test time. **b** Stability of four example channels vs. test time

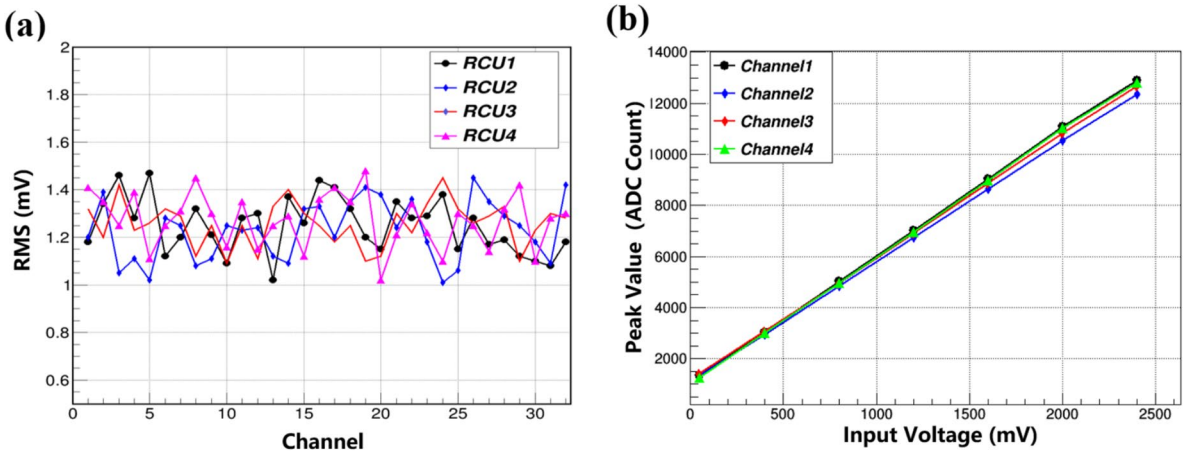

Fig. 8 Test result of baseline and linearity of electronic system. **a** RMS values for each channel. **b** Linear fitting of the example channel

channel, the output corresponding to each peak amplitude was recorded 1024 times, and the average value was calculated. A linear fitting was performed on the average ADC count for each channel. Figure 8b shows the fit of the example channel for each RCU. The horizontal axis represents the peak value of the input voltage, and the vertical axis represents the average output value. The integral nonlinearity (INL)[30] is expressed as a percentage using Eq. 2.

$$INL = \Delta\, V_{\mathrm{omax}}/V_{\mathrm{omax}} \times 100\%, \tag{2}$$

where $\Delta\, V_{\mathrm{omax}}$ represents the maximum error between the actual collection point and fitting point, and V_{omax} represents the maximum output dynamic range. After the calculations, the INL of all 128 channels in the system is better than 0.93%
.

3.1.3 Data-transmission link test

The readout electronics have two major types of data-transmission links: optical-fiber and ethernet links. The former exchanges data between the RCU and CRU. The latter is mainly used for debugging between the CRU and host computer. Bit-error rates are essential for optical-fiber links. In the test setup, four optical links on the CRU were connected to the RCU, and the other 32 optical links were connected to the self-loop. All 36 optical links were operated at 5 Gbps. The bit-error ratio (BER) is the ratio of the number of erroneous bits to the total number of bits transmitted within a certain time. The PRBS-31 pattern was used, and the test lasted for 30 consecutive hours. The Xilinx FPGA offers an integrated bit-error ratio test IP core [31] for directly monitoring the BER, which is recorded every hour. No stops or

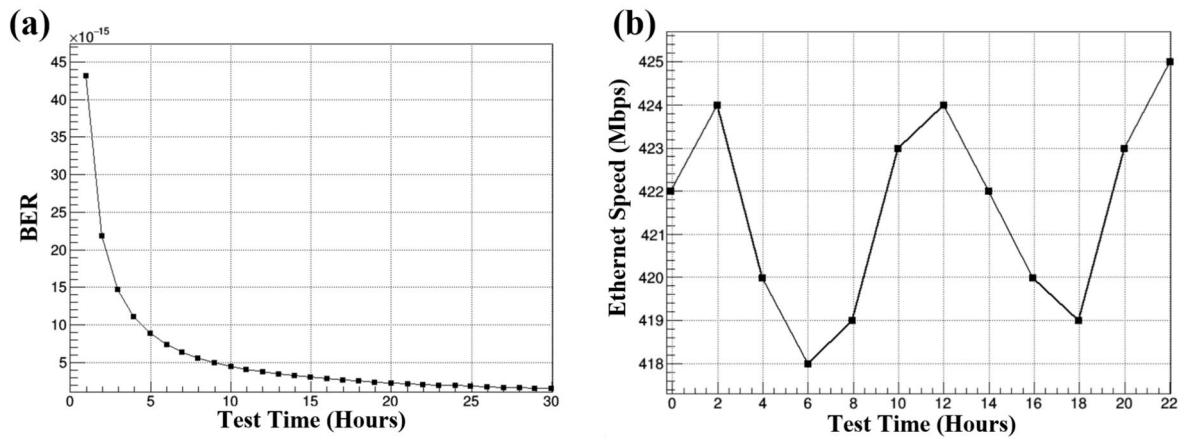

Fig. 9 Test result of data-transmission link. **a** Bit-error rate test results of the optical-fiber link. **b** Ethernet write-rate test results

erroneous bits are observed in any of the 36 optical links. Figure 9a shows the BER for one optical link between the RCU and CRU, where the number approaches 1×10^{-16} at the end of the test.

The bandwidth of the gigabit ethernet link is the key parameter between the CRU and the host computer. In the test, a 10 kHz pulsed signal generated by the signal source emulates the global trigger signal for the CRU, which is similar to the actual experiments. In the data packets of each event, the data are incrementally simulated from all '0' to all 'f,' and is generated on the CRU and transmitted to the host computer. The CRU operates in waveform mode to drive the ethernet link with a high data volume. The packet header consists of a trigger number and timestamp. To facilitate the analysis of the segmented data packets, each test saves data that are continuously transmitted for 2 min into a file. Under the same conditions, data collection is performed every 2 h, and 12 data-packet files are saved. The network-transmission speed is recorded once during each cycle. Figure 9b shows the bandwidth of the ethernet link, which is stable at approximately 420 Mbps, and the peak rate is approximately 425 Mbps. In addition, no bit errors or package losses are observed in the received packages, indicating the stability of the ethernet link.

3.1.4 Online peak-detection algorithm

A test was conducted to validate the accuracy and reliability of the online peak-detection algorithm. The signal source injects a 10 kHz signal into the FEC, and each channel first works in waveform mode and then in peak mode. The data collected in waveform mode are analyzed offline to detect the peak value. The data from the peaks only are the peak values extracted online. Figure 10a and b compares the peak distribution obtained with the two working modes for an example channel. By fitting the distribution to a Gaussian

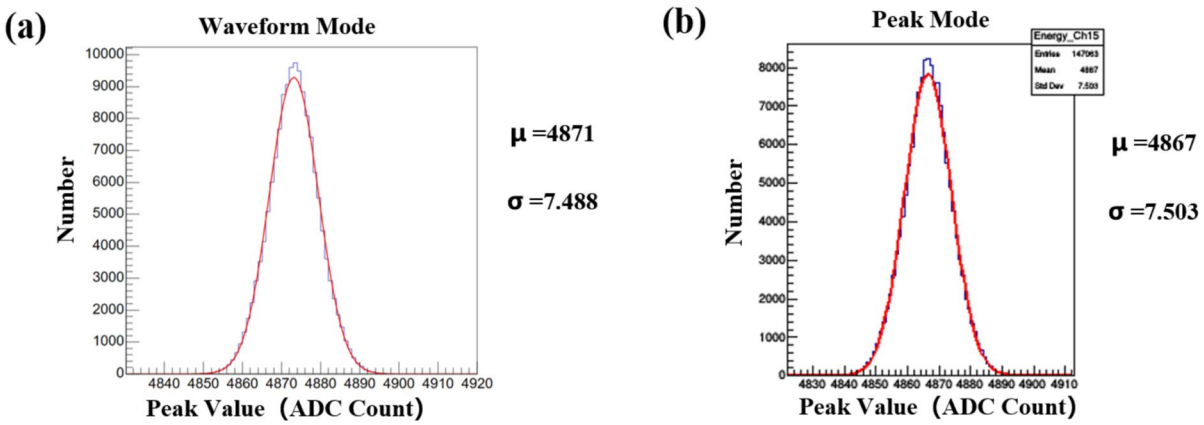

Fig. 10 Test results of peak distribution of an example channel. **a** Offline analysis. **b** Online peak detection

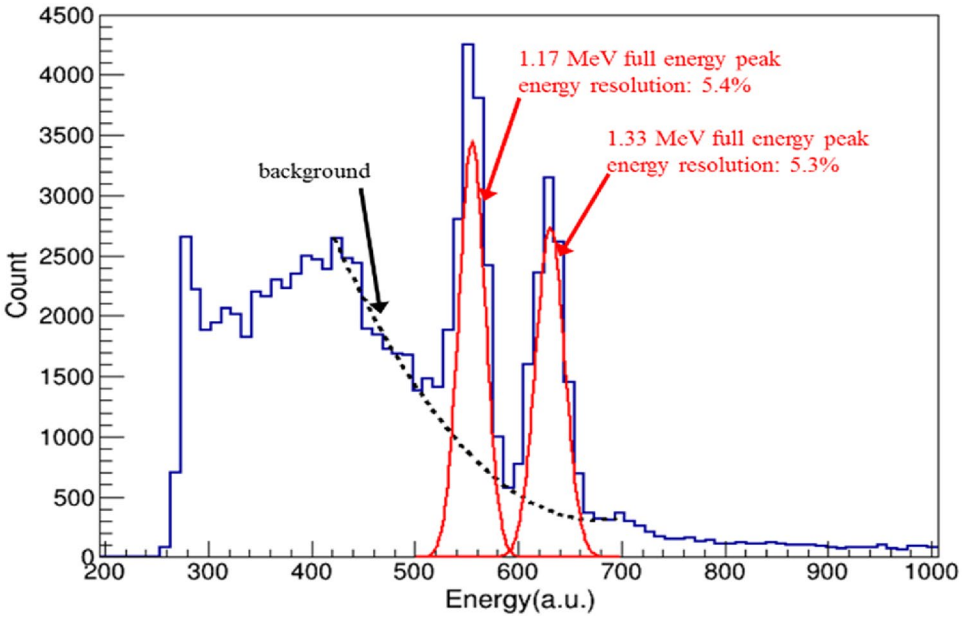

Fig. 11 Measured energy spectrum of the ^{60}Co

distribution, the mean and variation were observed to be rather close. A consistency between offline and online peak-detection algorithms exists in all channels, which proves the accuracy of the peak-detection algorithms.

3.2 Joint test with detector

To verify the performance of the readout electronics system further, a joint test with a detector was performed on one sector of the gamma detector, as shown in Fig. 6b. A ^{60}Co source was used as the radiation source, and the readout electronics operated in the peak-only and local trigger modes. ^{60}Co decays into ^{60}Ni, which is in an excited state, and immediately emits two photons with energies of 1.17 and 1.33 MeV [32, 33]. First, the photons emitted by the radioactive source are converted into light signals via detector crystals. The light signal is then converted into a charge signal by the APDs. Subsequently, the readout electronic system processes the charge signal. Finally, the data are transmitted to the host computer. Figure 11 shows the measured spectrum, where the full energy peaks at 1.17 and 1.33 MeV can be separated clearly with an energy resolution of 5.4%.

4 Conclusion

This study presents the readout electronics for gamma detectors at the ETF of the HIRFL-CSR. The readout electronics process signals from 1024 detector channels. It consists of thirty-two FECs, thirty-two RCUs, one CRU, one synchronization & clock unit, and one sub-trigger unit. The peak value of the detector signal could be accurately extracted online using the peak-detection algorithms implemented in the RCU. This method significantly reduced data volume. A comprehensive characterization was performed for one sector of the readout electronics. The electrical test showed that the INL was less than 1%, and the RMS of the baseline was less than 1.5 mV. A joint test with a detector demonstrated good energy resolution of 5.4%, which was achieved by measuring the photons emitted from a ^{60}Co source. The readout electronics are under installation and commission at HIRFL-CSR.

Author Contributions All authors contributed to the study conception and design. Material preparation, data collection, and analysis were performed by Xian-Qin Li, Hai-Bo Yang, Xiao-Meng Ma, Chao-Jie Zou, Tao Liu, Xian-Cai Zhou, Duo Yan, Yang-Zhou Su, Shu-wen Tang, Shi-tao Wang, Yu-Hong Yu, Zhi-Yu Sun, and Cheng-Xin Zhao. The first draft of the manuscript was written by Xian-Qin Li, and all authors commented on the previous versions of the manuscript. All authors read and approved the final manuscript.

Data Availability The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.j00186.00392 and https://www.doi.org/10.57760/sciencedb.j00186.00392.

Declarations

Conflict of interest Cheng-Xin Zhao is an editorial board member for Nuclear Science and Techniques and was not involved in the editorial review, or the decision to publish this article.

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