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Heavy ion energy influence on multiple-cell upsets in small sensitive volumes: from standard to high energies

Yang Jiao[1,2] · Li-Hua Mo[3] · Jin-Hu Yang[1,2] · Yu-Zhu Liu[1,2] · Ya-Nan Yin[4] · Liang Wang[5] · Qi-Yu Chen[1,2] · Xiao-Yu Yan[1,2] · Shi-Wei Zhao[1,2] · Bo Li[6,7] · You-Mei Sun[1] · Pei-Xiong Zhao[1] · Jie Liu[1]

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Abstract

The 28 nm process has a high cost-performance ratio and has gradually become the standard for the field of radiation-hardened devices. However, owing to the minimum physical gate length of only 35 nm, the physical area of a standard 6T SRAM unit is approximately 0.16 μm^2, resulting in a significant enhancement of multi-cell charge-sharing effects. Multiple-cell upsets (MCUs) have become the primary physical mechanism behind single-event upsets (SEUs) in advanced nanometer node devices. The range of ionization track effects increases with higher ion energies, and spacecraft in orbit primarily experience SEUs caused by high-energy ions. However, ground accelerator experiments have mainly obtained low-energy ion irradiation data. Therefore, the impact of ion energy on the SEU cross section, charge collection mechanisms, and MCU patterns and quantities in advanced nanometer devices remains unclear. In this study, based on the experimental platform of the Heavy Ion Research Facility in Lanzhou, low- and high-energy heavy-ion beams were used to study the SEUs of 28 nm SRAM devices. The influence of ion energy on the charge collection processes of small-sensitive-volume devices, MCU patterns, and upset cross sections was obtained, and the applicable range of the inverse cosine law was clarified. The findings of this study are an important guide for the accurate evaluation of SEUs in advanced nanometer devices and for the development of radiation-hardening techniques.

Keywords 28 nm static random access memory (SRAM) · Energy effects · Heavy ion · Multiple-cell upset (MCU) · Charge collection · Inverse cosine law

1 Introduction

The various energies and types of particles in space environments threaten the reliability of devices in different ways. In previous ground-based single-event effect (SEE) tests, the

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✉ Pei-Xiong Zhao
zhaopeixiong@impcas.ac.cn

✉ Jie Liu
j.liu@impcas.ac.cn

Yang Jiao
jiaoyang@impcas.ac.cn

[1] Institute of Modern Physics, Chinese Academy of Science, Lanzhou 730000, China

[2] University of Chinese Academy of Science, Beijing 100049, China

[3] Spallation Neutron Source Science Center, Dongguan 523803, China

[4] China Electronics Technology Group Corporation No. 58 Research Institute, Wuxi 214000, China

[5] Beijing Microelectronics Technology Institute, Beijing 100084, China

[6] Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

[7] Key Laboratory of Science and Technology on Silicon Devices, Chinese Academy of Sciences, Beijing 100029, China

average energy deposited per unit path along the ionization track of different ions as they traverse a material was defined as the linear energy transfer (LET). The on-orbit error rates can be predicted by obtaining the SEE cross section derived at different LET values. Therefore, the assessment typically focuses on a certain LET, regardless of the ion energy and species. However, as integrated circuit components applied to spacecraft continue to advance, there is growing concern regarding the adequacy of LET as the sole assessment indicator. Based on numerous simulations and tests, the impact of ion energy on the severity of SEE is becoming increasingly apparent.

Initially, researchers used Monte Carlo simulations to identify variations in the charge distribution of ions deposited within silicon at different energies, suggesting that a wider charge track radius of high-energy ions might enhance the charge collection by transistors [1, 2]. However, subsequent experiments found that low-energy ions have a larger SEE cross section near the LET threshold [3]. This demonstrates the correlation between the effects of heavy-ion energy and LET regions. Therefore, after rigorous experimentation using SRAM with transistor gate lengths ranging from 1 μm to 0.14 μm in different LET regions, Dodd et al. found that high-energy ions could cause higher cross sections below the direct ionization threshold because of secondary particles from nuclear reactions. No significant energy effect was found in unhardened devices above the threshold, which was attributed to the low charge density in the peripheral track region of high-energy ions, which had little effect on charge collection [4, 5]. Later, nuclear reactions affecting the SEE near the LET threshold were extensively investigated by experiments and simulations, and the secondary ion distribution from nuclear reactions was strongly influenced by the initial ion energy [6–10].

When transistors reach the nanometer scale, previous work discovered that in the direct ionization region above the LET threshold, charge collection in a small sensitive volume is increasingly influenced by charge track structures, that is, the ion energy. Raine et al. performed device simulations of nano-SOI transistors in conjunction with charge track structures using Geant4 and TCAD and concluded that lower-energy ions have a greater bipolar gain because they deposit more charge in the sensitive region [11]. Subsequently, using the "radial ionization profile" method, which is in better agreement with experimental data, it was demonstrated that the impact of the radial distribution of the charge track increases with technology generation [12–14]. Furthermore, the difference in the SEU cross section of a bulk silicon device with different energies significantly increases as the critical charge gradually decreases [15]. For SOI and bulk devices, a broader radial distribution of the charge track results in higher-order MCUs at high-LET values [13]. However, Geng et al. observed in their simulation results for 90 nm bulk devices that at a high LET, lower-energy ions deposit more charge because of their slower velocity. Consequently, this leads to an increased occurrence of MCU under a tilted incidence [16]. These simulations illustrate that the multinode charge-sharing effects leading to MCU are associated with the charge track radial width and charge density of the charge track structure. Luo et al. experimentally examined the SEU characteristics of 65 nm bulk SRAM across multiple LET regions. Their findings revealed that both the charge track radius and diffusion length influence the MCU pattern and order [17]. In summary, previous research has predominantly focused on the charge collection of individual transistors and has rarely explored the impact of energy on multinode charge collection mechanisms. To date, experimental and simulation studies on the energy effects of 28 nm devices have not been reported.

In this study, ground-based SEE experiments were conducted on a 28 nm SRAM using heavy ions of a similar LET but with different energies and species above the LET threshold. The objective was to compare our findings with those of previous generations of technology nodes and to examine the impact of ion energy on the MCU. By altering the angle of incidence and adjusting the LET region, we obtained insights into the influence of ion energy on different charge collection mechanisms. Finally, the applicability of the effective LET method is discussed.

2 Experimental setup

2.1 Heavy-ion test setup

Irradiation tests were conducted at the Heavy Ion Research Facility in Lanzhou (HIRFL) at the Institute of Modern Physics, Chinese Academy of Sciences, and at the HI-13 Tandem Accelerator at the China Institute of Atomic Energy. Four types of low- and high-energy heavy ions were used to obtain the SEU sensitivity. The details of the heavy ions used in the SEE testing are listed in Table 1. The HI-13 Tandem Accelerator was used to conduct Ge-ion experiments in a vacuum chamber. The ions were accelerated and directed toward the surface of the device. At HIRFL, considering the constant ion energy generated by the accelerator at the terminal, the device surface LET values can be varied using combinations of aluminum foils and air layers of diverse thicknesses to decrease the ion energy. To investigate the influence of ion energy and species on SEU, the combinations of aluminum foils and air layers were adjusted to make the LET of different ions as similar as possible. All the ions had a range of more than 30 μm and could reach the sensitive region of the device. Detailed information on the passivation and metallization layers was reverse-engineered, shown by a scanning

electron microscope (SEM) image in Fig. 1. Furthermore, we calculated the energy and effective LET of heavy ions upon reaching the active region of the device using TRIM-2013 and reported the results in Table 1. These irradiation experiments were performed in an atmosphere with an irradiation flux of approximately 1×10^4 ions/(cm^2 · s). The beam spot size was 2 cm × 2 cm, which completely covered the entire chip.

In the tilted tests, the ion incidence angle was adjusted using a four-dimensional rotating stage. At vertical incidence, the ions were incident in the direction normal to the device surface. SEE tests with tilt angles of 15°, 30°, 45°, and 60° were conducted parallel to the well direction, with the beam unobstructed by the surrounding package material.

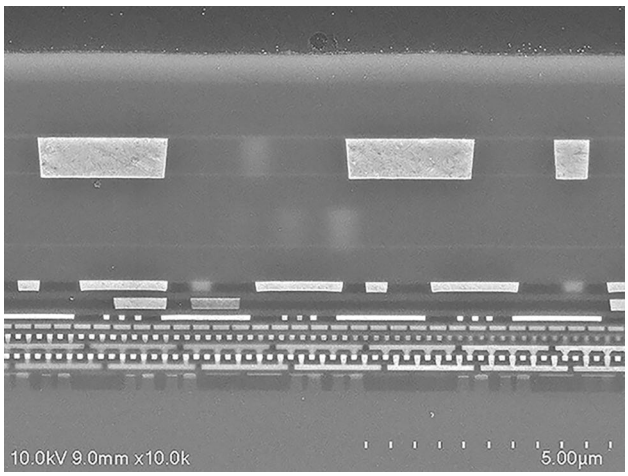

Fig. 1 Cross sectional profile showing the passivation and metallization layers using SEM

2.2 Device and SEU testing method

The chip for the heavy-ion SEE test was a 28 nm 6T SRAM fabricated using bulk CMOS technology with 128 kbits capacity, a standard core voltage of 0.9 V, and an I/O voltage of 1.8 V. The size of the SRAM cell was 0.58 µm × 0.27 µm, the drain area of the NMOS was approximately 1.51×10^{-2}µm^2, and that of the PMOS was approximately 5.66×10^{-3}µm^2. The transistors in the same bitline direction shared the same well, and well contacts were placed at both ends of the well. The chip was de-capped and soldered to a dedicated FPGA test board before the experiment and powered by an off-chip configurable power supply.

Upon irradiation, date pattern 55 h was written into all SRAM arrays, and the resulting data were compared to the preset pattern. During each readback cycle, the test system identified and recorded the details of the single-event upset cells, including logical address and error data. The number of errors was cumulatively recorded in each cycle. The irradiation was stopped when the total number of upset bits increased to at least 400.

The actual positions of the upset bits were obtained according to the mapping relationship between the logical and physical addresses. Physically adjacent or proximate errors that occurred in the same read cycle were classified as MCUs. The number of single-cell upsets (SCUs) and MCUs ($\text{Event}_{\text{i-bit}}$) under each incident condition was counted, and the SEU cross section (σ_{SEU}), event cross section (σ_{Event}), and MCU mean was calculated according to (1)(2)(3), where Φ is the beam fluence with units of ions · cm^{-2}, and N denotes the device capacity. σ_{SEU} was computed from all the upset bits, and represents the probability of a bit flip. In contrast, σ_{Event} was calculated from all SEE events, including SCUs and MCUs, representing the probability of an SEE

Table 1 Heavy ion parameters used in single-event effect testing

Ion species	Energy per nucleon (MeV/u)	Energy on device surface (MeV)	Range in Si (µm)	LET in active regions (MeV · cm^2 · mg^{-1})
^{78}Kr	59.5	4640.0	1176.0	10.7
	35.5	2769.9	522.9	15.2
	21.5	1680.6	252.2	21.1
	16.5	1287.4	176.2	25.1
	10.7	838.3	104.4	31.7
^{74}Ge	2.8	205.0	30.0	36.4
^{209}Bi	96.5	20173.0	1661.5	35.7
	64.0	13369.0	920.6	45.3
	30.4	6362.2	350.2	65.8
	24.8	5187.8	275.5	71.4
	20.8	4348.1	225.6	75.9
^{181}Ta	10.6	1912.1	111.3	78.1

event occurring. The MCU mean serves as an indicator of MCU severity [17, 18].

$$\sigma_{\mathrm{SEU}} = \sum_{i=1}^{\infty} \frac{i \times \mathrm{Event}_{i-\mathrm{bit}}}{\Phi \times N} \tag{1}$$

$$\sigma_{\mathrm{Event}} = \sum_{i=1}^{\infty} \frac{\mathrm{Event}_{i-\mathrm{bit}}}{\Phi \times N} \tag{2}$$

$$\mathrm{MCU\ mean} = \frac{\sigma_{\mathrm{SEU}}}{\sigma_{\mathrm{Event}}} \tag{3}$$

3 Results and discussions

3.1 Irradiation results and analysis

The irradiation results for four types of low- and high-energy heavy ions are presented in Figs. 2 and Fig. 3. The colors represent the various types of ions. The error bars represent one standard deviation from the measured values and are marked as $1/\sqrt{N}$, where N represents the number of upset bits measured during each irradiation test. First, in Fig. 2, as the LET increases, the SEU and event cross sections continue to grow without entering the saturation region. At an LET of 10.6 MeV · cm^2 · mg^{-1}, the SEU cross section is twice as large as the event cross section, indicating a low threshold for the occurrence of MCU. Figure 3 displays the MCU mean with different LETs. With increasing LET,

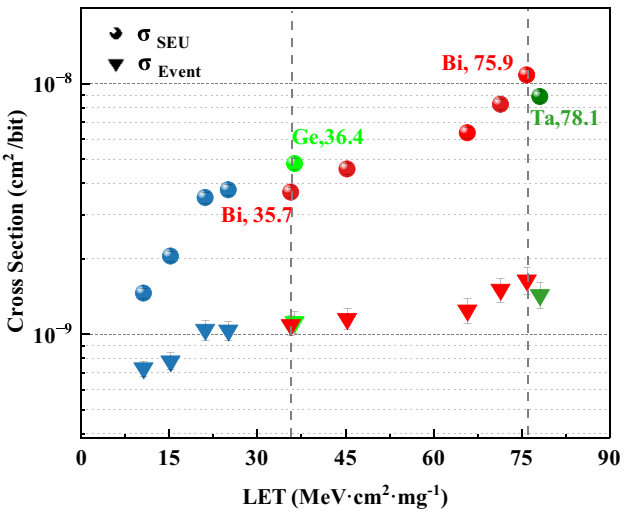

Fig. 2 (Color online) SEU and event cross sections as a function of LET for 28 nm SRAM. Different colors represent different ion species

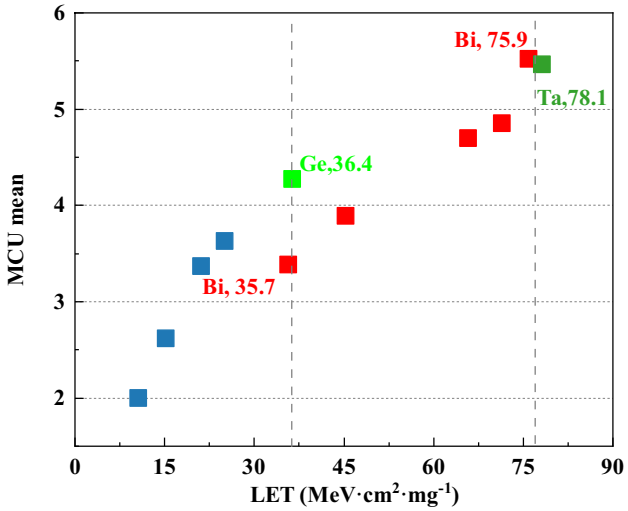

Fig. 3 (Color online) MCU mean as a function of LET for 28 nm SRAM. Different colors represent different ion species

the MCU mean continued to increase, indicating that the impact range of a single heavy ion on multiple sensitive cells gradually expanded. Second, the gradual rise in the event cross section shows that the sensitive area of the cell expands with increasing LET. Between LETs at 35.7 and 78.1 MeV · cm^2 · mg^{-1}, the event cross section occupying the cell area increased from 69.2% to 91.8%. These findings provide evidence supporting the phenomenon of non-saturating behavior.

Interestingly, certain irregularities were observed in regions similar to the LET but at different energies. At approximately 35 MeV · cm^2 · mg^{-1}, the SEU cross section and MCU mean for low-energy ions were greater than those for high-energy ions; whereas, the event cross sections exhibited comparable values. However, at an LET of approximately 75 MeV · cm^2 · mg^{-1}, the SEU and event cross sections of the high-energy ions exceeded those of the low-energy ions, but the MCU means of both were similar. Notably, the influence of ion energy on the SEU varies across different LET ranges.

Subsequently, the heavy ions with similar LETs but different energies (Kr−10.7 MeV/u and Bi−96.5 MeV/u) were incident at a tilted angle along the well direction, as shown in Fig. 4. Changing the incidence angle facilitates multinode charge sharing, providing more favorable conditions to examine the effect of ion energy on MCUs. With increasing incidence angle, the track of charge deposition within the active area was extended, and the diffused charge influenced a broader range of cell arrays. As anticipated, in both LET regions, there was a noticeable difference in the SEU cross section as the tilt angle increased. When the LET was 35 MeV · cm^2 · mg^{-1}, a greater SEU cross section was observed in low-energy ions than in high-energy ions.

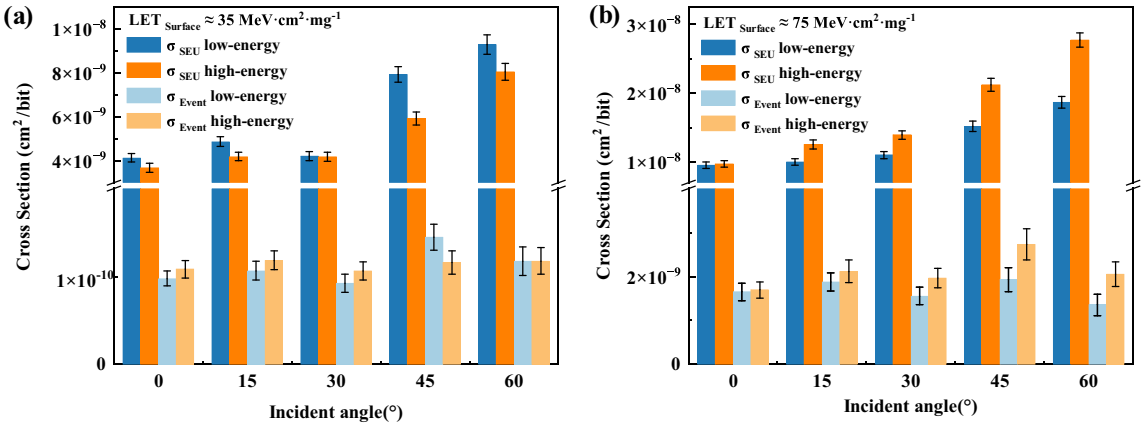

Fig. 4 (Color online) Comparison of SEU and event cross sections at increasing tilt angles for low- and high-energy heavy ions with similar LETs of **a** approximately 35 MeV · cm^2 · mg^{-1} and **b** approximately 75 MeV · cm^2 · mg^{-1}

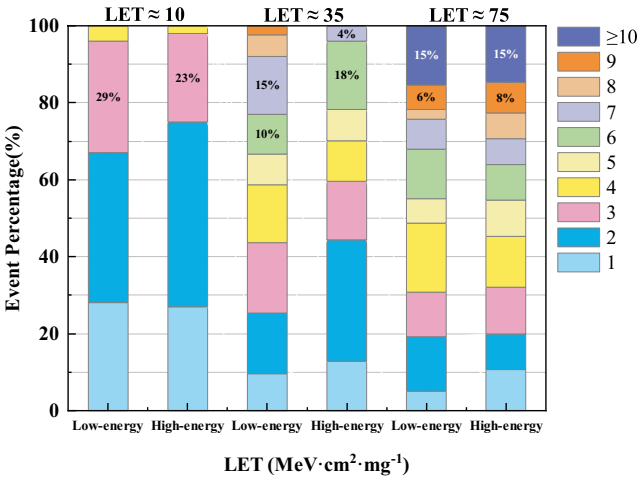

Fig. 5 (Color online) Comparison of MCU ratios of heavy ions at a vertical incidence with different LETs. The MCU ratio of low-energy ions at an LET of 10 MeV · cm^2 · mg^{-1} is referenced from [19]

Additionally, the event cross sections of both ions were similar, with the differences remaining within the error margins. Nevertheless, when the LET reached 75 MeV · cm^2 · mg^{-1}, a contrasting trend emerged. The SEU and event cross sections for high-energy ions exceeded those for low-energy ions, a distinction that became more pronounced with increasing angle.

Figure 5 shows a comparison of the MCU ratios of heavy ions at a vertical incidence with low, medium, and high LETs. The MCU ratio of low-energy ions with an LET of 10 MeV · cm^2 · mg^{-1} is referenced from the MCU ratio of the 28 nm SRAM in [19]. In general, the occurrence of higher-order MCU ratios gradually increased as the LET increased. At an LET of approximately 10 MeV · cm^2 · mg^{-1}, low-energy ions induced a higher proportion of 3-bits and 4-bits MCUs. Moving to an LET of approximately 35 MeV · cm^2 · mg^{-1}, the trend persisted, with low-energy ions still provoking a higher occurrence of >4-bit MCUs compared to their high-energy counterparts, thereby exacerbating the severity of the resulting MCUs. However, as the LET increased to 75 MeV · cm^2 · mg^{-1}, convergence in the proportions of MCUs between low- and high-energy ions became apparent.

Similarly, we investigated MCU ratios at varied angles of incidence, as shown in Fig. 6. Further, Table 2 and Table 3 show the MCU mean and highest-order MCU at different tilt angles with LETs of 35 and 75 MeV · cm^2 · mg^{-1}, respectively. As the incidence angle increased, the proportion of low-order MCUs for both low- and high-energy heavy ions gradually decreased. Conversely, the proportion of higher-order MCUs increased. Consistent with the vertical incidence, when the LET reaches 35 MeV · cm^2 · mg^{-1}, it becomes evident that low-energy ions produce a relatively higher proportion of higher-order MCUs across various incidence angles compared to high-energy ions. The results summarized in Table 2 further reinforce these findings, illustrating that both the MCU mean and the maximum order of MCUs exceed those induced by high-energy ions. In contrast to the characteristics observed in the medium-LET region, in regions with a high LET of approximately 75 MeV · cm^2 · mg^{-1}, there are comparable MCU proportions between the high- and low-energy ions. Additionally, the MCU mean and highest-order MCU for both high- and low-energy ions were similar, as shown in Table.3. Overall, across most LET curves, low-energy ions tended to exhibit a higher proportion of MCUs than their high-energy counterparts. With increasing LET, convergence was observed in the MCUs of both low- and high-energy ions. This convergence indicates a narrowing gap in the susceptibility of electronic systems to disturbances induced by ions with different ion energies.

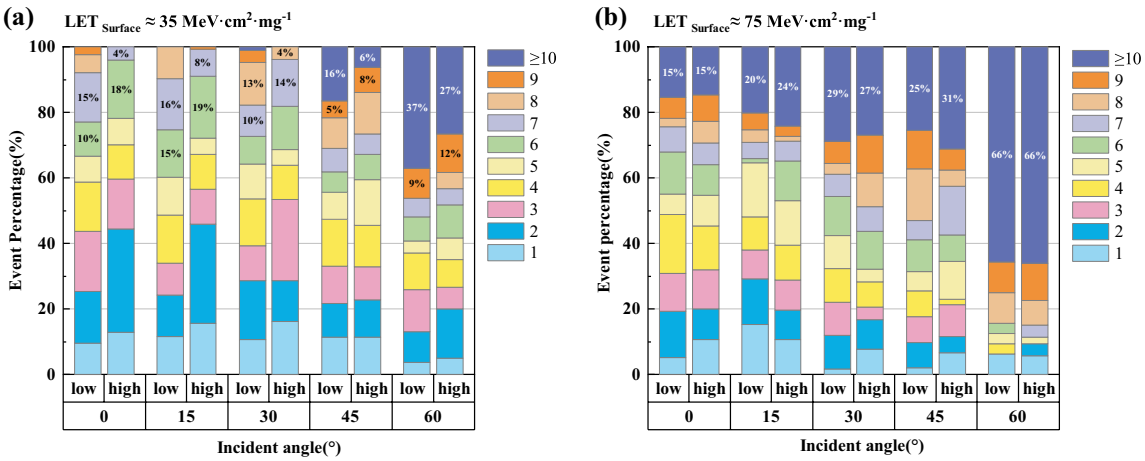

Fig. 6 (Color online) Comparison of MCU ratios at increasing tilt angle with similar LETs of **a** approximately 35 and **b** approximately 75 MeV · cm^2 · mg^{-1}

Table 2 MCU mean and the highest-order MCU at different incidence angles at 35 MeV · cm^2 · mg^{-1}

LET	Angle	MCU mean		Highest order MCU	
		Low energy	High energy	Low energy	High energy
35	0	4.29	3.38	9	7
	15	4.56	3.53	8	9
	30	4.56	3.91	11	8
	45	5.46	5.1	14	11
	60	7.91	6.83	16	15

Table 3 MCU mean and the highest-order MCU at different incidence angles at 75 MeV · cm^2 · mg^{-1}

LET	Angle	MCU mean		Highest order MCU	
		Low energy	High energy	Low energy	High energy
75	0	5.46	5.52	13	13
	15	5.33	5.92	14	13
	30	7.07	7.09	19	18
	45	7.86	7.75	16	17
	60	13.8	13.5	31	35

In summary, at low and medium LETs, low-energy ions tend to generate a higher number of high-order MCUs; whereas, the event cross section remains similar to that of high-energy ions. This results in a higher SEU cross section for low-energy ions. However, with increasing LET, the MCU ratios of the low-energy ions approaches that of the high-energy ions. The event cross section of high-energy ions surpasses that of low-energy ions under both vertical and tilted incidences, leading to a larger SEU cross section for high-energy ions in this scenario. As the LET increases, the disparity in MCU between low- and high-energy ions diminishes; whereas, the event cross section of high-energy ions appears to assume a pivotal role.

3.2 Results discussion

3.2.1 Charge track structures characteristics

Upon the impact of heavy ions on semiconductor materials, energy loss primarily occurs through the generation of high-energy secondary electrons, consequently establishing a nonequilibrium charge distribution region along the ion transit path. Within this charged region, the innermost core is characterized by an exceptionally high density of electron–hole pairs, surpassing 1×10^{22} cm^{-3}. Subsequently, the carrier densities decrease quickly in regions further away from the center [4]. The temporal evolution of the excess carriers in the initial track structure relies on three mechanisms: recombination, diffusion, and drift. Excess carriers in the high-density core experience an exponential decline, primarily driven by Auger recombination, whereas the remaining carriers in the outer regions primarily undergo Shockley–Read–Hall (SRH) recombination [1, 20]. For ions with similar LETs, the total charge in the material remains the same. Nevertheless, the initial radial distribution of the charge density deposited in the material by ions of different energies varies. These disparities have a substantial influence on the subsequent charge collection [2, 21–24].

Figure 7 depicts the charge track structures of heavy ions at different energies with LETs of 35 and 75 MeV · cm^2 · mg^{-1}, simulated by Geant4. In the simulation, we established a lateral size of 10 µm × 10 µm, which was sufficiently large to ensure the deposition of all electron–hole pairs within this area. Furthermore, we set

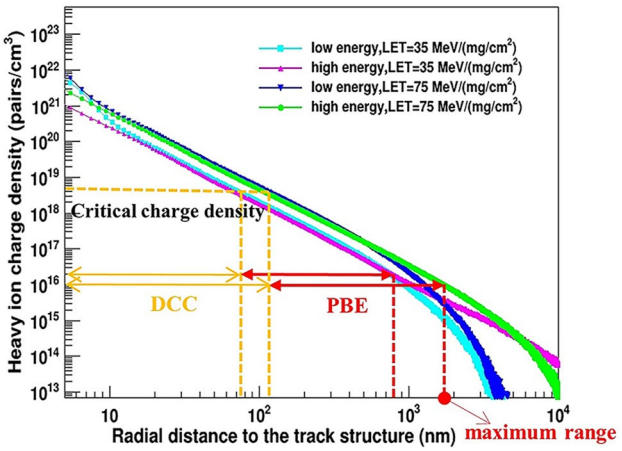

Fig. 7 (Color online) Charge track structures of heavy ions at different energies

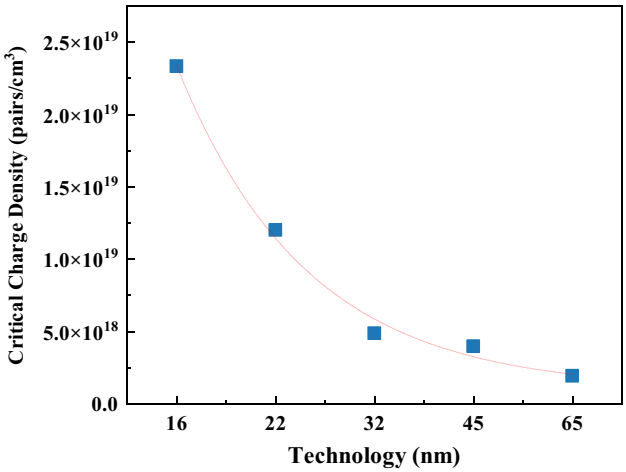

Fig. 8 Critical charge density trend with technology node

the collection depth to 1 µm. The number of incident ions was 10^4 , and the resulting charge track radial distribution was the average distribution of the individual heavy ions. At an LET of 35 MeV · cm^2 · mg^{-1}, low-energy heavy ions produced a significantly higher charge density at the core of the charge track, surpassing that generated by high-energy ions by an order of magnitude over a radial scale of 10 nm. Conversely, high-energy heavy ions generated a more extensive charge distribution that spread across a radius up to 10 µm. With an increase in LET to 75 MeV · cm^2 · mg^{-1}, the charge density within the track for both low- and high-energy ions experienced a noticeable increase, yet the disparity in charge density at the core of the track diminished [25]. Moreover, two heavy ions (low-energy ions at LETs of 35 and 75 MeV · cm^2 · mg^{-1}), possessing comparable amounts of energy per nucleon, exhibited similar charge track radii. With an increase in ion mass, there was a corresponding increase in the charge deposited within an identical track radius.

The response of the deposited charges in the circuits has a complex coupling with the incident particle properties and device structure. Traditionally, the critical charge Q_{crit} is defined as the minimum charge that must be collected for SEU to occur, and the critical charge density N is determined by the critical charge and the sensitive volume:

$$N = \frac{Q_{\mathrm{crit}}}{V} \tag{4}$$

With advancements in technology, both the critical charge and volume have decreased, but the volume has decreased more rapidly [26]. Referring to data from [26], we calculated the trend of the critical charge density with the technology node, as depicted in Fig. 8. The critical charge density exhibits an increasing trend as technology nodes advance. Based on the data presented in the figure, the critical charge density for the 28 nm technology node is approximately 5×10^{18} cm^{-3}.

When the ion deposition charge exceeds the critical charge of the device, the OFF transistor drain collects sufficient charge to flip the cell by drift and diffusion. This process is known as direct charge collection (DCC) [27]. However, for advanced node devices, well potential perturbations can also cause SEUs in regions smaller than the critical charge density. This is because charges that are not directly collected cause a potential gradient from the impact location to the well contact, which can activate the parasitic bipolar effect (PBE) of the MOSFETs, resulting in source-injected charge collection of multiple MOSFETs within the well [28–30]. The range of the well potential perturbation is significantly greater than that of the DCC, which is inversely proportional to the doping concentration of the well [29]. Excess carriers that are not exported by the well contact propagate far from the hit position. As the concentration approaches the well doping concentration, the majority of carriers provided by the impurity atoms in the well dominate the potential. Consequently, at this point, the potential perturbation is not sufficient to breach the intrinsic barrier of the P/N junction. For the 28 nm SRAM tested in this experiment, the cell was not affected by the ionized charge density if it decreased to approximately the substrate doping concentration of 1×10^{16} cm^{-3}.

Therefore, the track structure of the ionization charge distribution can be divided into three distinct sections. The predominant charge collection mechanism varies across different charge track ranges. The first region represents the area where the ionization charge density surpasses the critical charge density. A sensitive OFF transistor drain situated within or in proximity to this region can directly accumulate sufficient charge by drift, diffusion collection, and PBE

collection in the MOSFET itself to trigger a bit flip. This is defined as the DCC-dominated region. In the second region, although the deposited charge is not sufficient for the sensitive node to collect more than the critical charge, the PBE activated by the well potential perturbation contributes a major charge that is sufficient to flip the cell. This area is defined as the PBE-dominated region. The final section comprises the remaining area, wherein the perturbation of the well potential is insufficient to trigger the PBE. Depending on the critical charge density and substrate doping concentration, only approximately 100 nm within the initial charge track is DCC dominated, and the PBE-dominated region reaches the maximum range of 2 µm, as shown in Fig. 7.

3.2.2 MCU pattern and charge collection mechanism

When heavy ions of varying energies impact a 6T SRAM storage array, multinode charge collection generates distinct MCU patterns owing to different charge collection mechanisms and strike locations. Figure 9 and Fig. 10 show the MCU patterns of low- and high-energy ions at a vertical incidence with LETs of 35 and 75 MeV · cm^2 · mg^{-1}, respectively. In the medium-LET region, the MCU patterns are composed of a series of consecutive MCUs with *N* rows × 1 column or *N* rows × 2 columns. Based on the schematics shown in Fig. 11, the layout of the 28 nm SRAM features alternating arrangements of N and P wells. When ions hit the N-well, the charge drift, diffusion, and PBE along the well affect the OFF transistor drain of a column of PMOS in the well, resulting in the formation of MCU patterns with *N* rows × 1 column. Meanwhile, after the ions strike the P well, the deposited charge affects the sensitive drains of the two columns of the NMOS in the well through the charge-sharing effect, resulting in continuous MCU patterns of *N* rows × 2 columns [17, 31].

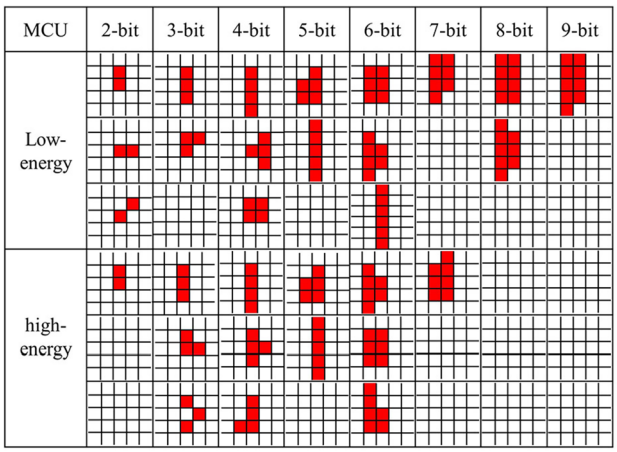

Fig. 9 (Color online) MCU patterns of low- and high-energy ions at vertical incidence with an LET of 35 MeV · cm^2 · mg^{-1}

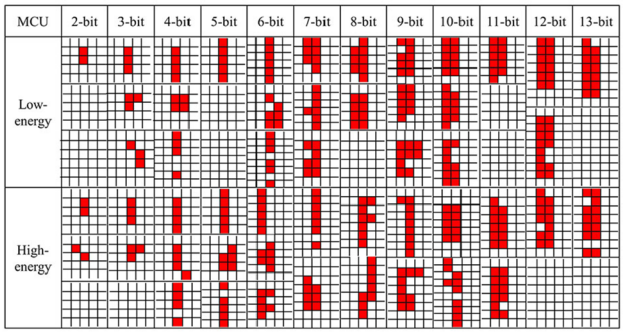

Fig. 10 (Color online) MCU patterns of low- and high- energy ions at vertical incidence with an LET of 75 MeV · cm^2 · mg^{-1}

When the LET is 35 MeV · cm^2 · mg^{-1}, as shown in Fig. 9, low-energy ions are capable of inducing 9-bit MCUs; while, high-energy ions are limited to a maximum of 7-bit MCUs. Additionally, regardless of their impact on the P or N wells, low-energy ions exhibit a broader range of influence than high-energy ions. Based on the analysis of the critical charge density, as shown in Fig. 7, the DCC-dominated region is limited to the sensitive node within a proximity of approximately 100 nm from the impact point. However, the maximum radius along the well for heavy ions extends from 3 × 270 nm, suggesting that PBE is the dominant charge collection mechanism within the range of 100 nm to 810 nm.

With an increase in the LET, the deposited charge increasingly perturbs the well potential, leading to a more complex multinode collection process and diverse MCU patterns. Not only does this lead to the occurrence of interval MCUs situations, but also results in a low probability of MCU patterns in *N* rows × 3 columns, as shown in Fig. 10. This is a notable distinction from the MCU situation observed in 65 nm SRAM [17].

First, upon reaching an LET of 75 MeV · cm^2 · mg^{-1}, the emergence of interval MCU patterns can be observed. This phenomenon was analyzed as a consequence of upset and recovery of cell. This can be attributed to competition of the PBE within an SRAM cell [27, 32]. As illustrated in Cell 1 of Fig. 11, when the N-well potential collapses from electron accumulation, the PBE occurs in the PMOS situated within the N-well. As a consequence of drift, diffusion, and the PBE accumulating sufficient charge, the sensitive drain of P1 undergoes a flip. This event further induces a forward bias in the source of P2. Because of the placement of contact points on both sides of the well in this device, the prompt removal of the deposited charge from the well is impeded, resulting in a sustained disturbance of the well potential. Consequently, P1 and P2 simultaneously accumulate charges, initiating a competitive process

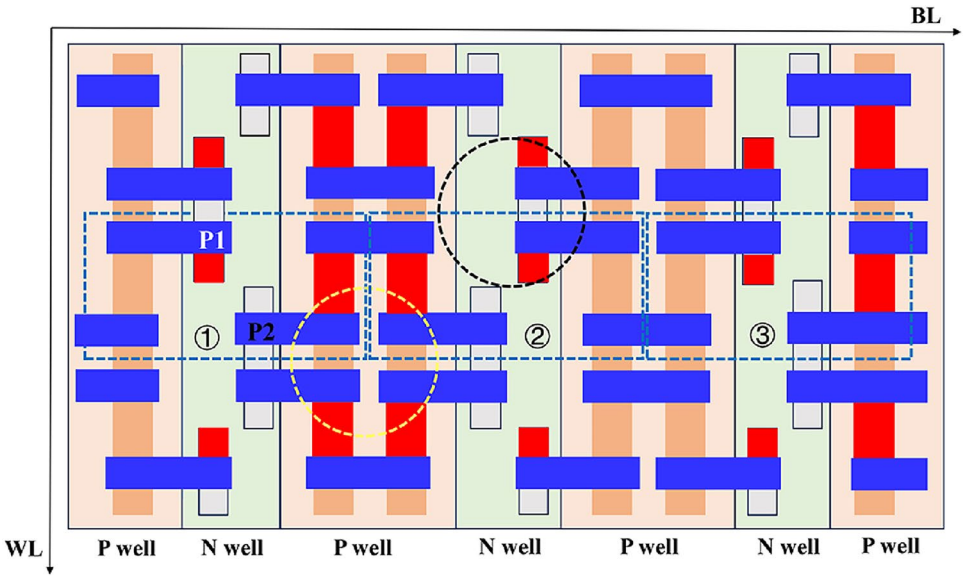

Fig. 11 (Color online) Memory array schematic for 6T SRAM involving nine cells. The red area denotes the OFF transistor drain

between the voltages of the two nodes. Following the persistence of the state of "weak 1" for a period, the final flip state of the SRAM cell is determined by the amount of charge accumulated by the P1 and P2 [27].

Additionally, there is a minor probability of MCU patterns in the form of N rows × 3 columns under a high LET. Along the direction of the bitline, the diffusion of heavy-ion charges is influenced by the potential barrier between the wells. In larger technology nodes, a wider well facilitates a more comprehensive collection of ionized charges within the well. However, at the 28 nm node, the width of the P-well measures 0.37 µm, and the N-well has a width of only 0.21 µm; whereas, the range of influence of heavy ions can reach approximately 1 µm. Consequently, the energy loss of heavy ions can affect the three SRAM cells. As shown in Fig. 11, when high-LET heavy ions strike the N-well as shown in the black circle, the sensitive nodes of SRAM Cell 2 within the N-well can directly accumulate charge and flip. In the P-well, located on the left side of the N-well, the electron–hole pairs generated by the energy loss of high-energy secondary electrons are collected by the sensitive node of SRAM Cell 1 through the diffusion process. Concurrently, on the right side, excess carriers migrate toward the depletion layers of the P and N wells of SRAM Cell 3 and are subsequently collected by the N-well. Owing to the increase in charge collection in this area, the potential of the N-well collapses, resulting in the injection of P-source holes. This injection eventually triggers the PBE, which also flips Cell 3. This outcome stems from indirect charge collection and is thus exclusive to occurrences at high LET levels.

In Fig. 10, at an LET of 75 MeV · cm^2 · mg^{-1}, both low- and high-energy ions can induce the highest-order MCUs of 13 bits, encompassing an impact radius of up to 5 cells, corresponding to an approximate range of 1.35 µm. Corresponding to Fig. 7, this range is near the maximum range of the PBE, suggesting that at an LET of 75 MeV · cm^2 · mg^{-1}, the MCU is approaching saturation.

3.2.3 Dependence of ion energies on charge collection mechanisms

In summary, the distinction between MCUs in various LET regions depends on the charge collection mechanism, which is affected by the energy of the heavy ions. This is discussed in more detail below.

When the LET was 10 MeV · cm^2 · mg^{-1}, the concentration of the charge deposited by the heavy ions remained low. Only the cells positioned close to the core were able to collect adequate charge through drift and diffusion. Owing to the generation of higher ionization charge densities within the DCC-dominated region by low-energy ions, the minority carriers possessed an extended lifespan and greater diffusion distance through SRH recombination, resulting in an increased MCU [17]. Figure 5 illustrates that the MCU predominantly manifests as two and three bits for both low- and high-energy ions. In addition, the proportions of 3- and 4-bit MCUs were higher for low-energy ions than for high-energy ions. The occurrence of 4-bit MCUs may be due to ion incidence at the yellow circle position in Fig. 11, which affects up to four cells by diffusion.

As the LET increased to approximately 35 MeV · cm^2 · mg^{-1}, there was a gradual increase in the PBE-dominated collection in the multinode charge collection. First, the duration of the potential perturbation increased with an increase in the deposition charge. In addition, the parasitic bipolar gain is determined by the total charge deposited in the sensitive region [28]. As evident from the MCU patterns shown in Fig. 9, heavy ions have

a maximum radius of influence of three consecutive cells, which is approximately 0.81 µm. In this region, the wider distribution of high-energy ions has minimal impact on the charge collection process; whereas, the higher charge density resulting from the ionization of low-energy ions has a more significant influence on charge collection. Thus, the higher charge deposition of low-energy ions in the well leads to a longer perturbation time in the well potential and a higher bipolar amplification gain compared with high-energy ions. Consequently, there is an increase in the number of MCUs.

At an LET of 75 MeV · cm^2 · mg^{-1}, low- and high-energy ions can induce an impact radius in the approximate range of 1 µm–2 µm. Within this range, both low- and high-energy ions exhibit a substantial increase in the ionization charge density across the entire charge track under high-LET conditions. Further, the difference in charge density within the central charge track region decreases. It should also be noted that the wider charge track radius of high-energy ions is mostly distributed outside the range of PBE charge collection. Hence, they exhibit similar amounts of deposited charge, leading to comparable perturbations in the well potential and a uniform situation in the MCU.

3.2.4 Inverse cosine law in the effective LET method

In ground-based SEE testing, an effective LET method is frequently employed to simulate ions that are incident vertically at a higher LET by varying the incidence angle. Tilted ions have a greater path length of $1/\cos\theta$ in the sensitive volume than ions incident vertically, and therefore deposit $1/\cos\theta$ times the charge. However, the assumptions inherent in the inverse cosine law are often not applicable to current small-node devices [33–36]. One of the main reasons for this is that angle-invariant funneling and diffusive charge collection lead to discrepancies between the deposited and collected charges. This discrepancy causes an overestimation of charge collection according to the inverse cosine law. Additionally, the dominant charge collection mechanism shifts as the angle increases [33]. By contrast, tilted incidence testing for MCU-sensitive devices triggers higher MCU ratios, resulting in an overestimation of the SEE sensitivity of the device [36–39]. For multiple small sensitive volumes, the charge collection mechanism for the anomalous increase in the MCU ratios owing to an increase in the incidence angle is not clear. Therefore, in this section, we discuss the differences in charge collection mechanisms by the tilted incidence of low- and high-energy ions and clarify the applicable range of the inverse cosine law.

As illustrated in Fig. 12, we compared the SEU cross section at vertical incidence with the cross section obtained for low- and high-energy ions using the effective LET method between LETs of 35 and 75 MeV · cm^2 · mg^{-1}. The results showed a positive correlation between the ion energy and

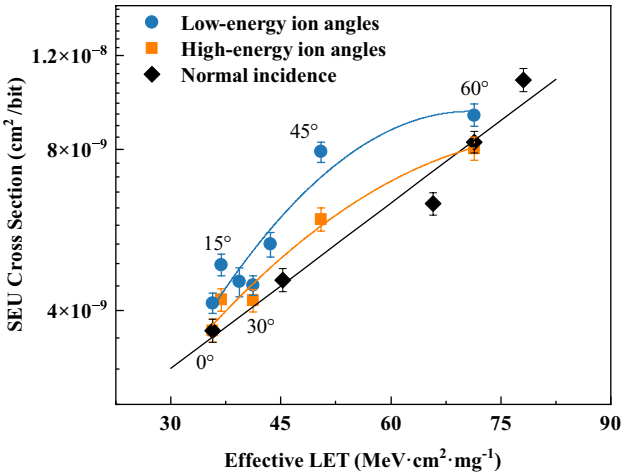

Fig. 12 (Color online) Comparison of SEU cross sections for effective LETs of low- and high-energy ions and vertical incidence

applicability of the effective LET method. Starting with an LET of 35 MeV · cm^2 · mg^{-1}, the trend in SEU cross section resulting from high-energy ions at tilted incidences resembles that of vertical incidence. At a tilt angle of 45°, a slightly larger SEU cross section was observed. However, the distinction between the SEU cross sections of low-energy ions and zero-angle incident ions tends to initially increase and subsequently decrease.

In Sect. 3.2.3, we discussed how the distinctions in SEU cross sections caused by low- and high-energy ions are primarily attributed to variations in the MCU. These distinctions in MCUs are intricately linked to the charge deposition and collection mechanisms. Consequently, variation in the collected charge may emerge as a critical factor affecting the applicability of the inverse cosine law.

In the low-LET region, as the incidence angle increases, the charge collection mechanism changes from drift-dominated to diffusion-dominated. Consequently, the amount of charge collected by the sensitive volume decreases [36]. We also observed changes in the charge collection mechanism as the angle increased in the medium-LET region. First, as shown in Fig. 7, the influence radius for the DCC-dominated region is only approximately 100 nm, resulting in a maximum of 4-bit MCUs. Because of angle-invariant funneling and diffusion collection [40], we assume that the impact of the DCC-dominated region remains, at most, on the 4-bit MCUs. Thus, we calculated the DCC-dominated proportion at various angles, specifically, the proportion of ≤ 4-bit MCUs, as shown in Fig. 13. When the LET of the vertical incidence is 35 MeV · cm^2 · mg^{-1}, the dominant charge collection mechanism is DCC for both low- and high-energy ions, as the DCC-dominated proportion exceeds 60%. As the angle increases, the DCC-dominated proportion decreases to varying degrees for both low- and high-energy heavy

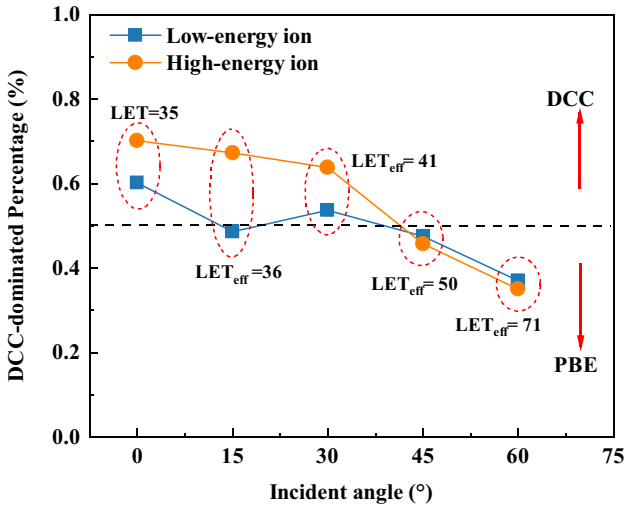

Fig. 13 (Color online) DCC-dominated percentage trends with incidence angle

ions. This suggests that the PBE produces more high-order MCUs.

Notably, at a 15° angle, the DCC-dominated proportion of low-energy ions decreases to approximately 50%. This suggests a transition in the predominant mechanism governing the MCU from DCC to competition between DCC and PBE. Conversely, high-energy ions continued to be dominated by DCC up to an incidence angle of 30°, beyond which there was a shift in the charge collection mechanism. As the incidence angle further increased to 60°, the DCC-dominated proportions were comparable for both low- and high-energy ions; therefore, the distinction in the SEU cross sections is attributed to variations in higher-order flips, as shown in Fig. 6a. This observation implies that at this point, the extent of charge collection is predominantly influenced by the PBE, indicating the dominance of PBE charge collection.

Therefore, we establish two rules: First, increasing the incidence angle does not cause a shift in the primary charge collection mechanism. Second, the incidence angle should not alter the proportion of the sensitive region within the cell, meaning that the event cross section remains unchanged. Conforming to both rules is essential for applying the inverse cosine law when tilting heavy ions toward a small sensitive volume.

Figure 4a illustrates that in the medium-LET region the event cross section remains consistent across all angles, aligning with the second rule. Nevertheless, in Fig. 13 the dominated charge collection mechanism for the low-energy heavy ions undergoes an abrupt shift immediately upon the initiation of the tilt angle. As a result, the SEU cross section of the low-energy ions consistently exceeded the fitted curve for vertical incidence, except at 60°. However, it was only at approximately 45° that the charge collection mechanism of high-energy tilted ion incidence transformed into a competition between DCC and PBE, resulting in a slightly higher cross section than the fitted curve. The distinction between low- and high-energy ions arises from the discrepancy in the ionization charge density within the charge track core, with low-energy ions exhibiting a markedly higher density than their high-energy counterparts. Despite the similarity in LET for both low- and high-energy heavy ions, the total charge deposited by low-energy ions exceeded that of high-energy ions across the entire scope of influence associated with DCC and PBE. Consequently, when low-energy heavy ions are tilted, they deposit a larger amount of charge along the path within the sensitive volume. Furthermore, the increased charge deposition within the well amplifies the well potential perturbation. Therefore, the dominant charge collection mechanism becomes more susceptible to the transition from DCC to PBE. The charge collection mechanism underwent a complete shift from DCC-dominated to PBE-dominated until the tilt angle reached 60°. This resulted in SEU cross sections for both low- and high-energy ions resembling the cross section for vertical incidence. In conclusion, we recommend using high-energy heavy ions to achieve a higher LET through tilted incidence in the medium-LET region.

4 Conclusion

This study investigated the effect of heavy ions with similar LETs but different energies on SEU cross sections and MCUs in 28 nm bulk SRAM. The results revealed that low-energy ions induce higher MCU ratios and SEU cross sections in low- and medium-LET regions, whereas at high-LETs, MCU ratios become similar. The discrepancies in MCUs are attributed to the varied influence of ion energy on the charge collection mechanism. Low-energy ions displayed superior direct charge collection and bipolar amplification gains in the low- and medium-LET regions. At a high LET, the well potential perturbations induced by heavy ions of different energies are similar.

In addition, when the event cross section of low-energy ions reaches saturation, high-energy ions have a larger sensitive region at high LETs, resulting in a higher SEU cross section. Therefore, we recommend using low-energy heavy ions to obtain a worse MCU situation and high-energy heavy ions to obtain a saturated cross section during the single-event sensitivity evaluation and hardened design of the device.

In tilted testing in the medium-LET region, we clarified the applicable range of the inverse cosine law for effective LET methods. This law applies only if both the dominant charge collection mechanism and occupancy of the sensitive region remain constant as the incidence angle changes. Therefore, we advise the employment of high-energy heavy

ions at a tilted incidence to achieve a higher LET. The experimental results presented in this paper improve ground-based test methodologies for investigating single-event effects in devices with a specific focus on ion energies.

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Author's contribution All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by Yang Jiao, Li-Hua Mo, Jin-Hu Yang and Pei-Xiong Zhao. The first draft of the manuscript was written by Yang Jiao and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Data availability statement The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.16436 and https://www.doi.org/10.57760/sciencedb.16436.

Declarations

Conflict of interest The authors declare that they have no Conflict of interest.

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