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Low-power SiPM readout BETA ASIC for space applications

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Abstract
The BETA application-specific integrated circuit (ASIC) is a fully programmable chip designed to amplify, shape and digitize the signal of up to 64 Silicon photomultiplier (SiPM) channels, with a power consumption of approximately ~1 mW/channel. Owing to its dual-path gain, the BETA chip is capable of resolving single photoelectrons (phes) with a signal-to-noise ratio (SNR) >5 while simultaneously achieving a dynamic range of ~4000 phes. Thus, BETA can provide a cost-effective solution for the readout of SiPMs in space missions and other applications with a maximum rate below 10 kHz. In this study, we describe the key characteristics of the BETA ASIC and present an evaluation of the performance of its 16-channel version, which is implemented using 130 nm technology. The ASIC also contains two discriminators that can provide trigger signals with a time jitter down to 400 ps FWHM for 10 phes. The linearity error of the charge gain measurement was less than 2% for a dynamic range as large as 15 bits.

Keywords Radiation detectors · Silicon photomultipliers · Photon sensors · Front-end electronics · Mixed-mode ASICs · Space technology

1 Introduction

This study presents the fi**B**er track**E**r readou**T** **A**SIC (BETA) developed for the readout of SiPM arrays in space applications. BETA has initially been developed to equip different subsystems of the High Energy Cosmic-Radiation Detection (HERD) facility. The HERD has been proposed as one of several particle astrophysics payloads onboard the Future Chinese Space Station (CSS) [1]. The main scientific goals of HERD include searching for dark matter particles, measuring the cosmic-ray spectrum up to PeV energies and monitoring the gamma-ray sky above 10 MeV.

The core of the experiment was a cubic calorimeter composed of more than 7000 crystals. From inside to outside, the HERD detector (Fig. 1) consists of a calorimeter (CALO) for measuring the energy of traversing particles and for electron/proton discrimination, a 5-side particle tracking system (the scintillating fiber tracker, FIT [2]) for reconstructing the particle trajectories and identifying the nuclei charge, a plastic scintillator detector (PSD [3, 4]) for the measurement of low-energy gamma-rays and for a redundant measurement of the nuclei charge, and a transition radiation detector (TRD) for energy calibration. Additionally, a silicon charge detector (SCD) is also used for charge reconstruction. The BETA ASIC is used in the readouts of the FIT and PSD.

The CSS is the ideal platform for providing the required resources for the HERD payload, which has a mass budget of four tons, a maximum power consumption of 1.2 kW, envelope dimensions of 2.3 m × 2.3 m × 2.6 m and an average downlink requirement of 100 Mbps.

Both PSD and FIT are read out with SiPMs and require good resolution and a high dynamic range to track events triggered by minimum ionizing particles (MIPs) and to reconstruct the charge of species up to Fe. The FIT and PSD provide trigger and veto signals for the low-level trigger

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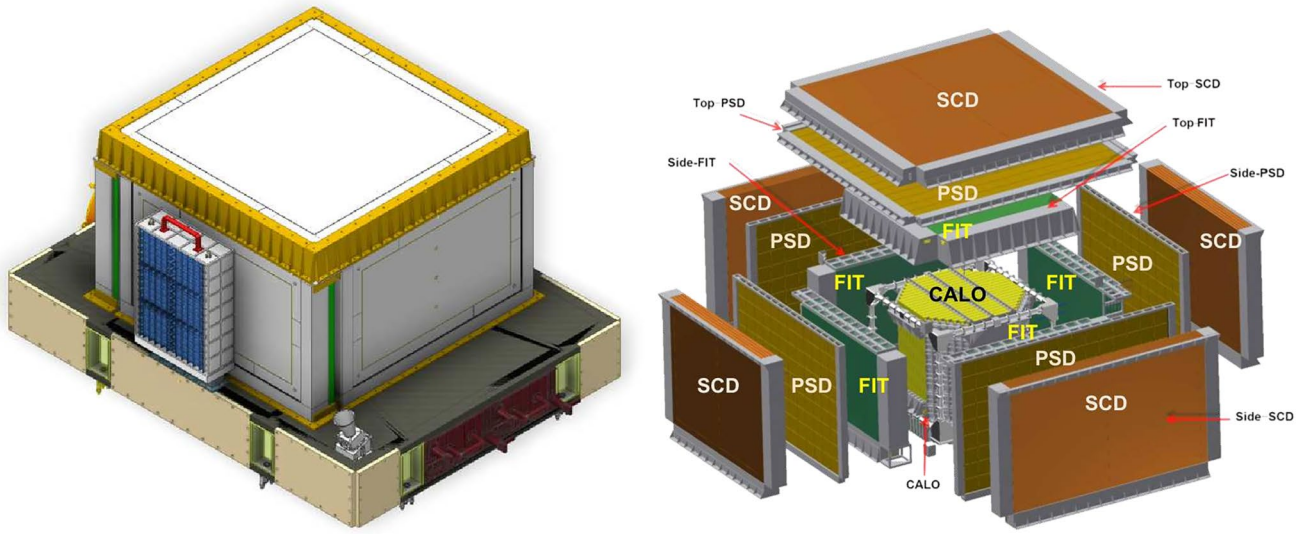

Fig. 1 (Color online) Sketch of the HERD payload. All services and most subsystem electronics are located in the lower plane to maximize the field of view of the instrument. The exploded view (right) of the detector shows the main HERD subsystems [4]

system of the HERD. Therefore, both require excellent signal-to-noise ratio (SNR) to achieve precise MIP detection, perform single-photon calibration and generate precise triggers and veto signals.

The FIT is similar to the scintillator fiber tracker (SciFi) at LHCb (CERN) [5]. To detect the scintillating light of the fibers, a custom-designed SiPM array with a small channel size and a reduced channel pitch (250 µm), which approximately matches the fiber spacing in the fiber mats, was used. This SiPM array is based on the LHCb SciFi sensor (S13552-50 SiPM [6]); however, its dynamic range must be increased to allow the charge measurement of high-Z particles. The FIT is based on a modified sensor array with a reduced microcell size (10 μm $\times$ 10 μm), which increases the number of microcells from 104 to 3749 (S13552-10 SiPM). Therefore, the dynamic range of the readout ASIC should be greater than 14 bits to measure signals of up to 3749 phes with an SNR $>$ 5 for a single-phe signal.

To select the optimal PSD layout, two geometries are currently under investigation: one based on long scintillator bars and the other on square tiles, with both layouts being read out by the SiPMs. The main requirements for the PSD include high detection efficiency, a broad dynamic range and good energy resolution. Different SiPMs are considered and can be combined in a redundant readout (more than one SiPM per tile or bar) to provide optimal performance for the detection efficiency or dynamic range, which is similar to that required by FIT ([3, 4]).

SiPMs are fast photosensors that are sensitive to extremely low photon fluxes and have a relatively high photodetection efficiency. Owing to their robustness, compactness, low-voltage operation and radiation tolerance, SiPMs have become one of the photodetector options for future space missions [7].

In space applications, where volume, cost and power budget are always limited, an ASIC capable of reading multichannel SiPMs and providing digital output while minimizing power consumption is crucial. FIT has hundreds of thousands of channels, and the power consumption requirement per channel is 1 mW/ch in a 64-channel system-on-chip. As for PSD, with a much smaller total number of channels, a 16-channel version is preferred to optimize the SiPM signal routing, allowing a slightly relaxed power consumption requirement. Moreover, PSD requires a trigger signal per channel, whereas FIT does not. A trigger signal per ASIC is sufficient for the FIT.

None of the integrated electronics available in the scientific community for SiPM readouts in space applications satisfies the aforementioned requirements. The PACIFIC 64-channel ASIC [8] was developed to read out the LHCb SciFi; however, its dynamic range is lower than 5 bits (only designed for tracking), and its power consumption is approximately 10 mW/channel. The SPHIRA (IDE3380) 16-channel ASIC [9] was designed for gamma spectroscopy; however, its dynamic range is 12 bits, and its power consumption is close to 2 mW/channel. Furthermore, the analog-to-digital converter (ADC) is not integrated on-chip. The CITIROC 32-channel ASIC [10] has a dynamic range lower than 14 bits and a power consumption of approximately 8 mW/channel. Its ADC is not integrated on-chip, and it was not designed to achieve radiation tolerance. The dynamic range of chips, such as LIROC, RADIOROC and SPACIROC, is

below 8 bits; they do not integrate the ADCs on-chip, and their power consumptions exceed 3 mW/channel [11, 12].

2 Circuit design

2.1 Architecture

A block diagram of the 16-channel version of the BETA ASIC is shown in Fig. 2. The front-end architecture is based on a dual-gain channel system that processes the input current from each SiPM anode node. The current is converted into voltage using a resistor divider. Each channel includes a high-gain (HG) and low-gain (LG) preamplifier.

The output of the HG preamplifier is used to generate the trigger and gain (or path) selection binary signals and for charge measurements. Both binary signals are obtained using a voltage rail-to-rail comparator with hysteresis [13] providing a nonlinear time-over-threshold response. The threshold of a trigger comparator is typically set to a level corresponding to the signal of a few photoelectrons. A global trigger signal is generated as the fast OR of the discriminated trigger output of each channel. In the 16-channel version of the BETA ASIC, the individual trigger signal of each channel is provided as the output signal. The discriminated path selection output is used to internally select the HG or LG signal processing chain depending on the number of detected photons (signal amplitude), thus preventing saturation. The threshold of the path selection comparator (configurable externally) is typically set to a level corresponding to a signal of 50-100 phes. This setting defines the dynamic range of the HG path. Higher signals are processed via the LG path.

The charge measurement chain consists of analog shaping, peak detection and digitization. The shaping stage is divided into an initial first-order low-pass filter (LPF) for each HG and LG preamplifiers. This LPF slows down the signal to allow the digital circuitry to select between the HG and LG signal paths using an analog switch. The selected signal path is followed by a single second-order LPF implemented using a Sallen–Key topology. The peak amplitude of the shaper is captured using a flip-around track-and-hold (T&H) circuit and then digitized. Different parameters (such as gain, shaping time, thresholds and bias currents) of the ASIC can be controlled using an I^2C interface.

The ASIC includes a digital backend to serialize the ADC data in the SEROUT SLVS output and manage different acquisition and trigger modes. Several BETA ASICs can be daisy-chained using SERIN SLVS data input. The TRGOn open-drain trigger output allows the synchronization of the acquisition and serialization of several BETA ASICs.

2.2 Preamplifier

Preamplifiers are based on a closed-loop voltage amplifier with capacitive feedback (Fig. 3) and a tunable gain that can be varied from 4 to 22 for the HG and from 0.3 to 2.4

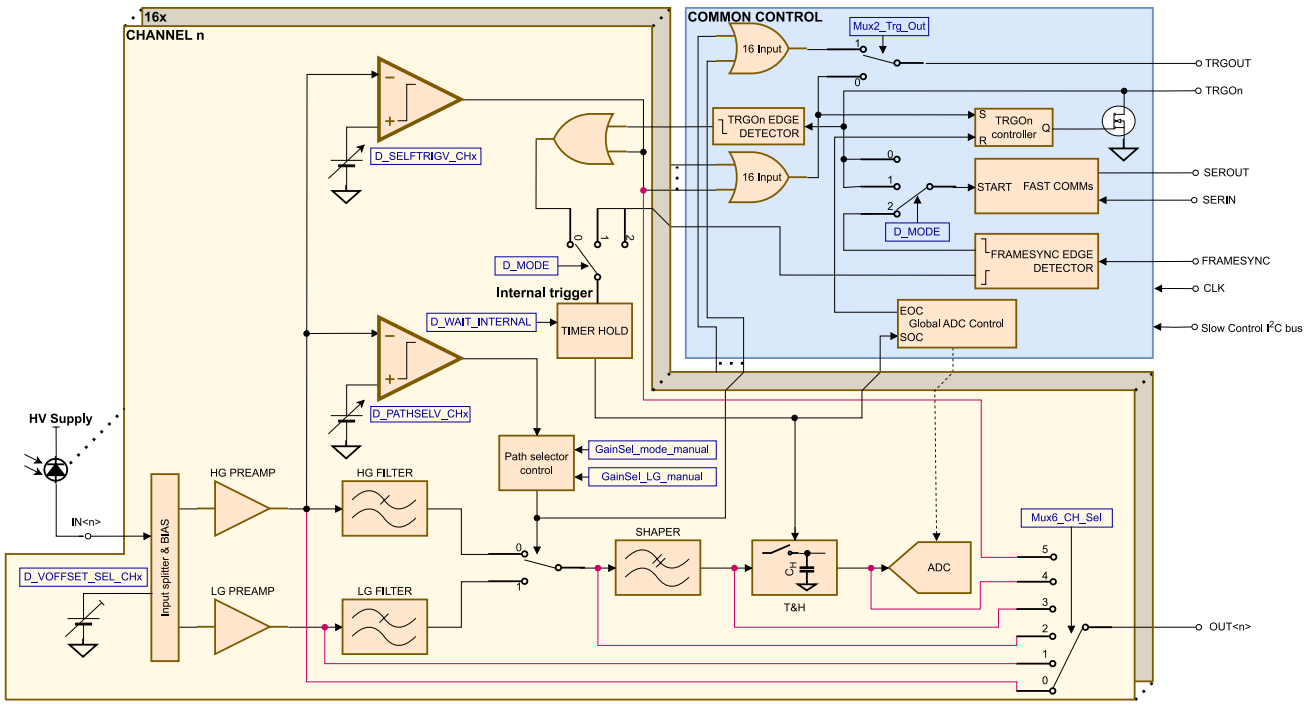

Fig. 2 (Color online) Functional block diagram of the 16-channel version of the BETA ASIC

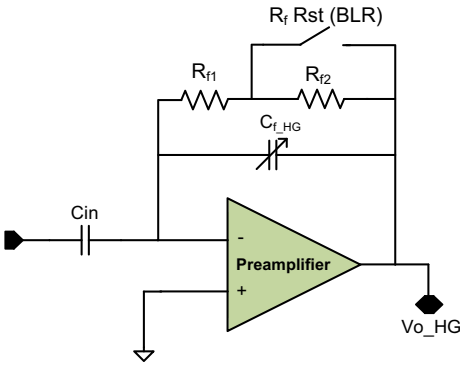

Fig. 3 (Color online) Preamplifier with baseline restoration. Closed-loop configuration based on a custom operational amplifier

for the LG (nominal values). A high-value (approximately 10 MΩ) DC feedback resistor R_f was used in parallel to the feedback capacitor C_f to prevent saturation of each preamplifier. R_f allows the discharge of C_f to its baseline with a time constant defined by $\tau_f = R_f \times C_f$. The feedback resistor R_f is implemented as a series combination of a high-value resistor R_{f1} and a lower-value resistor R_{f2}. The high-value R_{f1} is implemented using a MOSFET in a diode configuration working in weak inversion as a tunable pseudoresistor [14]. The pseudoresistor can be tuned from 1 MΩ to 100 MΩ by varying the bias current. The low-value resistor R_{f2} is approximately 100 kΩ and provides a faster return to the baseline when baseline restoration (BLR) is applied.

The operational amplifier (OpAmp) depicted in Fig. 4 is the basic building block of the different analog processing stages: the HG preamplifier, LG preamplifier, HG filter, LG filter, shaper, T&H and the output analog buffer. Slight variations were applied to optimize the power consumption of each stage. The circuit depicted in Fig. 4 is a two-stage OpAmp amplifier with rail-to-rail input and output ranges based on the design proposed in [15].

OpAmp contains a constant transconductance (g_m) rail-to-rail input stage and a simple class-AB output stage. The class-AB driver circuit was incorporated into the folded–cascode summing circuit of the rail-to-rail input stage. The combined summing circuit and class-AB control are biased by a simple floating current source with the same structure as the class-AB control, resulting in a quiescent current that is independent of the supply voltage. OpAmp was compensated using the well-known Miller-splitting technique. The basic characteristics of the operational amplifier are summarized in Table 1 for different temperatures and process corners.

The basic parameters of the complete preamplifier, including the BLR circuit (Fig. 3), are summarized in Table 2. The transimpedance gain combines the current-to-voltage conversion factor and the voltage gain obtained by transient simulations for a conventional SiPM input signal. Most of the performance parameters are within the specifications for different corners; however, significant variations in power consumption due to process variations can be observed. This is mostly related to variations in the bandgap reference voltage. However, the I^2C interface of the ASIC allows the tuning of the bandgap reference output voltage and controls the bias current of each

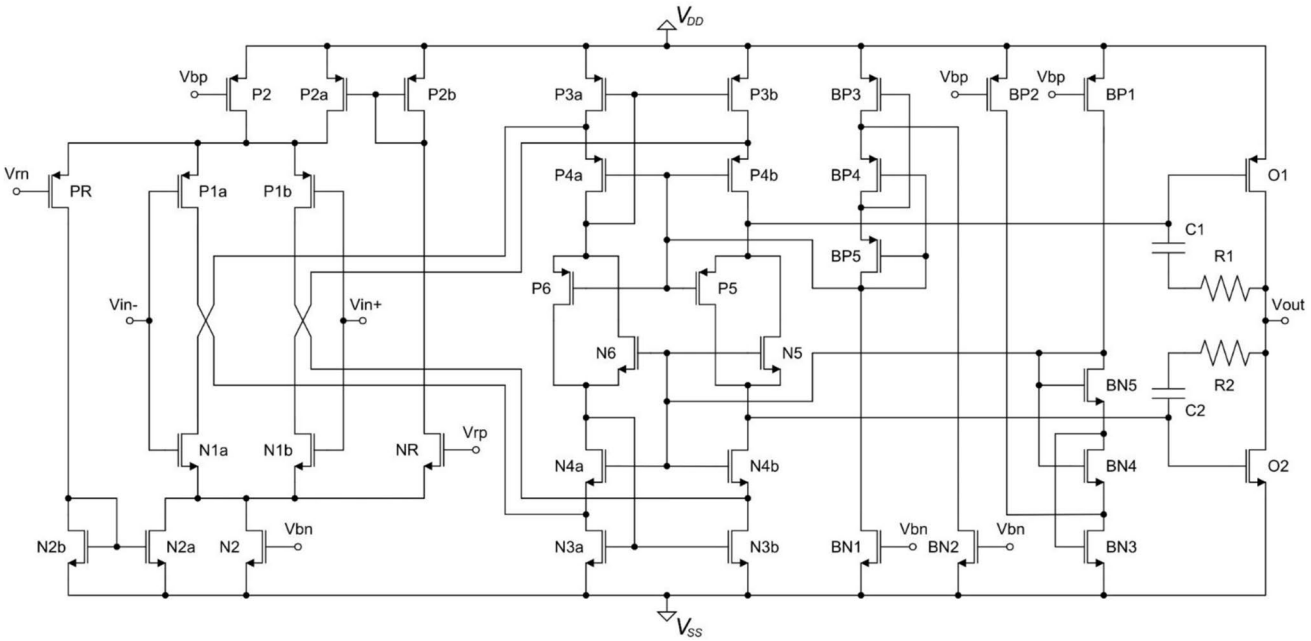

Fig. 4 Two-stage operational amplifier with rail-to-rail input and output range

Table 1 Basic operational amplifier parameters over different process and temperature corners

Parameter	TT[a] 27 °C	SS −20 °C	SS 20 °C	SS 80 °C	FF −20 °C	FF 20 °C	FF 80 °C	FS −20 °C	FS 20 °C	FS 80 °C	SF −20 °C	SF 20 °C	SF 80 °C
Power (μW)	97	83	88	94	100	107	114	90	96	103	92	98	104
GBW[b] (MHz)	74.9	66.4	61.6	52.2	108.4	99.1	73.7	82.0	74.9	56.5	82.8	76.7	64.9
LF open-loop gain (dB)	82.5	86.6	84.7	76.6	85.2	81.1	68.9	86.3	82.3	70.3	85.9	83.9	75.0
Phase margin (deg)	78.7	81.5	83.9	85.7	68.7	69.3	68.5	77.6	78.7	78.5	77.7	78.9	79.4
Gain margin (dB)	13.7	12.9	13.0	14.0	13.6	14.7	21.3	12.8	13.6	18.1	13.0	13.5	15.3

[a] Corners are defined as typical (T), slow (S) and fast (F). The first character corresponds to NMOS and the second one to PMOS transistors

[b] Gain Bandwidth Product (GBW)

Table 2 Simulation results corresponding to the main preamplifier performance parameters for different process and temperature corners

Parameter	TT 27 °C	SS −20 °C	SS 20 °C	SS 80 °C	FF −20 °C	FF 20 °C	FF 80 °C	FS −20 °C	FS 20 °C	FS 80 °C	SF −20 °C	SF 20 °C	SF 80 °C
Power (μW)	115	74	81	95	148	167	195	96	106	122	108	123	146
Bandwidth[a] (MHz)	9.6	7.9	7.2	6.1	15.9	14.6	12.5	10.6	9.7	8.5	10.7	9.6	8.2
Voltage gain[a] (dB)	22.7	22.2	22.1	22.1	23.5	23.4	23.4	22.7	22.6	22.6	22.7	22.7	22.7
Transimpedance gain[b] (kΩ)	2.7	2.7	2.8	3.0	2.4	2.5	2.7	2.5	2.7	2.9	2.5	2.6	2.8
Input impedance[c] [d] (Ω)	270	307	334	375	184	201	228	248	271	304	243	263	299
e_n [d] ($\frac{nV}{\sqrt{Hz}}$)	18.3	18.3	19.8	22.3	15.0	16.3	18.6	17.2	18.6	21.0	15.9	17.3	20.0
i_n [e] ($\frac{pA}{\sqrt{Hz}}$)	7.4	7.2	7.8	8.6	6.4	7.0	7.8	7.0	7.5	8.4	6.5	7.0	8.0

[a] Bandwidth and low-frequency closed-loop voltage gain of the preamplifier from AC simulation

[b] Gain is defined as the ratio of preamplifier peak output voltage to input peak current (transient simulation)

[c] Input impedance is defined as the ratio of preamplifier peak input voltage to input peak current (transient simulation)

[d] Input-referred voltage (series) noise

[e] Input-referred current (parallel) noise

analog processing block to compensate for these variations if needed.

The SiPM signal is AC-coupled to the preamplifier; hence, baseline fluctuations must be considered. Two baseline control methods are used. The first is a BLR circuit: A switch is activated after the conversion, and the feedback capacitor is discharged for a fast return to baseline after the conversion is performed. The second method involves bipolar shaping. The input capacitor of the preamplifier produces an undershoot (zero in the frequency response), whose level could be tuned using the pseudoresistor bias current, as depicted in Fig. 5. The larger the undershoot, the faster the return to baseline.

2.3 Shaping

As already described, the shaper is divided into two blocks: The first block consists of an LPF with an adjustable time

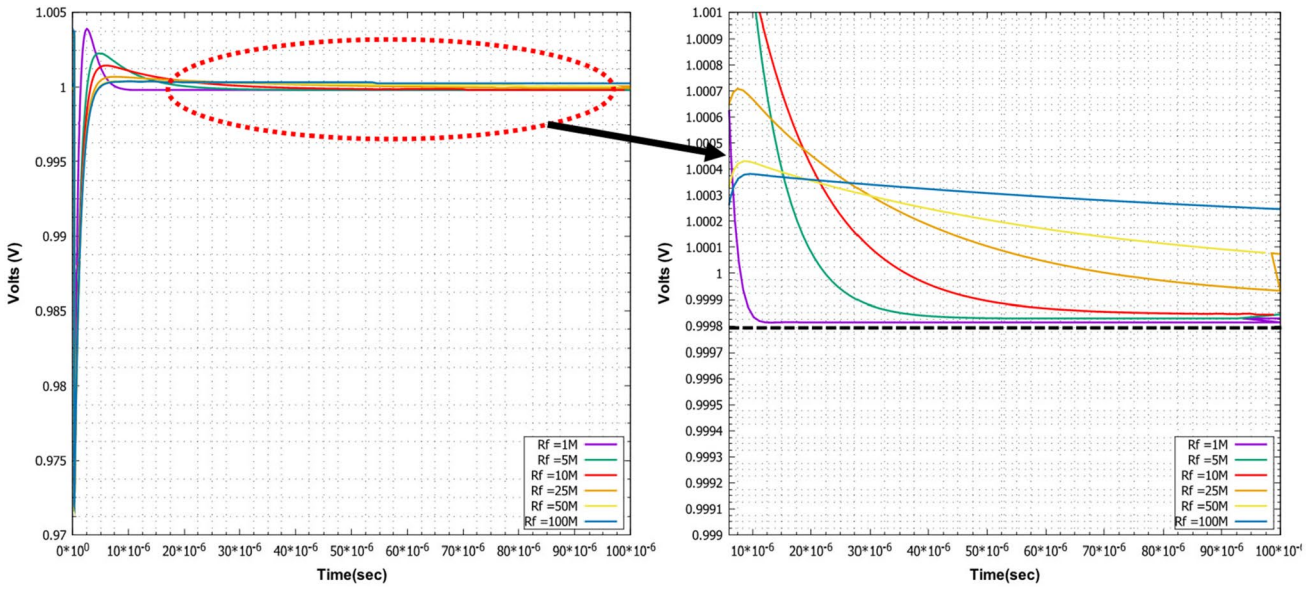

Fig. 5 (Color online) Normalized preamplifier response as a function of R_f value (left) and zoomed in mage of the baseline return (right). Note that the signal polarity is negative and the undershoot polarity is positive. Simulation results for a conventional corner at 27 °C

constant for each of the HG and LG preamplifiers. The LPF slows down the signal to allow the digital circuitry to select between the HG and LG signal paths using an analog switch. The selected signal path is followed by a second shaping block consisting of a second-order LPF implemented using a Sallen–Key topology (Fig. 6).

Thus, the block filter and signal bandwidth both contribute to optimizing the signal-to-noise ratio. The peak time of each shaper can be tuned from ≈150 ns to ≈1.5 us in steps of ≈70 ns, as shown in Fig. 6. The nominal peak time was approximately 1 μs.

The basic parameters of the shaper are summarized in Table 3. The process variations mostly affect the shaper time constant (related to the bandwidth and peaking time); however, the shaper capacitors (C1 and C2 in Fig. 6) can be tuned to compensate for these variations. The transimpedance gain is defined as the ratio of the peak output voltage of the shaper to the preamplifier input peak current; hence, it defines the gain of the complete analog signal processing chain. This was obtained through a transient simulation using a conventional SiPM input signal. The equivalent noise input current (ENI) is computed as the ratio of the integrated noise at the output of the shaper to the transimpedance gain. With current-sensitive preamplifiers, electronic noise is referred to as the input current, similar to the equivalent noise charge (ENC) for charge preamplifiers, and is usually expressed in nA rms.

2.4 Dynamic range

The shaper peak output voltage and corresponding linearity error from a transient simulation as a function of the input peak current are depicted in Fig. 7. For signals below 200 μA, the HG is selected using an automatic path selection system. When the peak amplitude at the output of HG is higher than the threshold set in the path selection comparator, the system switches to LG. The response is linear for input peak currents up to 10 mA. The gain, which corresponds to the slope of the linear sections of the HG and LG, is depicted in Fig. 7, and the switching point between HG and LG can be programmed.

The dynamic range is defined as the ratio of the largest and smallest values that a certain quantity can assume. As discussed previously, the largest signal that can be processed is at least 10 mA (the input peak current). The smallest detectable value is usually related to the noise floor, which corresponds to the ENI here. According to Table 3 the ENI is approximately 200 nA rms. Hence, the dynamic range of the system was approximately 50,000 A/A or 15.6 bits.

2.5 Acquisition and Digitization

The peak amplitude of the shaper is captured using a flip-around T&H circuit based on the bottom-plate sampling method [16]. The advantage of this technique is that it reduces the effect of charge injection and provides better linearity.

The digitization is based on the Wilkinson ADC architecture controlled by a finite state machine (FSM), as shown

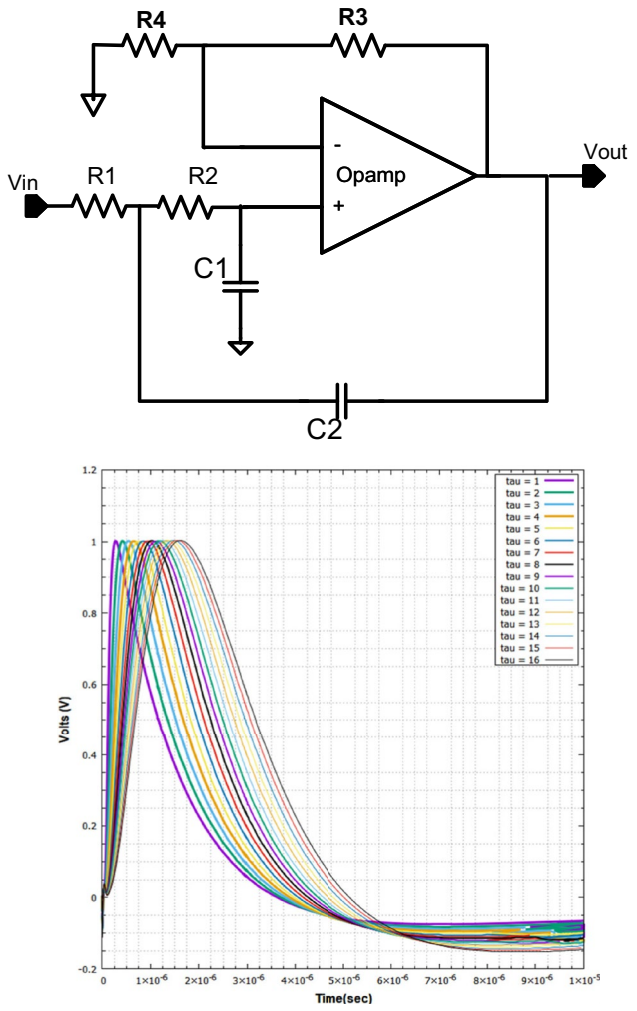

Fig. 6 (Color online) **Top:** Sallen–Key filter for shaper implementation. **Bottom:** Normalized shaper response for different peaking times. Simulation results for a conventional corner at 27 °C

in Fig. 8. The system lies in a steady state until either an internal or external trigger ("FrameSync" signal in Fig. 2) occurs. Figure 9 (top) shows a timing diagram describing the operation of the ASIC in the external trigger mode. After the trigger signal arrives, the system waits for a given number of clock cycles (programmable), during which the shaped analog peak is expected to occur. After this period, T&H is set to hold, such that the output remains constant. Simultaneously, a linear ramp generator (common to all channels) starts charging its internal capacitor and generates a V_{RAMP} signal. The ramp duration is adjusted to approximately 40 μs to reach the full-scale voltage. During this period, the latched comparator transitions from low to high when the ramp overpasses the hold signal of T&H; the higher the voltage, the later the transition.

In parallel, a binary counter counts the number of clock cycles that occur from the start of conversion (SoC) until the ramp crosses the signal level stored in T&H. The SoC signal is connected to the counter and generated by a comparator connected to the V_{RAMP} signal with a threshold set slightly above the baseline level of the ramp. This provides a fixed starting point for the ADC counter. Thus, a well-defined pedestal signal (corresponding to the T&H output quiescent DC level with no input signal) is generated, as shown in Fig. 9 (bottom). The pedestal is subsequently removed. Pedestal subtraction eliminates errors owing to different variations in the DC level between channels. An end of conversion (EoC) signal is generated based on an additional comparator with a threshold V_{FS}, which sets the full-scale (FS) range of the ADC. The converted value V_{FS} can be acquired for calibration. The EoC signal uses the FSM to rearm the ADC logic.

With a 50 MHz clock and a ramp time of 40 μs, the Wilkinson ADC achieves a 12-bit resolution, where the most significant bit (MSB) is given by the path selection comparator and 11 bits are given by the latched value of the counter. Considering the conversion and serialization times, the maximum event rate is approximately 10 kHz. Data were serialized and transmitted with a differential scalable low-voltage signaling (SLVS) driver, and analog electronics were rearranged for the next conversion.

Radiation-tolerant techniques have been used to prevent errors originating from single-event effects (SEEs). Layout techniques were applied to minimize the single-event latch-up probability. Triple-modular redundancy was applied to the configuration registers and state machines to prevent single-event upsets. The I^2C interface is implemented using a synchronous state machine to prevent the occurrence of errors from single-event transients.

3 Materials and methods

We developed a BETA measurement kit available upon request, which is almost plug-and-play and can be used to easily configure the ASIC and exploit its functionalities. It consists of two printed circuit boards (PCBs): a B-HER board and a B-MAX board. Figure 10 shows the BETA measurement kit for BETA-16 (a 16-channel version of BETA).

The B-HER board can hold up to four ASICs and has dedicated connectors to plug into the SiPM arrays. An additional pin input allows for the connection of a single SiPM. Finally, the user can inject an electric signal through a dedicated input (SMA connector type). The board also includes a test buffer that allows the monitoring of the analog response of the different processing stages in all channels from one of the ASICs.

The B-MAX board contains field-programmable gate arrays (FPGAs) that are used to control and configure the ASIC. It can be connected via USB to a PC, where the user

Table 3 Simulation results corresponding to the main shaper performance parameters for different process and temperature corners

Parameter	TT 27 °C	SS −20 °C	SS 20 °C	SS 80 °C	FF −20 °C	FF 20 °C	FF 80 °C	FS −20 °C	FS 20 °C	FS 80 °C	SF −20 °C	SF 20 °C	SF 80 °C
Power[a] (μW)	124	80	87	101	170	192	229	105	116	134	122	138	165
Bandwidth[b] (kHz)	322	226	228	229	482	486	487	320	322	321	318	321	323
Voltage gain[b] (dB)	4.9	4.8	4.8	4.8	5.0	5.0	4.9	4.9	4.9	4.8	4.9	4.9	4.9
Transimpedance gain[c] ($k\Omega$)	2.7	2.2	2.4	2.5	2.5	2.7	2.9	2.6	2.7	2.9	2.5	2.7	2.9
Peaking time (μs)	0.90	1.17	1.26	1.24	0.63	0.62	0.63	0.91	0.91	0.89	0.85	0.86	0.90
Output noise[d] (μV rms)	542	449	488	547	562	611	685	499	542	622	488	531	597
ENI[e] (nA rms)	201	202	207	215	222	229	239	195	199	214	194	200	207

[a] Includes HG filter and shaper power consumption

[b] Bandwidth and low-frequency voltage gain of the preamplifier from AC simulation

[c] Gain is defined as the ratio of shaper peak output voltage to input peak current (transient simulation)

[d] Integrated noise at the shaper output for a conventional detector (SiPM S13552-10) with a capacitance of 30 pF. Includes the noise contributions of the preamplifier and all the previous analog building blocks

[e] Equivalent noise input current for a typical detector capacitance of 30 pF (SiPM S13552-10). It is computed as the ratio of the integrated noise at the output of the shaper to the transimpedance gain

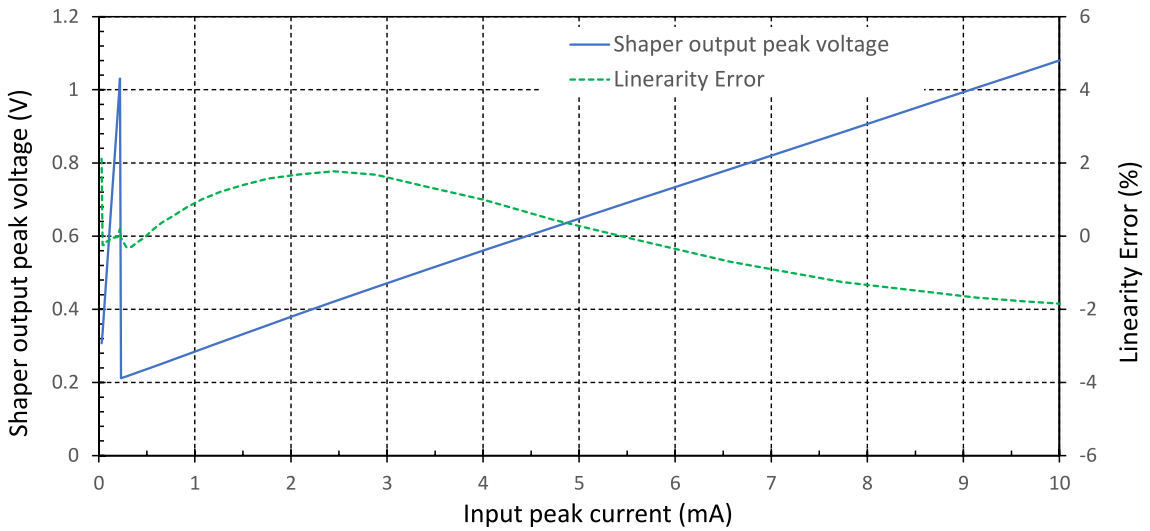

Fig. 7 Shaper peak output voltage and corresponding linearity error as a function of input peak current from transient simulations. The input signal shape follows the typical shape of the single cell signal of the S13552-10 SiPM and is linearly scaled to reach a 10 mA input peak current

can control via software the different registers of the ASIC, launch acquisitions and receive digitized data.

Among the several functionalities that the ASIC offers, the user can configure the gain of the preamplifiers and shaper, and the individual channel thresholds, and work with different trigger modes: internal, external, triggered by the FPGA clock or coincidence triggers of two or more ASICs. The user can also adjust the threshold of

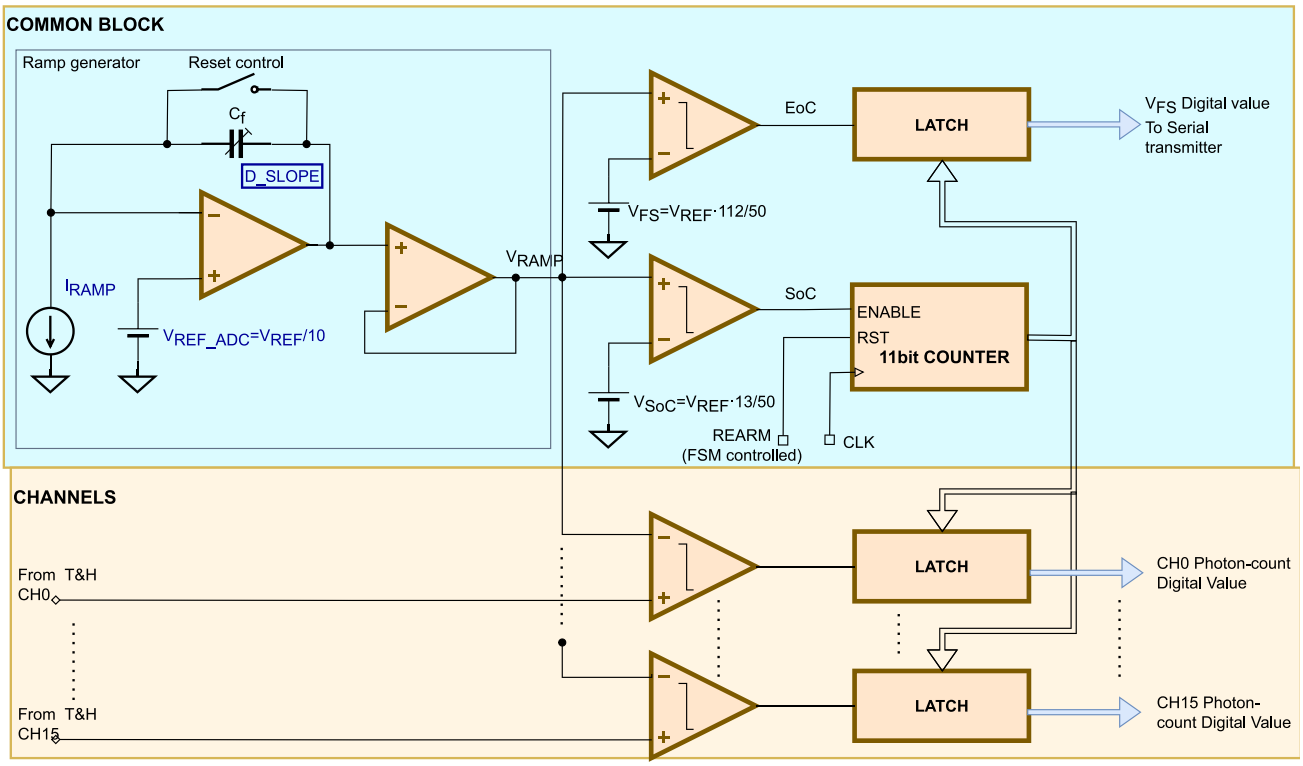

Fig. 8 Wilkinson ADC block diagram

the automatic path selection, which determines whether the HG or LG path will be digitized, or even override this path selection, forcing one of the two gains.

3.1 Linearity of the energy measurement

A linearity test was performed using an electrical pulse injected directly into the BETA ASIC, as shown in Fig. 11. An arbitrary waveform generator (Agilent 33250A 80 MHz) emulating the SiPM signal response sent the pulse to a programmable attenuator (Agilent 11713B). Thus, a wide range of attenuation factors can be swept to study the behavior of the ASIC with several signal amplitudes and, therefore, different input currents. The energy (charge) measurement can be taken using either the standard digitization path (on-chip ADC) or, for characterization, by reading the output signal of any internal analog block with an oscilloscope using the on-chip analog output buffer. For debugging purposes, the linearity and pulse shape of the internal stages (preamplifier, shaper and T&H) were studied using a Keysight MSOX3094T 350 MHz oscilloscope (5 GS/s).

3.2 Measurements with SiPM sensors

The setup used to take low-light-level measurements is shown in Fig. 12. The BETA measurement kit and the SiPMs were placed in a dark box. This was used to evaluate the single photoelectron response, charge resolution and timing resolution. An external trigger generator sends a signal to both the laser driver and oscilloscope. The laser driver (picosecond laser diode system "PiL040X" from Advanced Laser Diode Systems A.L.S. GmbH) generates a pulse at 405 nm that, according to the specifications, has a width < 45 ps FWHM. The laser flashes pass through a single-mode fiber (Thorlabs 305A-FC SM) toward a beam collimator. The fiber is coupled to a Thorlabs liquid-crystal optical beam attenuator, which can change the attenuation factor depending on the applied voltage (from 0 to 5 V, minimum to maximum attenuation, respectively). Finally, the beam pulse arrives at the Thorlabs N-BK7 ground-glass diffuser and spreads the light homogeneously over the sensor.

3.3 Signal-to-Noise Ratio

To evaluate the SNR performance, the laser intensity was adjusted to obtain the mean detected flux of a few photons. We acquired a SiPM signal digitized with BETA and generated histograms with the collected charge to obtain the characteristic few-photoelectron spectra of SiPMs. The SNR was evaluated as $\frac{\mu_1-\mu_0}{\sigma_0}$, where μ_1 and μ_0 are the positions of the first photoelectron and pedestal peaks, respectively, and σ_0

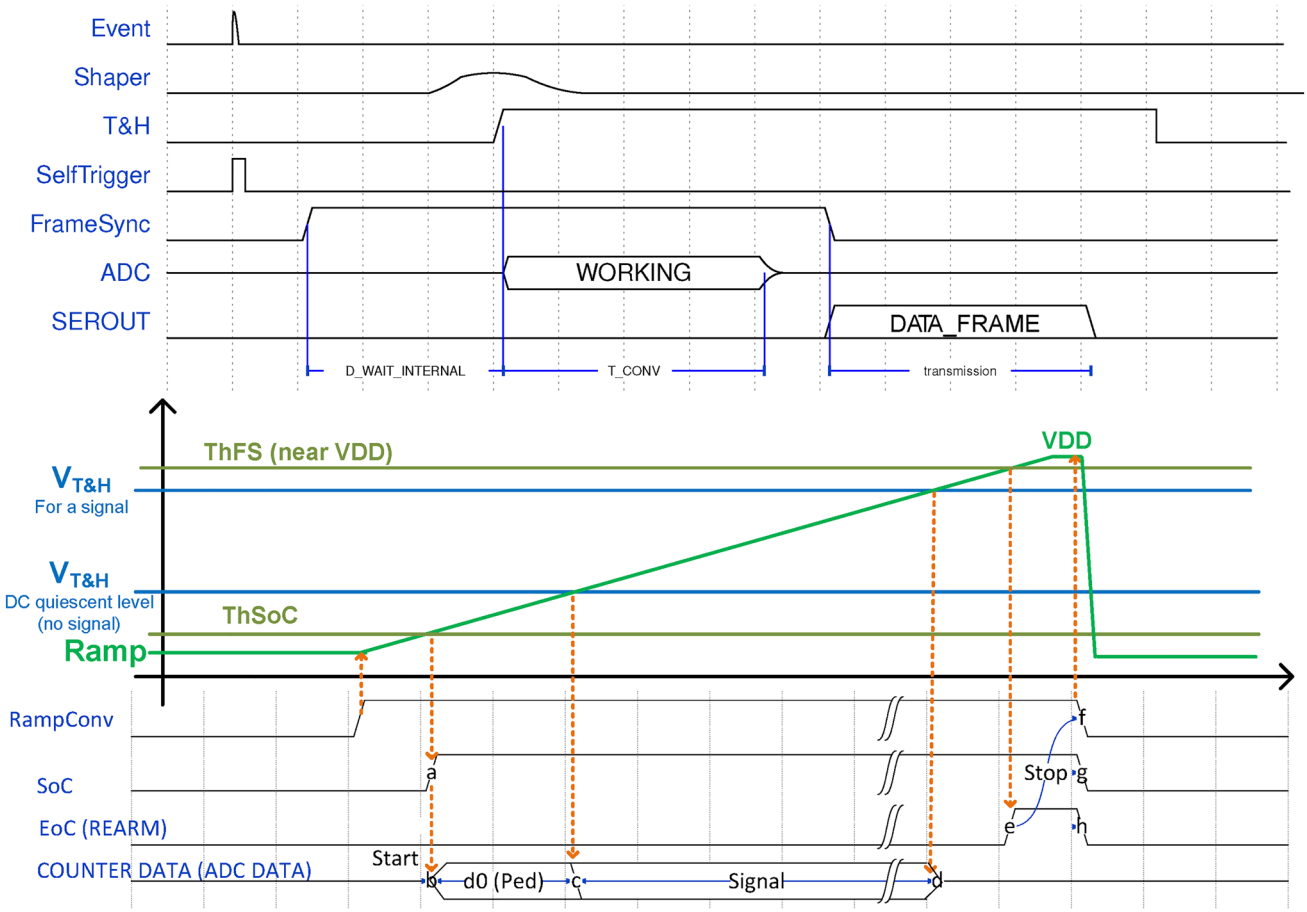

Fig. 9 **Top:** Timing diagram for data conversion in external trigger mode, representing analog processing, digitization and transmission. **Bottom:** Timing diagram of the Wilkinson ADC operation

is the standard deviation of the pedestal. The pedestal represents the signal acquired in the absence of an event and therefore captures the level of electronic noise.

3.4 Timing performance

The timing performance was evaluated by calculating the single-photon time resolution (SPTR) and generalizing the "N-photon" time resolution (NPTR). For these measurements, we adjusted the laser intensities to achieve fluxes of a few photons in the detector plane. Data were acquired using an Agilent MSO 9404A 4 GHz oscilloscope (20 GS/s). More specifically, the laser trigger and trigger signal generated by the BETA leading-edge trigger comparator output signal, which defines a time stamp, were captured. The delay distribution between the trigger and SiPM signal timestamps was used to compute the timing resolution. The number of photons is obtained based on the width of the trigger signal from the BETA ASIC, which follows a nonlinear behavior with respect to the number of photons or the amplitude of the pulse. By applying proper cuts to the width of the signal, it is possible to identify events with different numbers of detected photons. Each delay distribution corresponding to the events of a selected number of photons was fitted with either a Gaussian function or a combination of Gaussian and exponential distributions, where the FWHM value of the fitted distribution corresponded to the SPTR (or NPTR) in FWHM.

4 Characterization results

4.1 Evaluation of the BETA ASIC in the laboratory

We evaluated the performance of the BETA ASIC using the measurement kit described in Sect. 3. We tested the proposed system using different SiPMs. The main generic performance parameters of BETA ASIC are summarized in Table 4. The BETA ASIC not only fulfills the initial

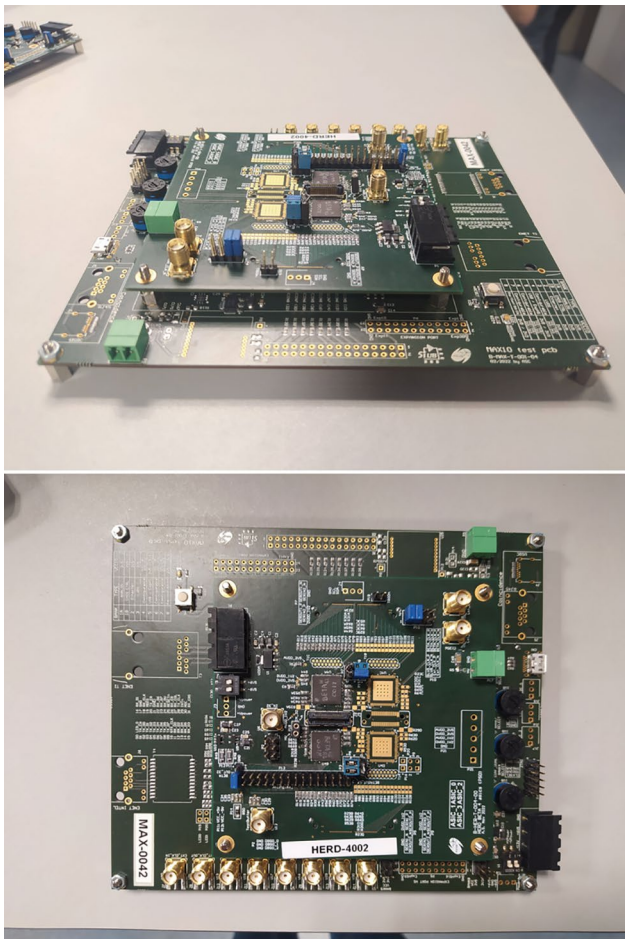

Fig. 10 (Color online) **Top:** BETA measurement kit, which consists of a B-HER board that holds the BETA ASICs. **Bottom:** B-MAX FPGA motherboard

requirements imposed by the HERD mission but also has a large dynamic range and low power consumption, making the ASIC suitable for most space applications. The power consumption is expected to be less than 1 mW/channel in the 64-channel version of the ASIC (BETA-64). The 16-channel version of the chip (BETA-16) includes an output driver per channel with a power consumption of 400 μW/channel, which is absent in the 64-channel version of the chip.

The linearity and dynamic range of the BETA ASIC were evaluated using the setup shown in Fig. 11. The linearity at different internal processing stages (preamplifier, LPF, shaper and T&H) was evaluated using different path selection configurations: path selection fixed to HG, path selection fixed to LG or automatic path selection. As shown in Fig. 13, the linearity error was less than 3% with no correction for the on-chip analog output buffer and acquisition (probes and oscilloscope) nonlinearity. The switching point from HG to LG was clearly observed in automatic path selection mode.

Linearity measurements based on the BETA on-chip ADC were taken. The results are shown in Fig. 14 for different configurations of HG and LG. The linearity error is also shown. Notably, it is equal to or less than the error obtained from previous measurements based on an oscilloscope (see Fig. 13). The linearity error was less than 2% below the saturation of each gain configuration. For the lowest gain configuration of the LG path, a range of 12 mA input peak currents can be achieved without saturation. The linearity error in Fig. 13 is higher because these measurements include two additional elements: the oscilloscope and the analog output buffer of the chip, which must drive large capacitive loads (capacitance from the output pads and PCB traces and components). The nonlinearity of these elements is not corrected and can be important, particularly because of the slew rate limitation of the analog output buffer. Conversely, this buffer is not required for measurements based on the internal ADC, as shown in Fig. 14. In standard data acquisition, an on-chip ADC is used, and an analog output buffer is not required. It is only used for characterization or debugging.

Figure 15 shows the charge spectra obtained in a single ASIC used to read out 16 of the 128 SiPMs of one of the Hamamatsu S13552-10 custom-made arrays equipped with the FIT modules. As mentioned above, each channel of the array has 3749 (23×163) microcells of 10 μm [2]. This array, with its small microcell size, is optimized to achieve a large dynamic range in a few mm^2. Although SiPMs with small microcells have a lower gain than those with larger microcells, with this array, we can achieve an SNR of ~ 5 at the single-phe level. As shown in the plot, this SNR is sufficient to clearly identify at least the first ten phe peaks. These values were obtained using the nominal gain of the BETA preamplifiers: ~10 for the HG path and ~0.45 for the LG path. A higher SNR can be achieved using a higher-gain configuration at the expense of a lower dynamic range of the HG path.

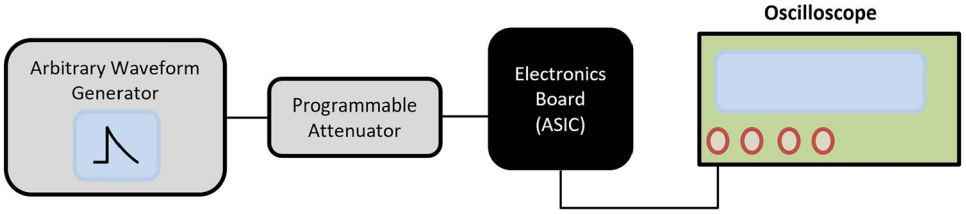

Fig. 11 (Color online) Schematic representation of the experimental setup used to evaluate the linearity of the energy measurement

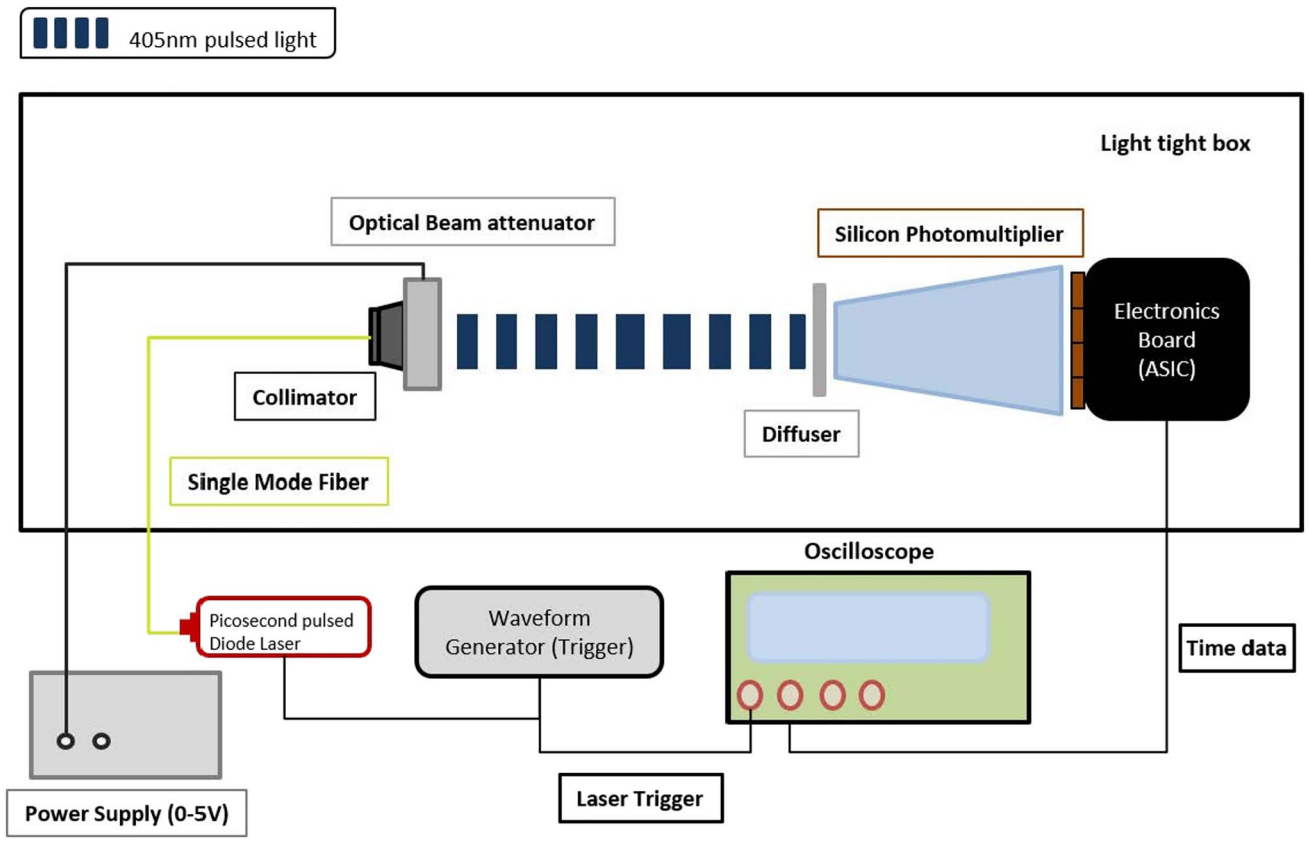

Fig. 12 (Color online) Schematic representation of the experimental setup using the blue laser source for SiPM and SPTR measurements

Table 4 Summary of the main performance parameters of the BETA ASIC

Number of channels	16[a]/64[b]
Power consumption	1.4 mW/channel[a]/1 mW/channel[b]
Preamplifier gain (HG path)	6 – 70
Preamplifier gain (LG path)	0.25 – 3.75
SNR (single-phe[c])	> 5
Max. signal range	~10 mA peak[c]
Linearity error (full range)	< 2%
Maximum operation rate	10 kHz

[a]BETA-16 and [b]BETA-64

[c] phe: photoelectron or detected photon

[d] This corresponds to about ~ 4000 phe for S13552-10 SiPM at 3 V overvoltage

The BETA chip was also characterized using a single Hamamatsu S13360-1350CS SiPM (with an area of ~ 1.3 mm × 1.3 mm). With a 50 μm microcell size, this SiPM has an intrinsically higher gain than that used for the FIT; thus, we could achieve an SNR of ~ 10 using the nominal gain of BETA. Figure 16 shows the single-phe spectrum obtained using this sensor. To produce this plot, we intentionally varied the intensity of the laser during the acquisition and overrode the path selection, forcing the HG path to show that using the ASIC enables the identification of peaks corresponding to events of 1 to above 20 phes.

Even if the ASIC is not designed for fast-timing applications, the time resolution of the system (SiPM + ASIC) can be studied using the trigger signal, which is the OR of the trigger signal from the 16 channels. The output is a binary pulse, where the information of the arrival time of the signal is encoded in its rising edge, and its width is related (nonlinearly) to the amplitude of the signal. As shown in the top panel of Fig. 17, the number of phes recorded in an event can be identified by plotting the arrival time of the trigger signal (the delay with respect to the trigger given by the laser) versus its width. Using this information, we evaluated the time resolution of the system for input signals with different light intensities. With the S13360-1350CS SiPM, the time resolution for signals above 10 phe was below the 400 ps FWHM.

The important parameters for trigger applications are the trigger signal propagation delay and walking time. These parameters are evaluated using an electrical

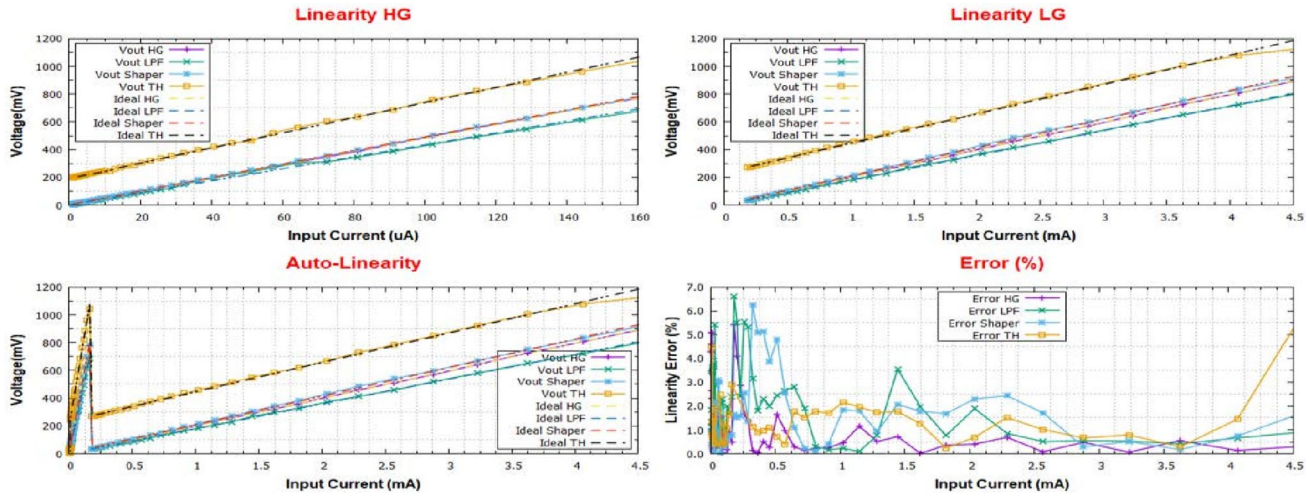

Fig. 13 (Color online) Linearity of BETA internal stages for different configurations of path selection control: HG (top left), LG (top right) and automatic (bottom left). The linearity error is also shown (bottom right)

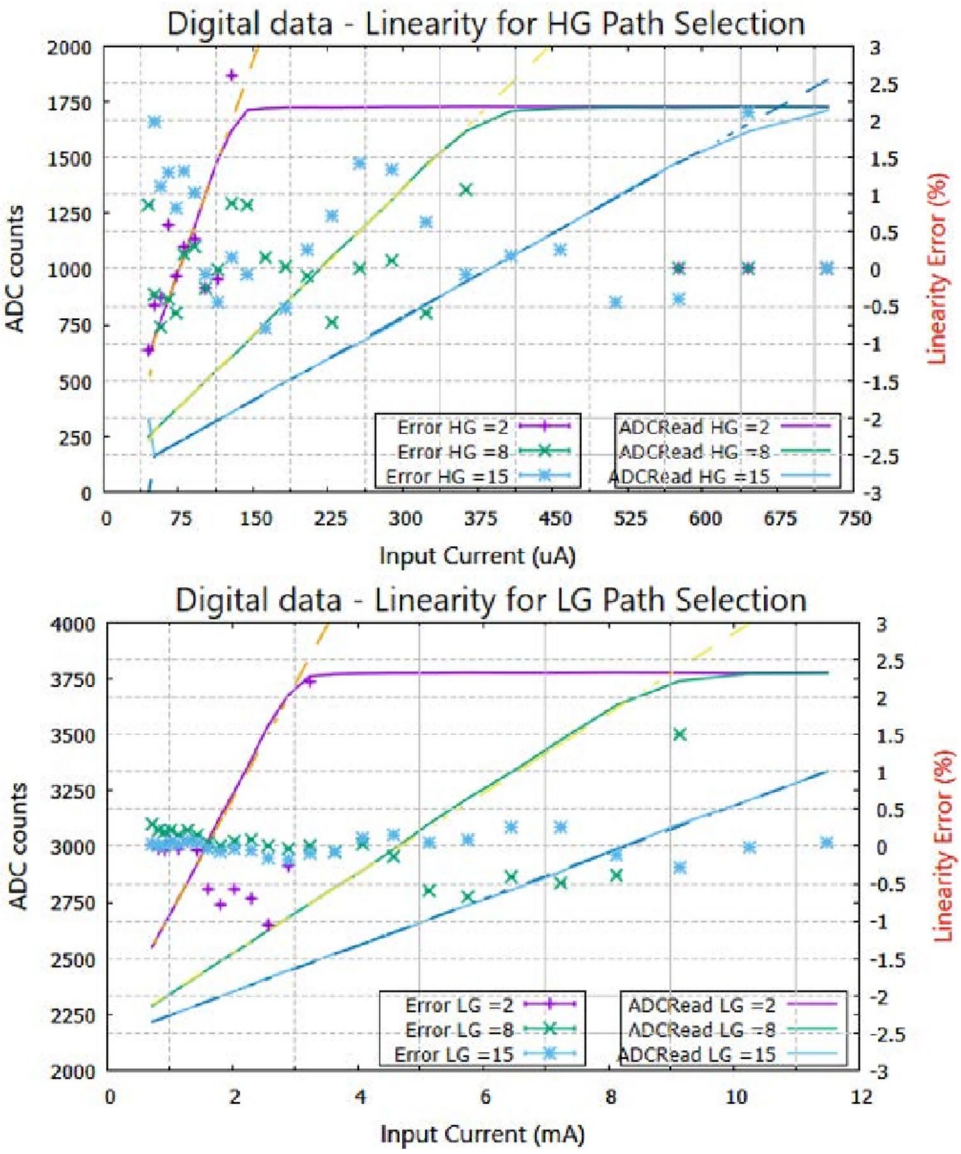

Fig. 14 (Color online) Linearity measurements of the BETA ASIC full chain, including ADC, for different configurations. **Top:** HG path. **Bottom:** LG path

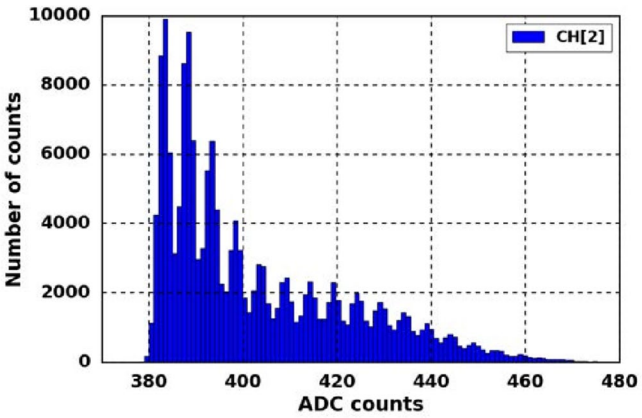

Fig. 15 Single-phe spectra recorded in 1 channel of the Hamamatsu S13552-10 array that were exposed to laser pulses

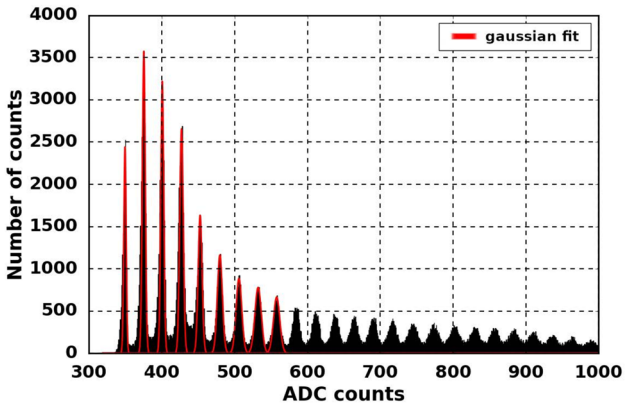

Fig. 16 Single-phe spectrum recorded with a S13360-1350CS SiPM. The intensity of the laser was modified during the acquisition to obtain pulses from 1 to above 20 phe

injection setup to measure the absolute delay introduced by the BETA ASIC. The results are depicted in Fig. 18, which shows that the trigger signal delay is less than 30 ns for a single-photon signal. Typically, the trigger is set to a higher level, above 3 phes, where the delay is less than 20 ns and the time walk with respect to events with a larger number of detected photons is below 5 ns.

4.2 Evaluation of the BETA ASIC for the FIT detector in the SPS test beam area at CERN.

The HERD BETA measurement kit was placed in the test beam area at CERN to test the behavior of the ASIC for the FIT detector. An S13552-10 SiPM array with 64 channels, coupled to a fiber mat, was read using four BETA chips, as shown in Fig. 19. The fibers were manufactured by Kuraray3 (type SCSF-78MJ) and had an average diameter of 250 µm [2].

A 20 GeV proton beam was used, and only 2-3 fibers were hit per event. The ASIC was configured in the external trigger mode, and the trigger was provided by another HERD subsystem, in this case, the PSD. Data were acquired with BETA ASICs using the ADC output and processed externally on a computer.

Figure 20 shows the single-phe spectra of ADC acquisition when summing the data from all 16 channels in a BETA ASIC after pedestal calibration. The pedestal was initially measured in the absence of a signal to calibrate the DC variations between different channels and then subtracted before summing the responses of all channels in an ASIC. Pedestal events were removed to better illustrate the photon peak distribution. The system was configured in the external trigger mode, and several events were recorded without a signal because of the efficiency of the system and the alignment of the fiber mat with respect to the beam. For this measurement, we manually acquired all data using the HG path.

As shown in Fig. 20, different numbers of photons are clearly identified. Notably, ASIC readout channels behave homogeneously even though the gain of the SiPMs has not been equalized. The mean ADC value measured for each photon (mean obtained by performing a Gaussian fit of the spectra) is shown in Fig. 21. As shown, the linearity error was below 2% for the entire dynamic range of the HG path. The measured SNR was approximately 6.4, indicating good detection sensitivity.

5 Conclusions and outlook

In this study, we describe the key characteristics of the BETA ASIC and evaluate its performance with electrical pulse injection and two different sensors from Hamamatsu: the S13552-10 array developed for FIT and a commercial S13360-1350CS single SiPM.

The experimental results proved that BETA ASIC presents a large dynamic range from ≈ 0.1 phe to ≈ 4000 pe,

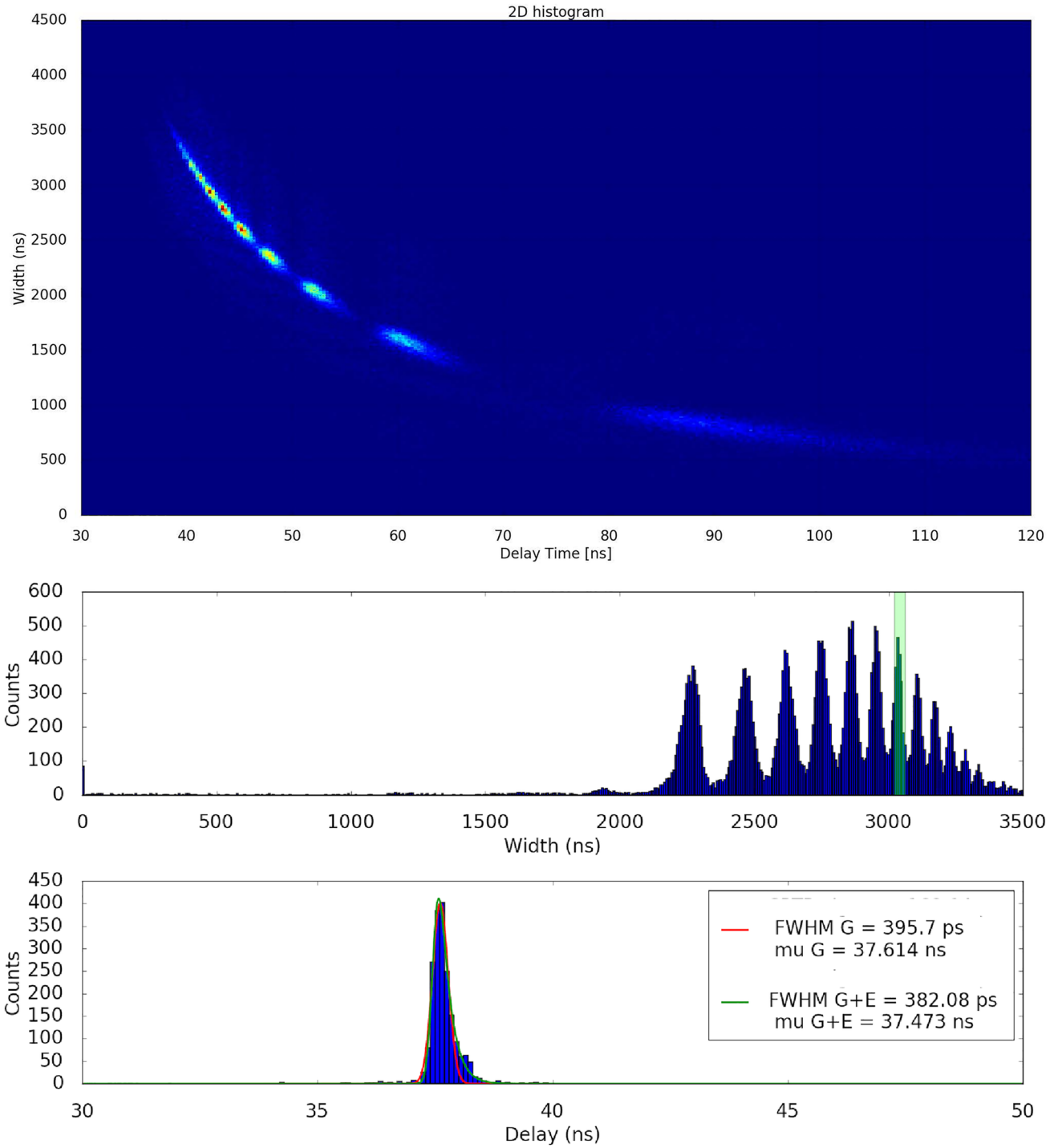

Fig. 17 (Color online) **Top:** Arrival time (delay) versus width of the BETA trigger signal. **Center:** Width distribution of the trigger signal for events over 3 phes. **Bottom:** Arrival time distribution for events of 10 phes. The arrival time distribution has been fitted by two different methods: using a Gaussian (red) and the combination of Gaussian and exponential functions (green)

with a low power consumption of 1.4 mW/channel in the 16-channel version. A power consumption below 1 mW/channel was predicted for the 64-channel version. Experimental measurements for Hamamatsu SiPM S13360-3050CS showed a time resolution of 400 ps FWHM for 10 phe signals, a propagation delay below 20 ns and a time walk below 5 ns.

The first prototype of BETA [17] was developed for the HERD FIT readout; however, after adding additional trigger and readout functionalities, it evolved into a versatile

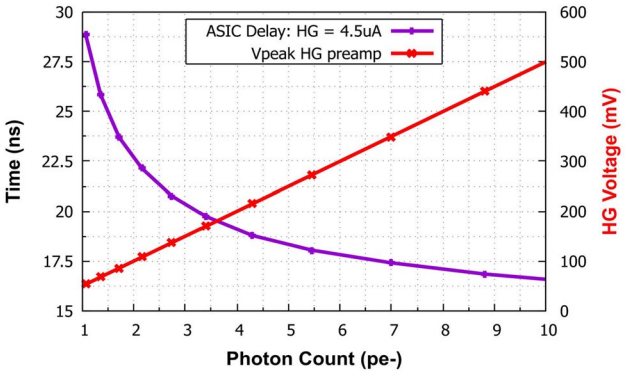

Fig. 18 Trigger signal delay (pink) as a function input signal level. The HG preamplifier output amplitude is also shown (red). Comparator trigger threshold is set to 0.5 photon signal level

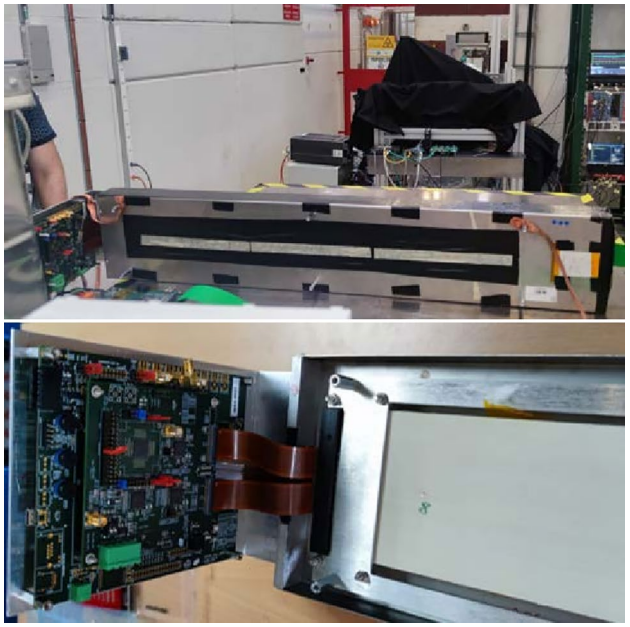

Fig. 19 (Color online) **Top:** HERD BETA measurement kit connected to a fiber mat in a test beam area at CERN. **Bottom:** Connection of the measurement kit to the SiPMs by using a flexible cable

front-end ASIC suitable for SiPM readout in multiple space and low-event-rate (10 kHz) applications: trigger and veto systems, charge measurement, calorimetry, photon counting and time-of-flight counters with moderate timing resolution. Indeed, beyond the HERD experiment, it will be used to develop a new version of the radiation monitor for the LISA missions [18] and is considered for different missions such as NUSES [19] and drone applications such as radiation monitoring.

The fact that BETA provides full signal processing, including digitization, with a power consumption of only 1

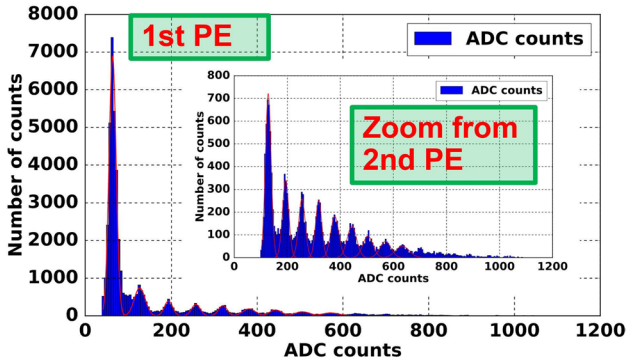

Fig. 20 Single-phe spectra corresponding to the summation of the 16 channels after pedestal calibration. Zoomed image showing events from the second photon are highlighted. No event selection based on coincidences is performed

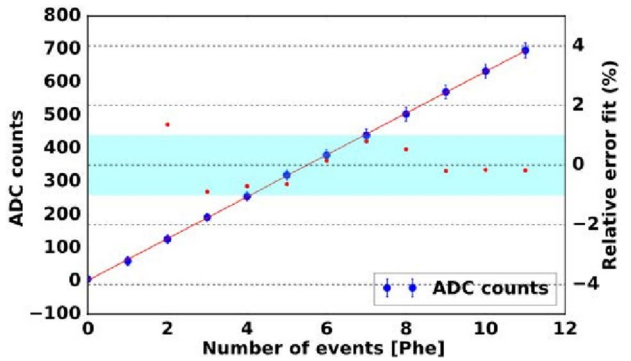

Fig. 21 Mean ADC value detected for each photon and linearity error

mW/channel may significantly simplify front-end systems, such as those proposed for various space missions [20] and CubeSats [21].

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Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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