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Readout electronics for a high-resolution soft X-ray spectrometer based on silicon drift detector

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Abstract The readout electronics for a prototype soft X-ray spectrometer based on silicon drift detector (SDD), for precisely measuring the energy and arrival time of X-ray photons is presented in this paper. The system mainly consists of two parts, i.e., an analog electronics section (including a pre-amplifier, a signal shaper and filter, a constant fraction timing circuit, and a peak hold circuit) and a digital electronics section (including an ADC and a TDC). Test results with X-ray sources show that an energy dynamic range of 1–10 keV with an integral nonlinearity of less than 0.1% can be achieved, and the energy resolution is better than 160 eV @ 5.9 keV FWHM. Using a waveform generator, test results also indicate that time resolution of the electronics system is about 3.7 ns, which is much less than the transit time spread of SDD (<100 ns) and satisfies the requirements of future applications.

Keywords Energy and time measurement · Soft X-ray detection · Silicon drift detector · Readout electronics

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1 Introduction

The X-rays emitted by galaxy clusters, black holes, and neutron stars are important for studying the extraordinary gravitational [1], electromagnetic, and nuclear-physics environments inside neutron stars, and exploring the exotic states of matter, of which the density and pressure are higher than in atomic nuclei [2]. X-rays of pulsars are attractive in autonomous navigation due to their properties of stable, periodic, and predictable signatures [3, 4].

In recent years, several projects of celestial soft X-ray detection in space have been carried out or planned, such as the X-ray Imaging Spectrometer of Suzaku [5], Neutron Star Interior Composition Explorer (NICER) [2], and Large Observatory for X-ray Timing (LOFT) [6]. The Suzaku satellite used charge-coupled devices to observe celestial X-ray sources of 0.2–12 keV. The NICER, scheduled to launch in early 2017, adopts silicon drift detector (SDD) for X-ray timing and spectroscopy of neutron stars in the soft X-ray band. The LOFT, proposed to launch around 2025, will adopt SDD for exploiting and diagnostics of rapid X-ray flux and spectra in 2–50 keV from neutron stars and black holes.

Being able to work at close to room temperature with a Peltier cooler, SDD is considered as an appropriate choice for soft X-ray detection, with high energy resolution and count rate. In SDD, an incoming photon generates a number of electrons and holes. The holes drift toward the back side of the detector, while the electrons drift toward the anode electrode with a proper bias of a set of cathodes [7]. The accumulated charge at the anode is connected to the gate of a field effect transistor, which forms the first stage of a charge sensitive amplifier.

A prototype high-resolution soft X-ray spectrometer is under development at USTC, aimed at conducting astrophysics studies, and pushing forward X-ray-based navigation and X-ray communication in space [8]. The detector, SDD H30 [9] made by KETEK GmbH, Germany, has a maximum input count rate of 1000 kcps and excellent energy resolution. With an active area of 30 mm^2, it is of about 80% at 1 keV and 98% at 10 keV in efficiency. In this paper, the readout electronics and test results are described in detail.

2 The readout electronics

2.1 Architecture

High-resolution time and charge measurement are widely used in nuclear physics [10–12]. Figure 1 shows a block diagram of the soft X-ray detection (SXD) readout electronics for time and energy measurement. It is mainly composed of two sections: analog and a digital electronics. In the analog electronics section, a pre-amplifier module (PA), a high-voltage module (HV), and a temperature control module (TC) are specially designed by the Original Equipment Manufacturer of SDD. All the other modules after the PA are developed by our group. The PA output goes to two channels: The one marked as 'Q_out' from a slow shaper is for energy measurement, and the other marked as 'T_out' from a fast shaper is for time measurement.

In the digital electronics section, the 'Q_out' is fed into an analog peak hold module and then sampled by an analog-to-digital-converter (ADC), while the 'T_out' is converted into a hit signal by a constant fraction timing circuit (CFT) and then sent to a time-to-digital-converter (TDC) for digitization. The ADC and TDC signals are buffered and fed into a data processor (DP). The system can be monitored and controlled by the DP according to the standard controller area network (CAN) protocol. The external power supplies of the whole electronics are ±6, +5, and +12 V.

2.2 Pre-amplifier

As shown in Fig. 2, a matched PA [13] for SDD is used to amplify the output current pulse of the detector, which offers an ultra-low noise, and a ramped reset type CSA with high gain (4.5 mV/keV ± 15%). The amplitude of the ramped output signal is between ±2 V with a reset duration of <5 μs, and the period of the reset ranges from a few milliseconds to a few hundred milliseconds, which depends on the frequency of the incoming photons and the temperature of the detector.

The output of PA is a voltage step when the signal produced by an X-ray photon appears. The rise time (from 10 to 100 ns [14]) mainly depends on the location where X-rays interact with the SDD, while the voltage amplitude depends on the energy deposition of the incoming photon.

2.3 Energy measurement circuit

For energy measurement, the signal amplitude is detected efficiently, achieved via the analog peak detection and ADC method. As shown in Fig. 3, the PA is followed by a slow shaping circuit consisting of a CR-RC^2 filter, which is employed to form a quasi-Gaussian signal. The peak value of the quasi-Gaussian signal is held by a peak hold module (PH300 from Amp-Tek) and then digitalized by a 14-bit ADC (AD9243) with 3 MHz sampling clock. The pole zero cancellation circuit is not necessary in case that being the signal form PA a step voltage [15].

Noise contribution of the SDD and readout electronics is analyzed, to find the performance-limiting factor of the system.

Energy resolution of the detector, staged in the datasheet, is 126.9 eV @ 5.9 keV [9] (at below −60 °C using a Peltier cooler, peaking time of 16 μs). For the slow shaping circuit, a Pspice simulation shows that the noise RMS is 3.4 mV, which is equivalent to 44 eV @ 5.9 keV. A 14-bit ADC with a quantization error of 0.12 mV (1.5 eV @ 5.9 keV) is selected, which shall be a minor role in affecting the total energy resolution.

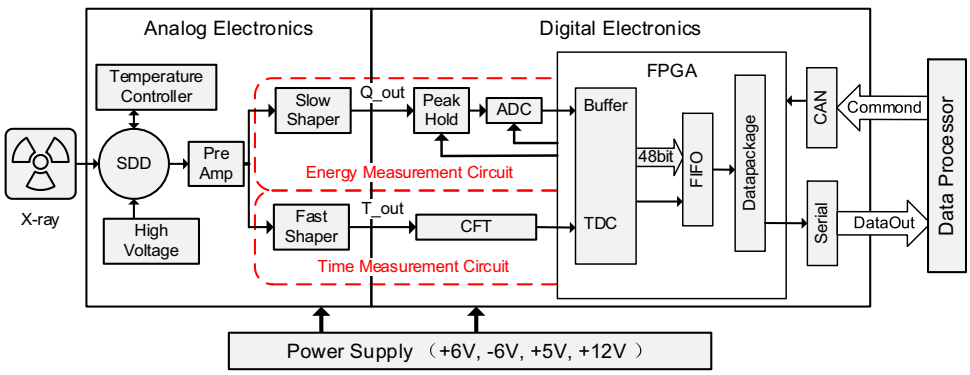

Fig. 1 Block diagram of the SXD readout electronics

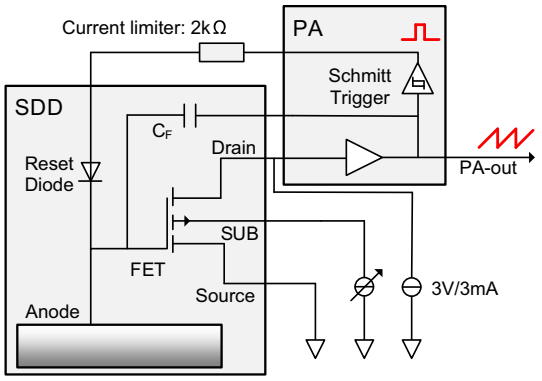

Fig. 2 Block diagram of PA connecting with SDD

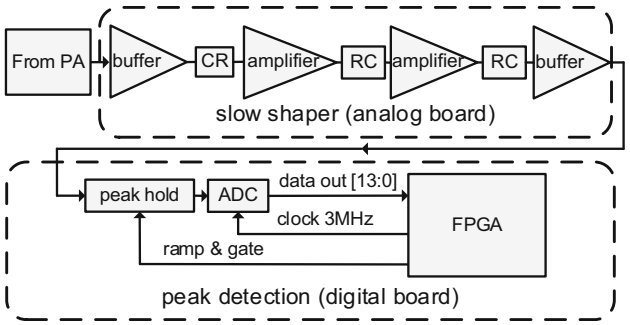

Fig. 3 Block diagram of the energy measurement circuit

In addition, the rise time of the real signal will cause extra loss of the shaped signal height, which is termed as the ballistic deficit. Although increasing the peaking time (i.e., the time constant of CR and RC) can decrease the ballistic deficit, it will increase the dead time of the energy measurement. A peaking time of 2 μs is determined finally to guarantee a proper counting rate and the energy resolution. Test results with a signal generator show that the actual electronic noise ($FWHM_{\text{electronic}}$) of the energy measurement circuit is equivalent to 68 eV @ 5.9 keV as a constant in the dynamic range with a peaking time of 2 μs.

2.4 Time measurement circuit

Compared with leading edge timing, a constant fraction timing circuit essentially eliminates the amplitude-dependent time walk for signals and has better timing resolution [16]. Figure 4 explains the CFT principle briefly, and a delay time 'Δt' of 8 ns as an attenuation coefficient 'q' of 0.5 is chosen, leading to a fixed delay 't' of 16 ns.

As shown in Fig. 5, the PA is followed by a fast shaping circuit, which consists of an AC coupled circuit (CR with a time constant of 0.5 μs) and an amplifier, to condition the signals for time measurement. The fast shaper also drives three branches of the CFT circuits: The first branch is

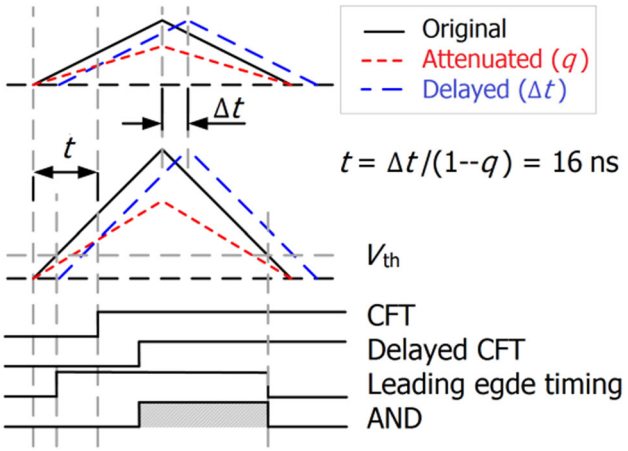

Fig. 4 Brief explanation of the CFT principle. The delay 't' is constant and independent from the slope of the input signal

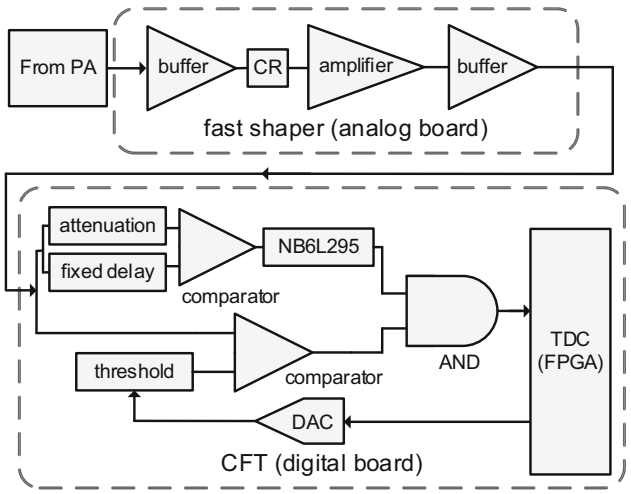

Fig. 5 Block diagram of the time measurement circuit

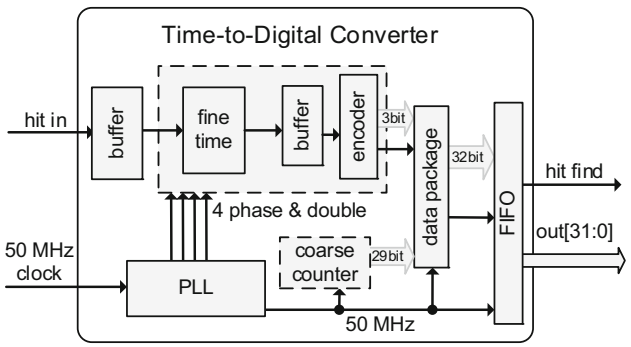

Fig. 6 TDC integrated in the FPGA. 3-bit 'fine time' and 29-bit 'coarse counter' constitutes a final 32-bit time measurement result (with the bin size of 2.5 ns and dynamic range of 10.74 s)

delayed by a time of 't_d' (8 ns), the second one is attenuated by a coefficient of 'q' (0.5), and the third one is compared with an adjustable threshold for noise canceling.

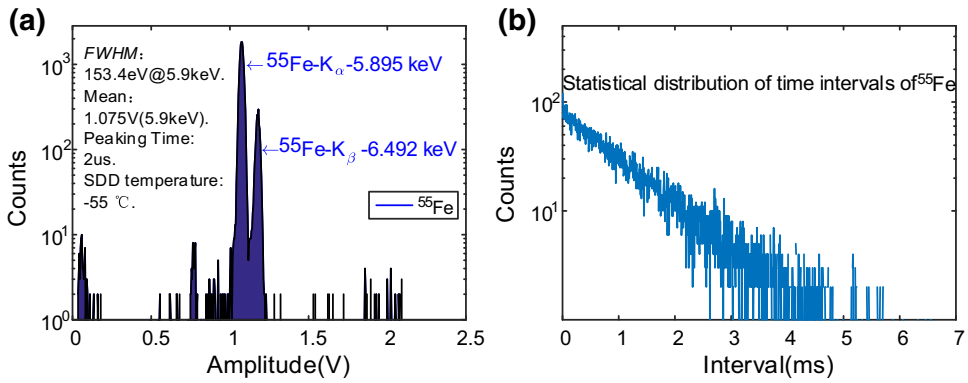

Fig. 7 Energy spectra (**a**) and time interval distribution (**b**) of a ^{55}Fe using the SXD system

Table 1 X-ray fluorescence used for the calibration of the SXD

X-ray	Cu–K_β	Cu–K_α	Fe–K_β	Fe–K_α	Cr–K_β	Cr–K_α	Ti–K_β	Ti–K_α
Energy (keV)	8.91	8.04	7.06	6.40	5.95	5.41	4.93	4.51
Mean[a] (code)	5583	5072	4479	4091	3821	3503	3212	2960
INL (%)	−0.05	0.07	0.06	0.03	0.01	0.07	−0.02	−0.04
$FWHM_{all}$ (eV)	163.2	162.1	149.1	148.0	138.8	137.6	127.7	126.8
$FWHM^{b}_{Fano}$ (eV)	148.4	147.2	132.7	131.5	121.0	119.6	108.1	107.0

[a] Mean is the peak position expressed in ADC channels

[b] $FWHM_{Fano} = (FWHM^2_{all} - FWHM^2_{electronic})^{1/2}$. $FWHM_{electronic}$ is about 68 eV as a constant

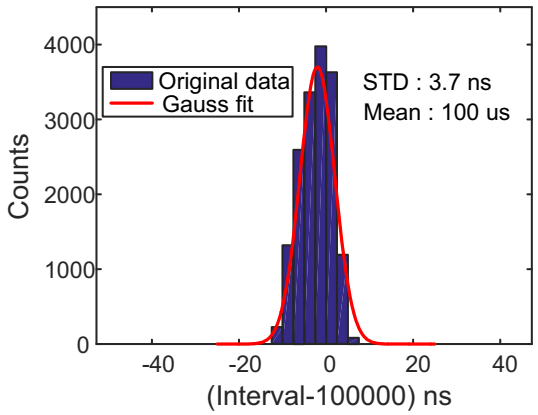

Fig. 8 Performance of time precision test with 10 kHz (period of 100 μs) pulse input

The output of both comparators is fed into an 'AND' gate for coincidence and then digitized by an FPGA based TDC.

Since accuracy of time measurement is highly sensitive to CFT circuit, stringent hardware design is considered. A 100-Ω impedance fixed delay line (1919-20B, Data Delay Device) is used to achieve high-precision delay and impedance matching. An ultra-high-speed comparator (MAX9601, MAXIM Inc.) is selected, with 30-ps propagation delay dispersion and differential PECL outputs. A programmable delay line (NB6L295 from ON semiconductor) configured at 5 ns is used to delay the CFT branch to guarantee the timing constrain. The AND gate (MC100LVEL05,ON Semiconductor) has two differential ECL inputs with a propagation delay of 340 ps.

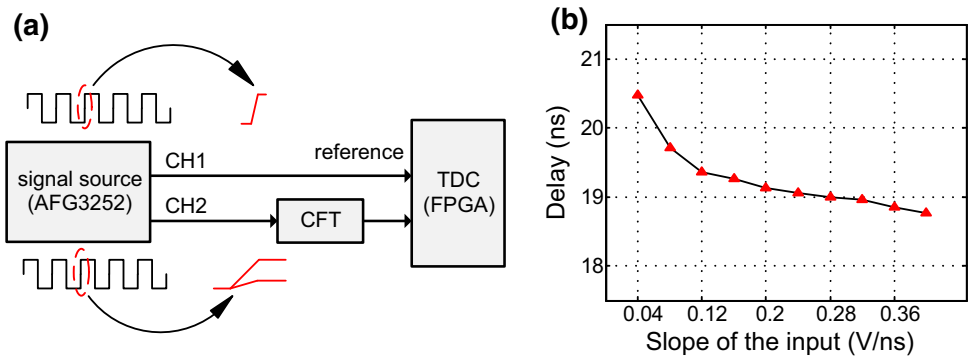

Fig. 9 Test method (**a**) and results (**b**) of the CFT circuit. Delay is the skew of the 'reference' and the output of 'CFT'

2.5 TDC integrated in FPGA

To digitize the output signals from the CFT module, a TDC is implemented in a XILINX FPGA (XC5VLX110), which reduces the system complexity and provides good flexibility [17, 18]. Figure 6 shows its block diagram. The arrival time of the 'hit in' signal is digitized by a 3-bit 'fine time' and a 29-bit 'coarse counter' modules and then encoded to a final 32-bit time measurement result, which is finally read out by a FIFO.

A 50-MHz external clock is fed into the FPGA and then used by an internal phase lock loop (PLL) to generate four 100-MHz clock outputs with 90° phase interval (0°, 90°, 180°, 270°), which is equivalent to 2.5 ns least significant bit (LSB) and much less than the transit time spread of SDD.

3 Test results

The test platform to evaluate performance of the system mainly consists of a power supply (KEITHLEY 2230-30-1), a signal source (Tektronix AFG3252), an oscilloscope (Tektronix DPO5104), a ^{55}Fe X-ray source, and the aforementioned analog electronics module and digital electronics module. A series of tests are conducted to evaluate performance of the SXD readout electronics.

3.1 Energy measurement results

On the SXD system, using the ^{55}Fe source, the energy resolution is measured at 153.4 eV @ 5.9 keV *FWHM* (Fig. 7a). Statistical distribution of time intervals of two photons is shown in Fig. 7b, where the counts have the characteristic of Poisson distribution and behave in accordance with the theoretical property of radioisotope.

The energy resolution and linearity (properties of the detector and electronics) X-rays of different energies are listed in Table 1. The X-rays are electron beam-induced fluorescence from samples of Cu, Fe, Cr, and Ti [19]. The linearity of one representative SDD indicates that the integral nonlinearity (INL) of less than 0.1% can be achieved. It is worth noting that the minor INL can be corrected by off-line analysis.

3.2 Time measurement results

The RMS of time measurement is basically contributed by two factors: the noise of circuits and the quantization error. A 10-kHz pulse (30 ns rise time, 50 mV amplitude, generated by a Tektronix AFG3252) is utilized to drive the fast shaper module directly, to evaluate the performance of time measurement. Test results of the SXD (including contribution of both analog and digital electronics) are shown in Fig. 8. It can be seen that the standard deviation (STD) is 3.7 ns, which is much less than the transit time spread of SDD.

As mentioned in Sect. 3.3, CFT essentially eliminates the amplitude-dependent time walk for signals. Figure 9a shows the tests to observe performance of the CFT circuit. The first channel (CH1) is the reference signal with a frequency of 10 kHz and 2.5-ns rise time, while CH2 is created based on waveform of the fast shaper, which has different amplitudes (0.4–4 V) with 10-ns rise time. Figure 9b shows the performance of CFT circuit. The propagation delay of CFT circuit is 20 ns with the time walk less than 3 ns.

4 Conclusion

The readout electronics system for a prototype soft X-ray spectrometer with SDD is successfully implemented, and good time and energy measurement performance are achieved. A time measurement resolution below 5 ns is obtained. The energy resolution is 153.4 eV *FWHM* @ 5.9 keV with analog peak detection and ADC method. XRF tests indicate that the INL is less than 0.1% with a dynamic range of 1–10 keV. All these show that the SXD system has broad potential for X-ray timing and observation missions in space.

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