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Prototype of the readout electronics for the RICH PID detector in the STCF

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Abstract The ring imaging Cherenkov (RICH) detector for particle identification (PID) is being evaluated for the future super tau-charm facility (STCF) complex. In this work, the prototype readout electronics for the RICH PID detector is designed. The prototype RICH PID detector is based on a thick gas electron multiplier combined with a micromegas detector for Cherenkov light detection. Considering that there will be a large number ($\sim$ 690,000) of detector channels in future RICH detector, the readout electronics faces many challenges to precisely measuring time and charge information, such as reducing the noise, increasing density, and improving precision. The requirements of the readout electronics are explored, the down-selection of the ASICs is made and thus a prototype readout electronics is designed and implemented. Tests are also conducted to evaluate the performance of the prototype readout electronics, and the results indicate that the time resolution is better than $\sim$ 1 ns (RMS) when the input charge is greater than $\sim$ 12 fC based on the APV25 chip, while the time resolution is better than $\sim$ 1 ns (RMS) at an input charge of over $\sim$ 48 fC based on the AGET and STCF ASIC chips, and the equivalent noise charge is better than $\sim$ 0.5 fC (RMS) @ 20 pF based on the three ASICs. The test results indicate that the prototype readout electronics design meets the requirement of the future RICH PID detector and thus provides a reference for future engineering.

Keywords Readout electronics · Time measurement · Charge measurement · RICH PID detector · STCF

1 Introduction

The super tau-charm facility (STCF)[1, 2], with a center-of-mass energy range between 2 and 7 GeV and a peak luminosity of 0.5×10^{35} cm^{-2} s^{-1}, is a symmetric electron–positron collider that has been proposed in China for construction after the Beijing electron-positron collider II (BEPC-II)[3, 4]. Some of the key detectors are in the research and development stage; one of these detectors is the barrel detector for particle identification (PID), which plays an important role in the whole STCF. A good PID is required for the STCF, especially in the search for exotic particles and physics beyond the standard model. Charged hadrons with a momentum of up to 2 GeV/c require a dedicated PID detector to obtain the particle separation between the π-meson, K-meson, and proton[5]. Owing to their broad momentum range, detectors based on the Cherenkov radiation are widely used for PID in high-energy particle experiments. By accurately measuring the Cherenkov emission angle, the momentum of the particle can be obtained to identify the particle. The ring imaging

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Cherenkov (RICH)[6] technique is a suitable candidate for PID within a momentum of up to 2 GeV/c at the STCF barrel region. In the STCF RICH PID detector, micropattern gas detector (MPGD) photon detectors are being evaluated. Gaseous photon detectors are still the only available option to instrument detection surfaces when insensitivity to a magnetic field, low material budget, and affordable costs are required in view of the large detection systems[7–9].

The prototype RICH PID detector is based on a hybrid MPGD combination, consisting of a thick gas electron multiplier (THGEM) followed by a resistive micromegas (MM) on a pad segmented anode[10–12]. The THGEM also acts as a reflective photocathode: its top face is coated with a CsI film[13]. The feedback from the photons generated in the multiplication process is suppressed by the presence of the THGEM, while the large majority of the ions obtained from the multiplication are trapped in the MM stage. The total gain of the prototype RICH PID detector for a single photoelectron is around 10^5. To evaluate the performance of the prototype RICH PID detector and explore the integration solution for a large-scale system, a high-density readout electronics with the capability of precise charge and time measurements is studied in this work. In Sect. 2, the prototype readout electronics is described in detail, and the design methods of each submodule are discussed in Sect. 3. In Sect. 4, the measurement of several parameters that permit the estimation of the performance of the system is presented.

2 Prototype readout electronics for the RICH PID detector

2.1 Requirements

The primary requirement of the RICH detector for PID is the capability to detect a single photoelectron. The average charge of a single photoelectron multiplied by the RICH detector is 16 fC and obeys the Polya distribution[14]; that is, the charge distribution has a long tail. Physical simulations show that the detector output signal can be well covered when the dynamic range of the readout electronics is 3 times ($\sim$ 48 fC) of the mean pedestal. A noise $\leq$ 0.5 fC (RMS) @ 20 pF detector capacitance, a time resolution $\leq$ 1 ns (RMS) @ 48 fC, and the average event rate $\leq$ 1.6 kHz. should be achieved in the readout electronics. Additionally, the large number of detector channels requires a high-density front-end electronics system placed close to the back of the RICH PID detector, and the available space for readout electronics installation is thus restricted.

2.2 Prototype readout electronics

Multiple-channel front-end ASIC is the optimization solution to address the large number of MPGD detector channels. A 1024-channel prototype readout electronics was built to prove the design concept for reading out the RICH PID detector. The issues with the RICH PID detector readout system are not only the large number of readout channels but also the experimental environment as the detector itself is placed in a very compact space. The architecture of the proposed prototype readout electronics of the RICH PID detector is illustrated in Fig. 1 and consists of a low-noise front-end card (FEC), which is coupled to a multichannel analog-to-digital converter (ADC) adapter via cables and to a purely digital readout unit (RU) or directly to the RU via high-density cables or optical fibers depending on whether the output format of the front-end ASIC is a digital signal or an analog signal. The RU receives and packages the data from multiple FECs or ADC adapters and finally transfers them to the data acquisition (DAQ) system via a high-speed fiber link. The RICH PID electronics does not participate in the generation of the global trigger signal. The RICH PID readout electronics has to receive the global trigger and implement trigger matching in the RU. The RICH PID detector readout electronics also has to be synchronized with a global clock signal, and this clock is fanned out to the ASICs in the FECs or ADC adapters through the RUs.

2.3 Signal Processing Method

According to the typical characteristics of the output signal of the MPGD detector, the charge signal generated at the anode pad can be modeled as a short pulse current source with a total width of $\sim$ 100 ns, a fast-rising edge (typically with a duration of 1 ns), and a capacitance C_d for the detector capacitance modeling[15]. The analog signal processing of one channel mainly adopts the following method for the high-precision charge and time measurements. To prevent an electronic static discharge (ESD) or large signals from damaging the front-end amplifier, special ESD-protection circuits are designed for each channel in the input stage, and the analog signal is clamped below a protection voltage by an ESD protection diode. A charge-sensitive amplifier (CSA) is used to read out the signals from the anode pad of the MPGD detector, and the signal from the CSA is fed to a shaper. The CSA is characterized by a low noise and a high charge-measuring performance, and its output signal amplitude should not be affected by the parameter mismatch among the channels. The readout ASICs of the MPGD detector are investigated according to the readout requirements of the detector and the characteristics of its output signals. At present, the ASICs

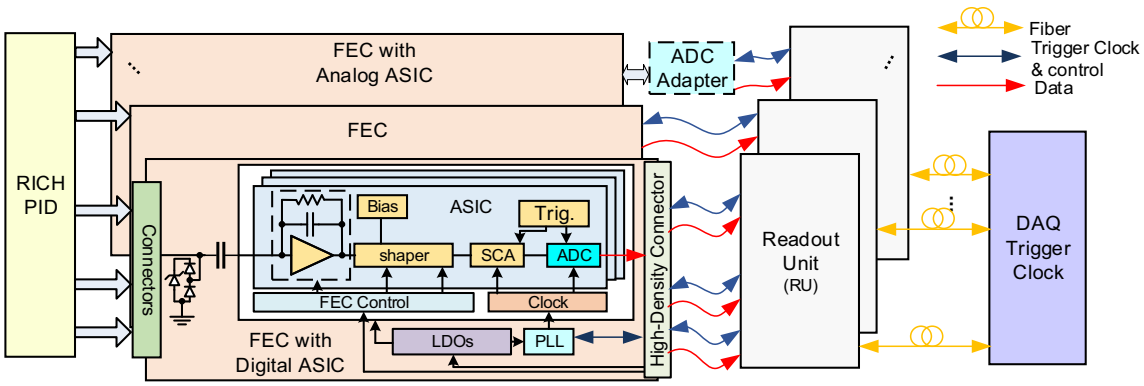


Fig. 1 (Color online) Structure of the proposed prototype readout electronics of the RICH PID detector

simultaneously realize high-precision charge and time measurements can be based on waveform digitization techniques. The signal processing flow based on this scheme is shown in Fig. 2. This technique can be used to obtain a complete detector waveform, which is beneficial in the evaluation of the detector performance. The incoming analog signal from the MPGD detector is first amplified by a CSA, then fed to a shaper, and finally transferred to an isolation buffer or a switching capacitor array (SCA); thus, an ADC is required[16]. The digitized signal is sent to a field-programmable gate array (FPGA), and the charge information can then be obtained through peak detection or area calculation of the digitized waveform[17, 18]. Additionally, the time information can be obtained using a leading-edge discrimination method. Considering the application investigated in this work, since the detector is still in the research and development stage, useful information is expected to be obtained through waveforms; thus, the use of the waveform digitization scheme meets the readout requirements of the current RICH PID detector.

By comparing different MPGD experiments, it was found that ASIC chips are widely used for the front-end electronics due to their large number of readout channels[19–22]. The choice of a suitable chip for the readout of the RICH PID detector among these ASICs requires an analysis of the key parameters of the readout electronics system. The time measurement attempts to optimize the determination of the time of at which the investigated event occurs. A key factor that determines the accuracy of the time and charge measurements is the signal-to-noise ratio (SNR) of the system. The SNR characteristics of the readout electronics are usually determined by considering the readout equivalent noise charge (ENC) as:

$$\mathrm{ENC} = \frac{Q}{\mathrm{SNR}}, \tag{1}$$

where Q is the charge collected at the CSA input. According to Eq. (1), ENC is defined as the electrons that must be collected at the input to obtain an output voltage that equals the noise. It can be demonstrated[23] that, if the preamplifier parallel noise is negligible, ENC is a linear function of the test load capacitance C_d connected to the CSA input according to:

$$\mathrm{ENC} = mC_d + n, \tag{2}$$

where m and n are constants. ENC is a very important parameter that affects the accuracy of charge and time measurements. In addition, in the time measurement, the measurement accuracy is also closely related to the rise time and sampling rate of the waveform. The leading edge of the pulse is used for the timing, and the instantaneous signal level is modulated by the noise. Due to these fluctuations, the time of the threshold crossing fluctuates; the timing variance or "jitter" can be written as[24]:

$$\sigma_{\mathrm{t}} = \frac{\mathrm{ENC} \cdot t_{\mathrm{r}}}{Q} \cdot \frac{1}{\sqrt{t_{\mathrm{r}} \cdot f_{\mathrm{s}}}}, \tag{3}$$

where t_{r} is the rise time of the signal, Q is the charge of the input signal, and f_{s} is the sampling rate. From Eq. (3), it becomes clear that a low ENC is not the only important factor to achieve a precise time measurement; indeed, also

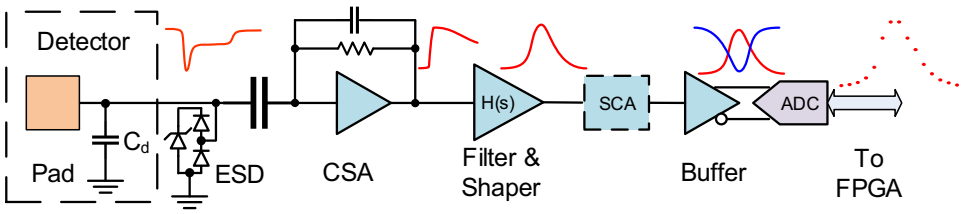


Fig. 2 (Color online) Signal processing flow

a high sampling frequency and a short signal rise time are necessary. To attain a 1 ns time resolution, the simulations show that with a fixed ENC and at least two sampling points on the leading edge, f_s and t_r have an operating region, as shown in Fig. 3a. The red line marks the boundary of the 1 ns time resolution. In the upper of the red line, the time resolution is greater than 1 ns, which does not meet the requirements of the RICH PID detector readout system. In the bottom of the red line, the time resolution is better than 1 ns, and the values of t_r and f_s in this region meet the requirements of the RICH PID detector readout system. In addition, the time resolution parameter depends on t_r, f_s, and ENC, as shown in Fig. 3b. Increasing ENC can reduce the time resolution, so it is also important to minimize the total capacitance C_d at the input.

2.4 Front-end ASIC selection

As mentioned above, there are several readout ASICs based on waveform digitization that can realize high-precision time and charge measurements at the same time. The AGET [19, 25] and APV25 [20] ASICs are close to meeting the readout requirements of the RICH PID detector, and their main features are listed in Table 1. However, these two ASICs also have several shortcomings that do not fully meet the reauirements of RICH detectors. For example, the dynamic range of AGET is too wide, while that of APV25 is slightly smaller. Therefore, our group designed an STCF ASIC to meet all the requirements of the RICH PID detector. The AGET (ASIC for GET) front-end circuit was developed to perform the amplification of the time projection chambers (TPCs) used in nuclear physics experiments [19]. The APV25 ASIC was originally built for the readout of the CMS silicon microstrip tracker [26] and has been successfully adopted for the readout of the COMPASS GEM, pixel MM, and tracking detectors [7, 27]. The design is driven by the detector characteristics and the time and resolution requirements imposed by the physics and trigger scheme of the STCF experiment. The STCF ASIC performs a direct digitization of all channels after the preamplifiers/shapers and the SCAs. It greatly improves the integration of the system and reduces the costs. The specifics of the APV25 and STCF ASIC as well as their readout electronics are described below. The strategy of this work is to use the existing AGET and APV25 to verify the design scheme of the prototype readout electronics, and tested for comparision with the results using the STCF ASIC designed by our group. We aim to build a flexible and efficient detector readout system whith a high density, and a low cost to

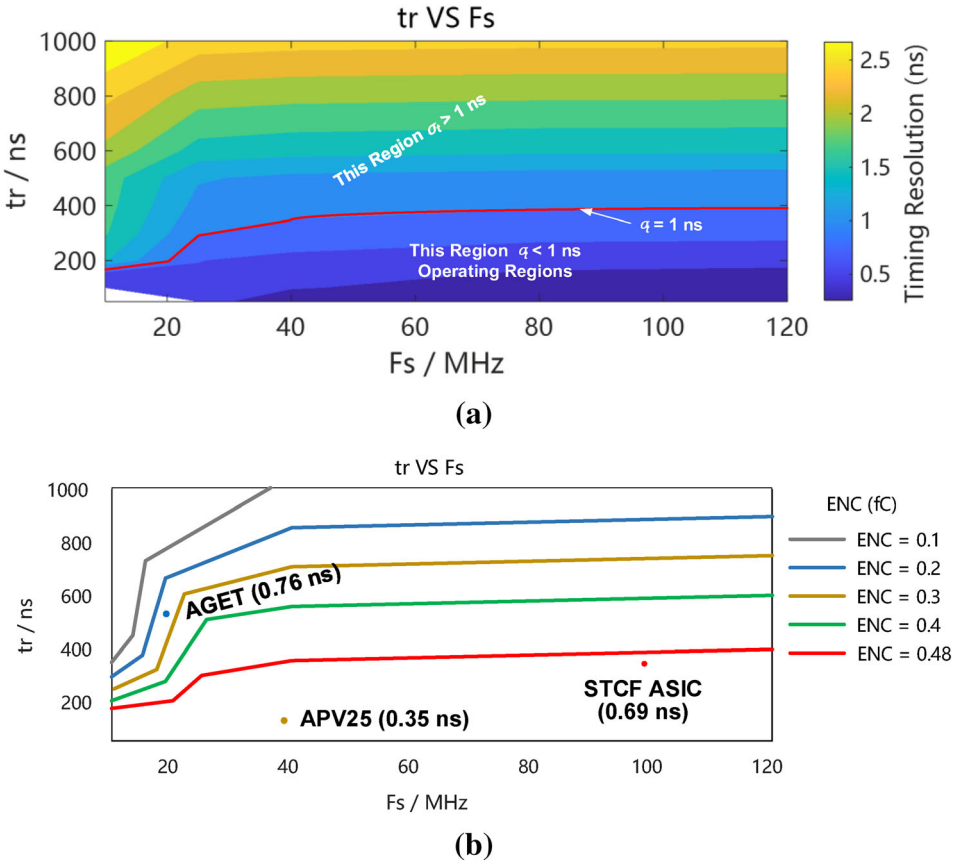


Fig. 3 (Color online) Resolution of the time measurement. **a** Time resolution parameter sweep in terms of f_s and t_r @ ENC = 0.48 fC. **b** Time resolution parameter sweep in terms of f_s, t_r, and different ENC values

Table 1 Comparison of the different ASICs for MPGD detectors

ASIC	Channels	Dynamic range	Noise (fC/pF)	Power consumption (mW/ch)	Sample rate (MHz)	SCA cells	Output
APV25	128	20 fC	0.039 + 0.0058 fC/pF	2.7	40	192	Analog
AGET	64	120 fC, 240 fC, 1 pC, or 10 pC	0.072 + 0.0016 fC/pF	10	1–100	512	Analog
STCF ASIC	8	48 fC, 96 fC, 240 fC	0.379 + 0.0054 fC/pF	20	1–100	256	Digital

achieve a comprehensive performance evaluation of the STCF ASIC and RICH PID detectors. This provides a guideline for the final electronics design using the STCF ASIC.

3 Circuit design of the prototype readout electronics

Based on the above considerations, we decided to use APV25, AGET, and STCF ASIC to test the prototype design. As the AGET ASIC system was already tested in our previous work [28], it will not be described in detail here. However, in this work, the AGET system was tested more extensively as an additional reference for the comparison of the two technical routes. Firstly, we will present the design of the electronics employing APV25.

3.1 Prototype readout electronics based on the APV25 ASIC

Each APV25 channel consists of a CSA, a unity-gain inverter (UGI), a 50 ns CR-RC-type shaping amplifier, and an analogue pipeline (AP), which completes the sampling of the analog signal. The incoming analog signal from the RICH PID detector anode pad is first amplified by the CSA and then shaped and changed in width by a shaper. The CR-RC shaper output amplitudes are sampled at a frequency of 40 MHz and stored by the AP. The AP buffers the data with a programmable latency of up to 160 clock cycles, thus allowing for a trigger decision to be made within $\sim$ 4 μs. When an event is marked as completed with the corresponding readout points (in the multipeak mode, the maximum number of readout points is 30), the signals from the analog buffers are read out through a 128:1 multiplexer at 40 MHz into a single differential output. The multiplexed analog data stream from each APV25 FEC, which was designed by INFN for the readout electronics of the JLab Hall A GEM Tracker detector [29], is then transferred to a differential analog buffer on the ADC adapter card via an HDMI cable. The structure of the readout chain of the RICH PID detector is shown in Fig. 4. A small-scale prototype readout electronics was designed to test the readout electronics and the performance of the RICH PID detector. This prototype readout electronics contains a RICH PID detector readout plane with 5×5 mm^2 anode pads, an FEC with readout ASICs, an ADC adapter, and an RU with high-density or high-speed readout interfaces. Furthermore, the RU also receives the trigger and clock signals from the trigger and clock system and synchronously fans them out to each FEC. The prototype readout electronics adopts the implementation architecture of the mother–daughter card and transfers data through an optical fiber, which has a high flexibility and scalability and is useful for detector development and laboratory tests. The scaling up of the system to larger sizes is achieved by deploying multiple FECs, ADC adapters, and RUs.

The ADC adapter card, which is composed of differential analog buffers, a clock synchronous fan-out, a 12 bit ADC, and LDOs, is mainly used to digitize the analog signal from the FECs, as shown in Fig. 5a. The analog signal from each FEC is independently received with a very-low-noise, low-distortion, high-speed differential amplifier circuit based on an Analog Devices ADA4930, including an impedance matching network to restore some of the high-frequency cable losses and improve the settling time. The simulation results show that its 3 dB bandwidth is 300 MHz, and when the input is a step signal, the output reaches a stable state within 4 ns. The amplitude–frequency response and transient simulation results are shown in Fig. 5b, c, d, and e. The analog signal is then passed to octal 12 bit ADC channels based on an Analog Devices AD9637, which has an outstanding dynamic performance, a low power consumption, a programmable reference voltage, a conversion rate of up to 80 Msps, and a common voltage output to complete the digitization of the analog signal. The ADC sampling clock and the APV25 sampling/readout clock are both derived from the clock fan-out chip because the APV25 remains active and performs sampling during the readout process; it uses a common clock for both functionalities. A sampling frequency of 40 MHz is used.

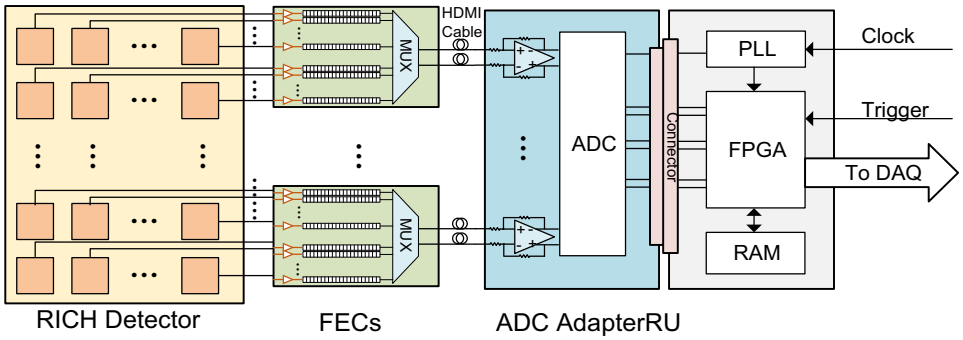
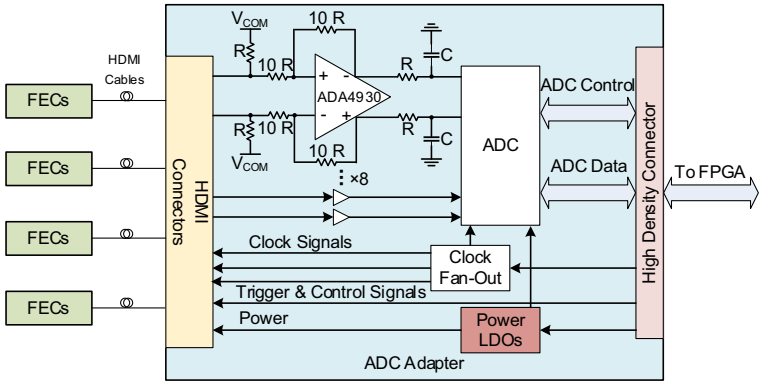
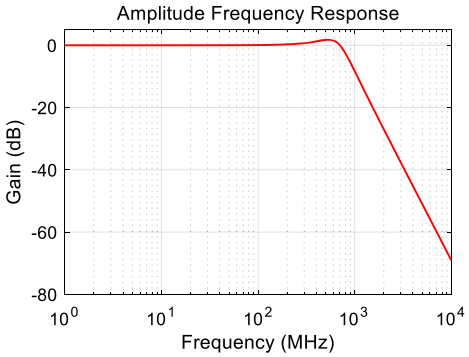


Fig. 4 (Color online) Structure of the readout chain for the RICH PID detector



(a)



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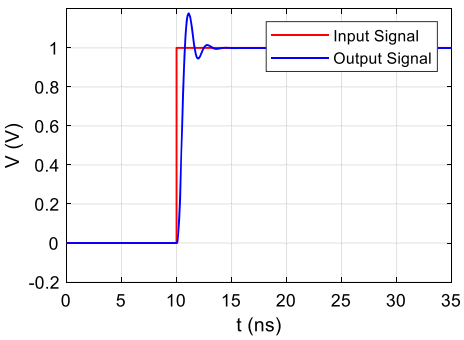
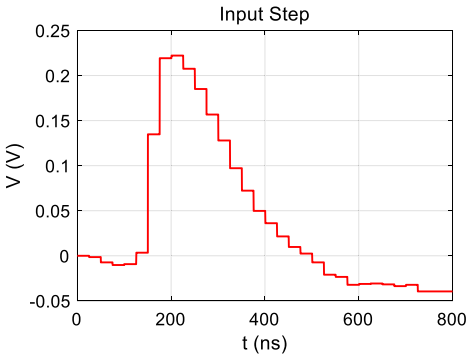
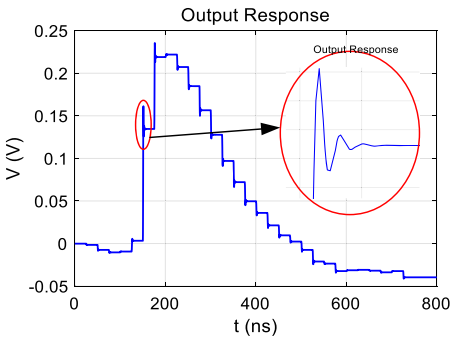


(c)



(d)



(e)

Fig. 5 (Color online) Block diagram of the ADC adapter card and simulation results **a** Block diagram of the ADC adapter card; **b** Amplitude–frequency response; **c** Step response; **d** ADA4930 input step signal coming from the APV25; **e** ADA4930 output response

The clock fan-out chip based on an Analog Devices ADCLK854 is used to ensure that the sampling clock of the ADC is aligned with the leading edge of the readout clock of the APV25. The final digitized signal is transmitted to the FPGA through a high-density connector. In addition, the slow control interface and power supply of the FECs are connected to the RU through high-density connectors and HDMI cables. The slow control interface complies with the I^2C standard. The APV25 ASIC has 17 read/write registers and 1 read-only error flag register. Except for the power on reset circuit, all operations are controlled by these registers. We connected the I^2C lines to all APV25 chips on each FEC and connected them to the cable without buffering. The FEC interconnection board contains a pull-up resistor connected to a VDD. The I^2C interface protocol is adopted and processed in the FPGA firmware of the RU.

3.2 Prototype STCF ASIC and FEC circuit design

Each channel of the STCF ASIC integrates mainly a CSA, a CR–RC^2 shaper, an analog memory based on the SCA technology, and a 12-bit channel ADC. The CSA has a variable gain, adjustable for each channel, which can fully satisfy the requirement of the RICH PID detector. The shaping time of the shaper is adjustable in the range from 180 ns to 1 μs. The filtered signal is sent to the analog memory and quantized to a digital signal through the channel ADC, and the digital signal is finally output to an FPGA through the serial interface. The charge information can then be obtained through peak detection or area calculation of the digitized waveform. In addition, the time information can be obtained using a leading-edge discrimination method. To evaluate the performance of the STCF ASIC, the prototype readout electronics was designed and tested. The RICH PID detector signals are AC-coupled to the STCF ASIC via a Hirose surface mount connector and protected against discharge using a commercial fast ESD diode (NUP4114) with a low stray capacitance (typically < 0.6 pF; I/O to GND). The SCA sampling, ADC, and readout clocks of the STCF ASIC chip are provided by a multioutput clock generator chip based on an Analog Devices AD9522 with a subpicosecond jitter performance. The final digitized signal is transmitted to the FPGA through a high-density connector. In addition, the slow control interface and power supply of the FECs are connected to the RU through high-density connectors. The slow control interface of the STCF ASIC and AD9522 originates from the FPGA on the RU.

3.3 RU design

The RU carries out all operations required for the control of the FEC and data acquisition. The RU is based on a Kintex-7 Xilinx FPGA (XC7k325T), integrating eight SFP + interfaces for high-speed data communication, two 2 Gbit × 16 DDR3 memory chips, and several general-purpose interfaces. The RU can be used to transmit the global clock, trigger, and global reset, control signals from the DAQ or trigger and control systems, such as SMA interfaces and LEMO standard interfaces, and control signals to HDMI interfaces. In order to meet the requirements of flexibility and scalability, redundancy is fully considered when designing the RU, which can cover potential FECs based on different multichannel ASICs. On the front-end side, five high-density connectors from Samtec are used. Both the differential IO and single IO from the FPGA are routed to these high-density connectors; with sufficient design redundancy, wires of the same length and the IO level could be adjusted according to the different FECs. In addition, power supplies from the DC–DC power module are also connected to the high-density connectors. By reconfiguring the interface, the specific adapter and corresponding FEC work normally under the control of the RU, which uses an SFP + transceiver module to connect to the DAQ. In addition, multiple RUs can be assembled in a topology through SFP + ports. This method makes this prototype readout electronics suitable for experiments with a large number of detector channels.

Event data directly from the FECs or ADC adapter cards are collected, processed, and packaged in the FPGA, as shown in Fig. 6. Many ADC adapters or direct digital output FECs use a serialized interface to provide digital data over differential or single-end IOs per ADC or digital output ASIC in the component package to the FPGA. The analog signal is converted into a digital serial data stream with a 12-bit ADC or a higher resolution, which is provided together with a high-speed data clock (Data_CLK) and a sync or frame clock (Frame_CLK). Due to the printed circuit board (PCB) routing and clock buffer delay inside the FPGA, the Data_CLK must be repositioned for capturing data and frame signals. The Data_CLK, which is also sent as data to the D input of the ISERDESE2 in the same I/O tile as the IDELAYE2, is routed from the ADC through an IDELAYE2 used in the variable mode to the input of a BUFIO in order to align the Data_CLK and BUFR to reconstruct the Frame_CLK. It is then connected at a data-capture level to the CLK and CLKDIV inputs of all ISERDESE2. The Data_CLK essentially registers itself in the ISERDESE2 using a delayed version of itself as a clock. Since the serialized output data stream is deserialized by the ISERDESE2, the parallel data is transferred to a channel FIFO and then to a peak detection (PD) module and a digital constant fraction discriminator (DCFD) module to calculate the charge and time information. The corresponding data is then selected by the multiplexer to be

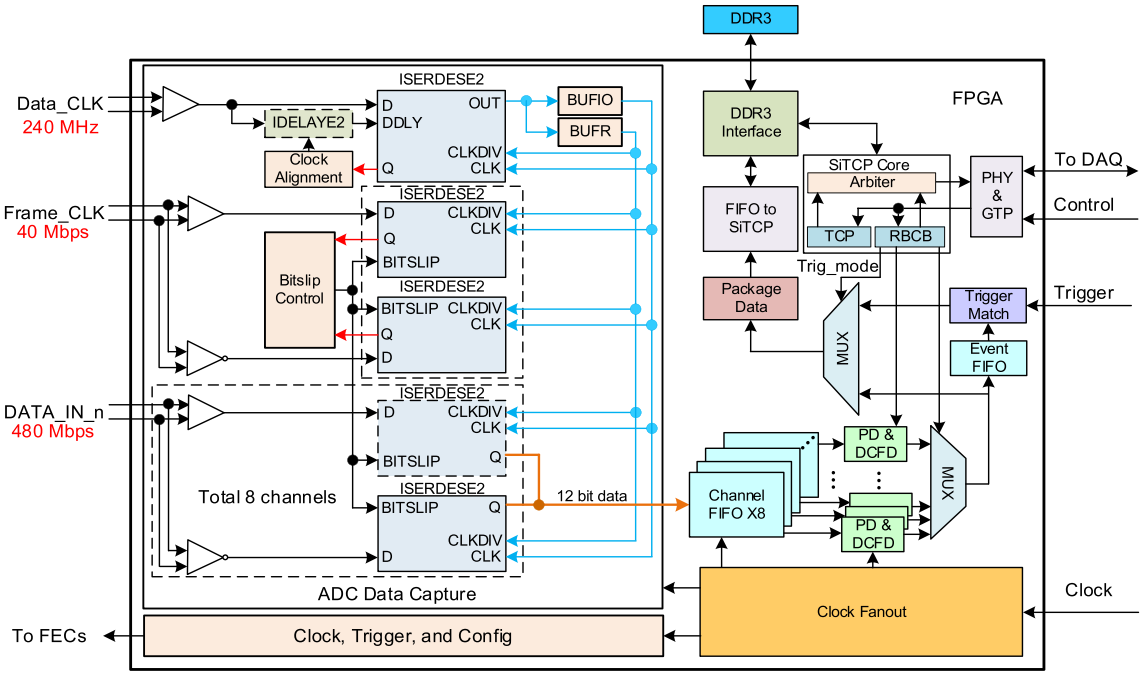


Fig. 6 (Color online) Block diagram of the data collection and transmission logic

transmitted to the event FIFO. This is because the RICH PID electronics does not participate in the generation of the global trigger signal. Therefore, in this prototype readout electronics, there are two optional methods for valid data readout. One is triggerless, which means no trigger signals are required, and the other is the traditional trigger mode, which requires a global trigger signal and implements trigger matching in the RU. The data from the FECs are first stored in the event FIFO on the RU; when the RU receives a trigger signal, it calculates a valid time range in which valid data are contained, according to the trigger window width and trigger latency. The valid data are then transferred to the DAQ. To reduce the logic complexity and guarantee a good stability, the SiTCP core [30] is used for data packaging. The command and status information is transmitted through the user datagram protocol (UDP) interface of the SiTCP. In order to deal with transient burst data, an external 2 Gbit $\times$ 16 DDR3 memory is employed as an additional data buffer. The RU contains most of the high-complexity components of the prototype readout electronics for the RICH PID detector.

4 Performance of the readout system

The prototype readout electronics of the RICH PID detector with two sets of FECs based on the APV25 and STCF ASIC and one ADC adapter was implemented and assembled. After the design and fabrication, we conducted a series of tests to evaluate the performance of the prototyppe readout electronics. The output of the RICH PID detector consists of a charge pulse signal, and the voltage pulse output obtained from the external step attenuator has to be converted into a charge pulse and sent to the FEC ASIC. As shown in Fig. 7, according to the RICH PID detector output waveform recorded by a high-speed oscilloscope, an arbitrary function generator (AFG31252 from Tektronix Inc.) is used to generate the input signal for the FEC. The signal amplitude is tuned by an external step attenuator (RSC-04 from Rohde & Schwarz Inc.), and the time and charge measurement resolution can then be tested with different input amplitudes. The output data from the FEC are transferred to a PC through Ethernet.

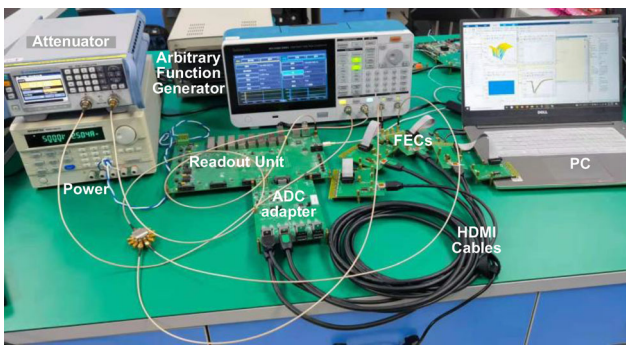


Fig. 7 (Color online) System under test

4.1 APV25 FEC test

To evaluate the prototype readout electronics performance, charge should be injected into the CSA input. This is typically done by applying a voltage pulse ΔV through a small test capacitor C_{test} at the input of the CSA [31]. The test voltage pulse generated by the AFG31252 is injected at the falling edge of one channel through a calibration capacitor, and a slow rising edge prevents the positive charge injection. The injected charge ΔQ is given by:

$$\Delta Q = \Delta V \frac{C_{\text{test}}}{1 + \frac{C_{\text{test}}}{(A_0+1)C_{\text{f}}}} \approx \Delta V C_{\text{test}}, \quad (4)$$

where A_0 is the voltage gain of the amplifier, and C_{f} is the feedback capacitor of the CSA. Since in practice $C_{\text{test}} << (A_0 + 1)\ C_{\text{f}}$, the injected charge ΔQ is totally fed into the CSA.

For the APV25 ASIC, the peak time and charge can be obtained by applying a fitting function to the sampled shaper output values. When the APV25 is working in peak mode, for each trigger, the system reads three consecutive amplitudes in time, so that the information about the signal amplitude and its timing can be extracted. Figure 8a shows a typical event with 30 samples, where the amplitude represents the charge, and the peak time is determined by the shaping time. By adjusting the amplitude of the input pulse, the input/output curve over the full chip dynamic range for the 20 fC range is depicted in Fig. 8b. The integral nonlinearity (INL), calculated as the normalized residues of a linear fit to the measured data, is better than 2%, as shown in Fig. 8c. Using the self-trigger mode, the baseline of a particular channel is sampled, and the ENC of the 30 sample cells can be plotted, as shown in Fig. 8d. The ENC is $\sim$ 0.2 fC (RMS) @ 20 pF. Furthermore, the ENC was measured as a function of different input capacitance values, as shown in Fig. 8e for the peak mode for a particular channel. The ENC increases according to 0.063 + 0.0066 fC/pF. In addition, the time resolution was measured as a function of different input capacitance values, and the corresponding test results are shown in Fig. 8f. From this figure, it can be seen that the time resolution is better than 1 ns (RMS) at an input charge exceeding $\sim$ 12 fC.

4.2 STCF ASIC FEC test

Using a test method similar to the APV25 FEC, the performance of the STCF ASIC FEC was also tested. Figure 9(a) shows a typical event with 256 sample cells, where the amplitude represents the charge, and the peak time is determined by the shaping time. By adjusting the amplitude of the input pulse, the input/output curve over the full chip dynamic range for the 48 fC range is depicted in Fig. 9b. The INL, calculated as the normalized residues of a linear fit to the measured data, is better than 4%, as shown in Fig. 9c. The ENC was measured as a function of different input capacitances. The baseline of a particular channel was sampled, and the ENC level of the 256 sample cells is plotted in Fig. 9d. The ENC is better than $\sim$ 0.48 fC (RMS) @ 20 pF, which is beyond the application requirement. In addition, the ENC was measured as a function of different input capacitances, as shown in Fig. 9e for a particular channel. The ENC increases according to 0.38 + 0.0055 fC/pF. Furthermore, the time resolution was measured as a function of different input capacitances, and the corresponding test results are shown in Fig. 9f. From this figure, it can be seen that the time resolution is better than 1 ns (RMS) at an input charge of $\sim$ 37 fC.

4.3 AGET readout system test

Based on the previous investigations, the AGET electronics system was tested in detail, and the results are shown in Fig. 10. The ENC is $\sim$ 0.27 fC (RMS) @ 20 pF, which is beyond the application requirement. Furthermore, the ENC was measured as a function of different input capacitances, as shown in Fig. 10a. The ENC increases according to 0.088 + 0.0095 fC/pF. In addition, the time resolution was measured as a function of different input capacitances, as shown in Fig. 10b. From this figure, it can be seen that the time resolution is better than 1 ns (RMS) at an input charge exceeding $\sim$ 45 fC.

Based on the above test results, the ENC and time resolutions obtained from the simulations and tests of the APV25, AGET, and STCF ASIC chips are compared in detail, as shown in Table 2. Moreover, the prototype readout electronics concord well with our analyses. Thus, our results provide an important guideline for future engineering electronics work.

5 Conclusion

The prototype readout electronics of the RICH PID detector for the STCF was designed and tested. Analyses were conducted, and the key parameters of the circuits were determined to guide the selection of the optional front-end ASIC. The designed prototype readout electronics modules were mainly composed of an FEC, an ADC adapter, and an RU, which could realize the readout of 1024 channels. Finally, the performance of the RICH PID readout system was tested; the ENC and time resolution of the three ASICs were compared in detail; and the results of the prototype readout electronics were found to be in good agreement with our analyses. Therefore, this study provides

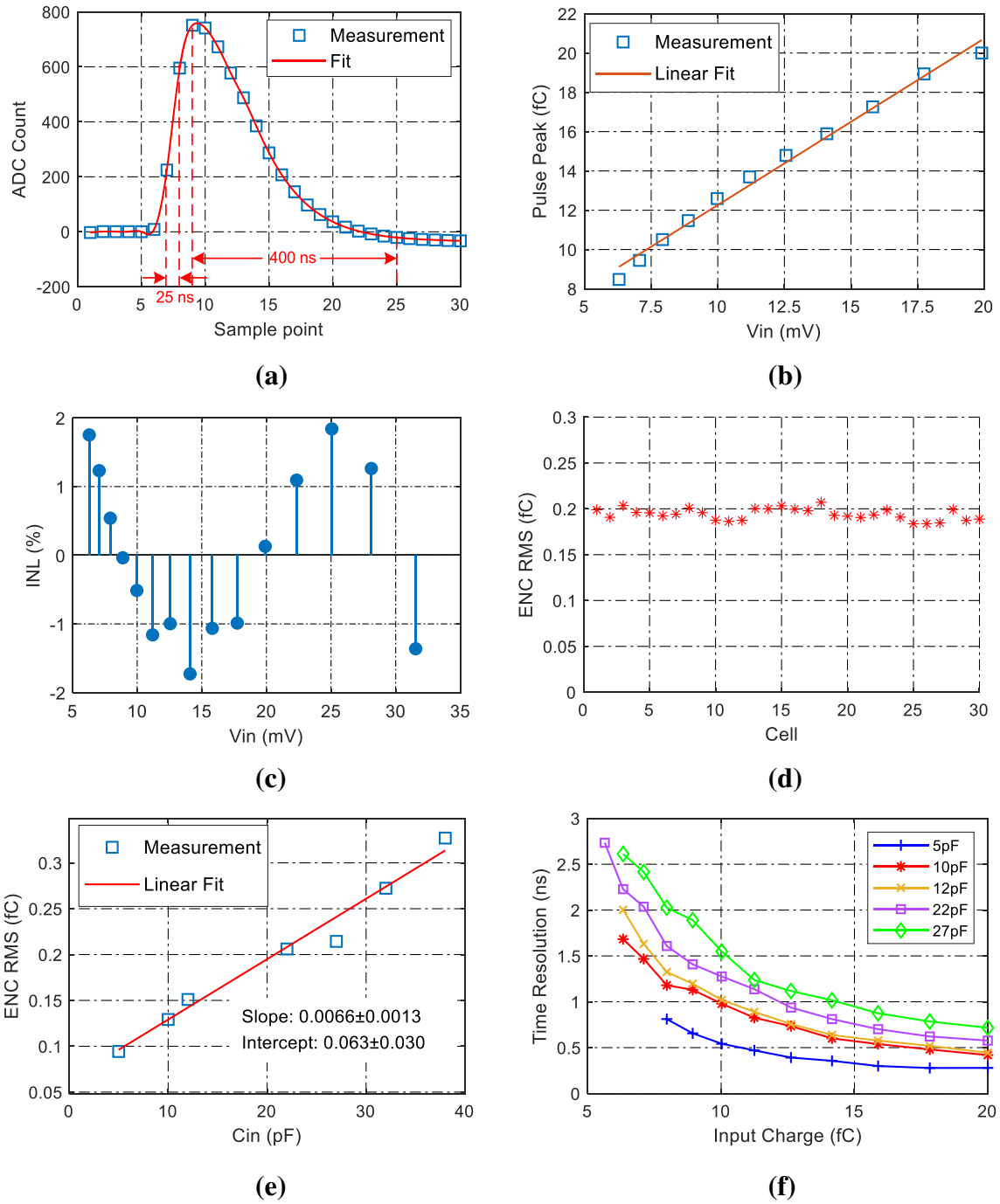


Fig. 8 (Color online) Test results for the APV25 FEC **a** Response curve of the input signals; **b** Typical input/output curve; **c** The INL is better than 2%; **d** ENC level for different sample cells; **e** ENC level for different input capacitances; **f** Time resolution as a function of the input-signal amplitude for different input capacitances

an important technique preparation for future engineering electronics work. The prototype readout electronics system was also designed with a flexible structure, which could adapt different FECs with one single RU. Furthermore, it was proven that the electronics structure has a scalable architecture, which is suitable for large-scale systems.

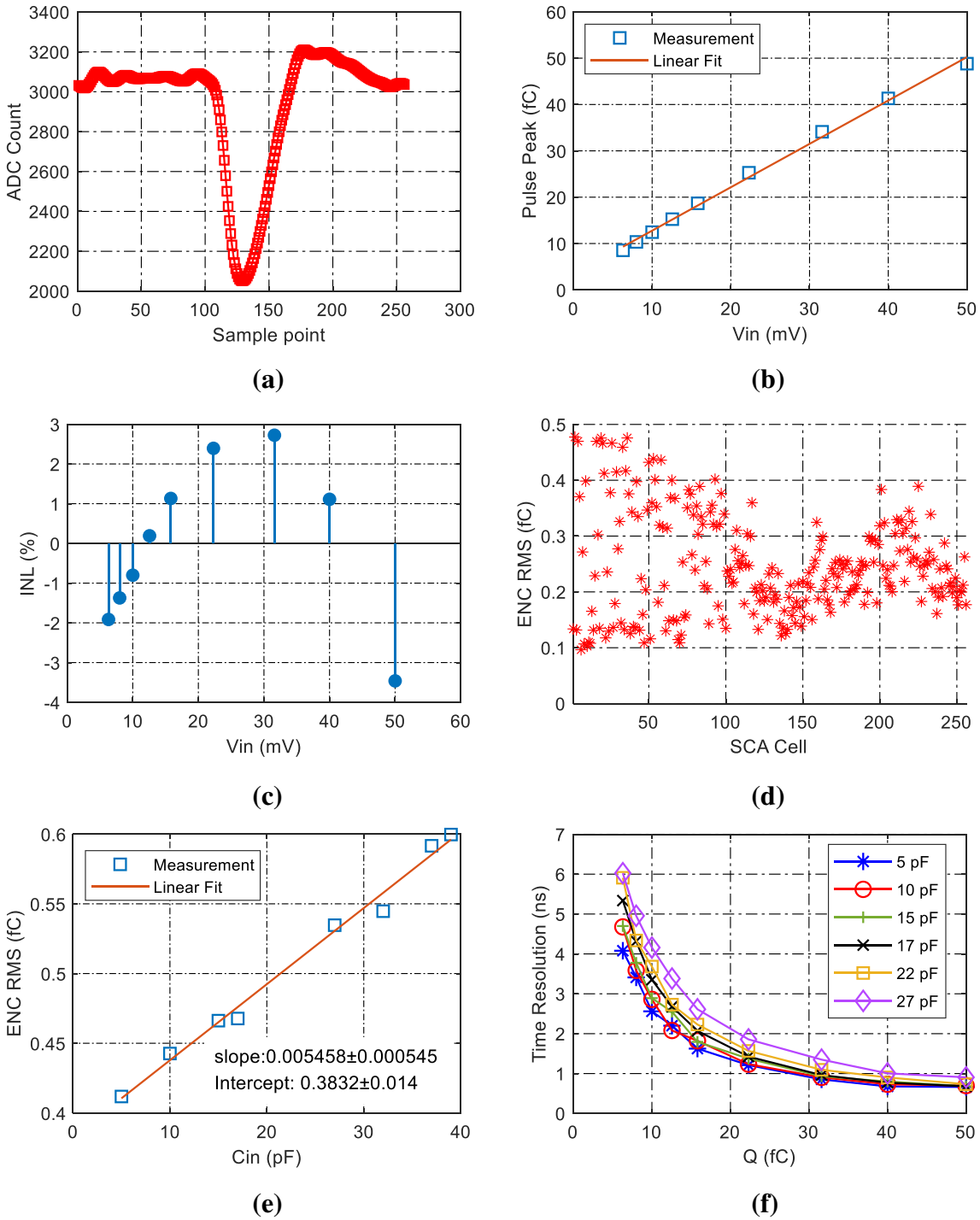


Fig. 9 (Color online) Test results for the STCF ASIC FEC **a** Response of the input signals; **b** Typical input/output curve; **c** The INL is better than 4%; **d** ENC level for different sample cells; **e** ENC level for different input capacitances; **f** Time resolution as a function of the input-signal amplitude for different input capacitances

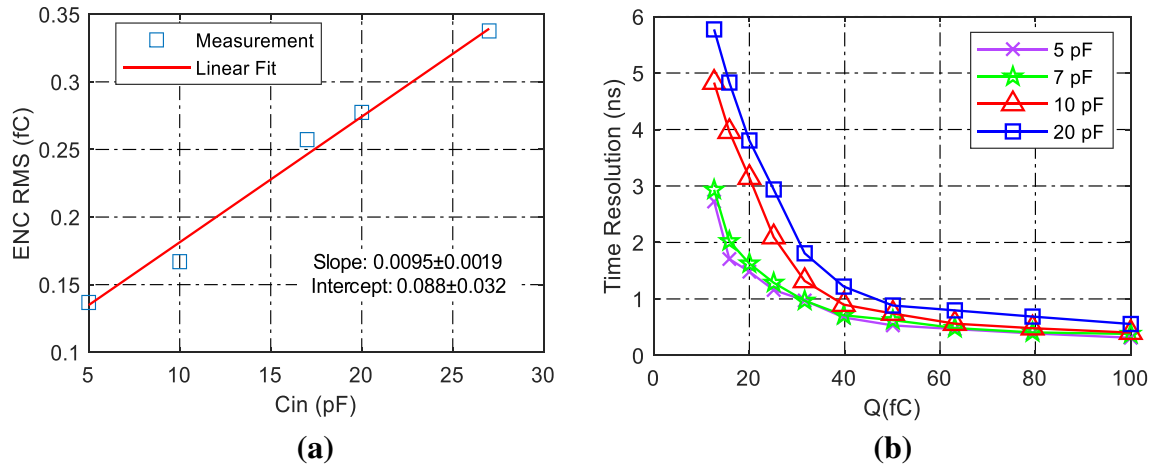


Fig. 10 (Color online) Test results for the AGET FEC **a** ENC level for different input capacitances; **b** Time resolution as a function of the input-signal amplitude for different input capacitances

Table 2 Comparison results of the different ASICs

Parameters		Readout electronics based on APV25	Readout electronics based on AGET	Readout electronics based on STCF ASIC
Time resolution	Simulation (ns)	0.35	0.76	0.69
	Test (ns)	0.56	0.85	0.73
ENC RMS (fC)@ 20 pF		0.2	0.27	0.48
INL (%)		< 2	< 3	<4

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