NUCL SCI TECH (2020) 31:100
https://doi.org/10.1007/s41365-020-00806-6

Design and preliminary test of the LLRF in C band high-gradient test facility for SXFEL

Cheng-Cheng Xiao[1] · Jun-Qiang Zhang[1] · Jian-Hao Tan[1] · Wen-Cheng Fang[1]

Received: 14 July 2020 / Revised: 8 September 2020 / Accepted: 9 September 2020 / Published online: 10 October 2020

Abstract This paper describes the design and preliminary test of the low-level radio frequency (LLRF) part of the C band high-gradient test facility for the Shanghai Soft X-ray Free-Electron Laser (SXFEL)-Linear Accelerator (LINAC). Before installation, the accelerating structures should be tested and conditioned. During the conditioning process, breakdown detection is needed to protect the accelerating structures and klystron from damage. The PCI extensions for instrumentation-based LLRF system and auto-conditioning algorithm are designed and applied in the LLRF part of the C band high-gradient test facility. Three C band accelerating structures and 1 pulse compressor have completed conditioning and were installed in the SXFEL-LINAC.

Keywords Accelerating structure · High gradient · C band · Breakdown · LLRF · Conditioning

1 Introduction

A revolutionary advance in light sources has been realized with the recent advent of the free-electron laser (FEL) [1]. The FEL is regarded as a fourth-generation light source [2] and has a series of advantages that cannot be replicated by existing laser sources. These advantages include a continuously adjustable frequency, a wide spectrum range, high and adjustable peak and average powers, excellent coherence, strong polarization, and controllable temporal structure [3].

The Shanghai Soft X-ray Free-Electron Laser (SXFEL) facility is the first coherent X-ray light source in China [4]. It is being developed in two steps, namely the SXFEL test facility (SXFEL-TF) and the SXFEL user facility (SXFEL-UF) [5]. The SXFEL-TF is a critical development step toward the construction of a soft X-ray FEL user facility in China and is currently undergoing commissioning at the Shanghai Synchrotron Radiation Facility (SSRF) campus. The test facility will generate 8.8 nm FEL radiation using a 840 meV electron LINAC with a two-stage cascaded HGHG-HGHG or EEHG-HGHG (high-gain harmonic generation, echo-enabled harmonic generation) scheme [6, 7].

The LINAC in SXFEL-TF is designed to increase the beam energy from 150 to 840 meV. C band accelerating structures are applied here to guarantee a high gradient. The entire LINAC is built with 12 C band accelerating structures working at 40 MV/m. The RF field stabilization is controlled by a low-level radio frequency (LLRF) system based on accurate RF field measurements at the frequency of 5.712 GHz [8]. The LLRF parameters therefore need to be optimized to maximize the beam stability [9]. There is a large amount of residual absorbed gas and micro-protrusions left in the cavities in the C band accelerating structures after their manufacture which act as emission sources for electrons and ions. Increasing the electric field in the accelerating cavity requires the breakdown rate (BDR) to be decreased [10, 11]. Before installation in the LINAC, the C band high-gradient accelerating structures must go through a process called conditioning to decrease the BDR

This work was supported by the National Key R&D Program of China (No. 2018YFF0109203).

✉ Wen-Cheng Fang
fangwencheng@zjlab.org.cn

[1] Shanghai Advanced Research Institute, Chinese Academy of Sciences, Shanghai 201210, China

to a level that is acceptable within the theoretical design of the SXFEL-TF (10^{-4} breakdowns per pulse).

The high-gradient test for high-gradient accelerating structures is a relatively long process that can last for weeks. Automating the high-power test is therefore greatly significant for experimental accuracy and operation simplicity. Additionally, the high RF feed power during the process of conditioning increases the likelihood of vacuum pressure increases and frequent breakdowns (BDs), which can easily cause irreversible damage to the accelerating structures and klystron and necessitate the incorporation of interlock protection. In the subsequent diagnosis of the accelerating structure, it is necessary to store the waveform when a BD occurs to determine the location of the BD. The high-gradient test facility should therefore be able to control all the parameters in the conditioning process, detect the operation of the machine in real-time, record and analyze various information, and decide what to do during both the planning and the actual execution of the conditioning process.

The LLRF system design and implementation will be described in detail in the following sections together with the test results of the entire conditioning process.

2 System design

Unlike online LLRF systems in use in LINACs, the LLRF system in the high-gradient test facility is required to possess the advantages of convenient adjustment, online software structure, and support for hardware driver changes, which would save time for the entire conditioning process. Compared with other architectures like MTCA (Micro Telecom Computing Architecture) and VME (VersaModule Eurocard), the PXI architecture from National Instruments has more software flexibility that would allow us to customize and reconfigure the systems to meet evolving test requirements. We therefore chose the PXI architecture to build the LLRF part of the high-gradient test facility.

The layout of the whole high-gradient test facility is shown in Fig. 1. The main LLRF system contains a PXI crate, a triggering and interlock control box, a radio frequency (RF)-local oscillator (LO) box, and a RF front-end box. Digitizers for data acquisition and signal generation and a field-programmable grid array (FPGA) extender card for distributing the triggering signals and receiving interlock signals are installed in the PXI crate and connected with the FPGA module. These devices communicate through the backplane bus. The PXI crate is responsible for most of the controls, triggers, and interlocks in the system. The RF frond-end box is responsible for down-converting the pickup RF signals to intermediate frequency (IF) signals. The RF-LO box provides a clock signal to the digitizers for data acquisition and a LO signal to the RF front-end box. The triggering and interlock box transfers all the triggers and interlocks from the NI 6583 to the BNC interface.

The pulse compressor requires a phase-modulated input pulse to produce a compressed and flat output pulse. We therefore used a PXIe-5673E to generate a modulated pulse signal with a phase shift within 180 degrees. The NI 5673E is a vector signal generator with a 50 MHz–6.6 GHz RF output frequency range and consists of three separate synchronized devices: a 145 MHz bandwidth, 2-channel, 16-bit PXI PXIE-5450 *I*/*Q* signal generator, a PXIE-5611 *I*/*Q* vector modulator, and a PXIE-5652 master oscillator. These three devices work together to produce a modulated RF pulse. The 5712 MHz RF signal generated by the NI PXIE-5652 master oscillator is divided into two channels, one of which is used as a continuous reference signal to serve as the signal reference of the whole system. The other channel enters the NI PXIE-5611 *I*/*Q* vector modulator and is divided into two mutually orthogonal components, which are, respectively, mixed with the baseband I and Q signals from the NI PXIE-5450 to generate *I*/*Q* radio frequency modulation pulses. These pulses in turn go through in-phase synthesis to generate the radio frequency modulation pulse output with a macro-pulse envelope for driving the solid-state amplifier (SSA). The SSA then drives the 50 MW Toshiba klystron. The RF power is delivered to the pulse compressor and finally to the C band accelerating structures.

The main RF frequencies are shown in Table 1. During the process of conditioning, the transmission power of the klystron, the transmission power of the pulse compressor, the reflection power from the power compressor, and the transmission power of the accelerating structures are down-converted to IF signals and sampled at quadruple frequency by a NI 5761 with a 250 MS/s, 14-bit ADC. The signals would then would be processed by the FPGA to determine whether a BD is occurring. A BD is regarded as occurring whether the reflection power delivered back to the klystron is more than 0.23% of the transmission power (VSWR = 1.1). The RF signal source and the triggers for the modulator and SSA will then be stopped for ten seconds. The DC current from the Faraday cup can also help to diagnose the dark current. A so-called dark current spectrometer can be used to investigate the geometric source of the emitted electrons during a BD in real time [12].

3 Breakdown processing

It has been observed in experiments and reported that the BDR can be approximated by the relation

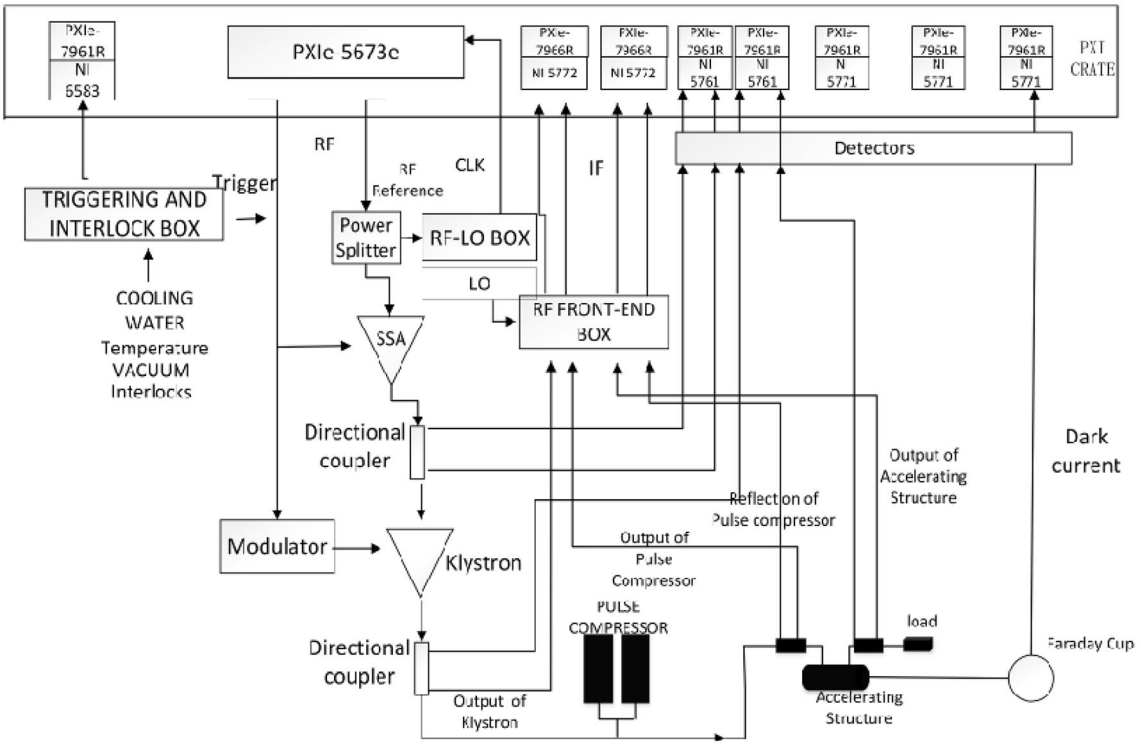


Fig. 1 Overview of the high-gradient test facility

Table 1 The main RF frequencies

RF signal	Frequency (MHz)
Master oscillator	5712
Local oscillator	5686.5
Sampling clock	102
Intermediate	25.5

$$\frac{E_0^{30} \times \tau^5}{\mathrm{BDR}} = \text{const.} \quad (1)$$

In this equation, E_0 indicates the accelerating gradient and τ the RF pulse length. The best fits for most fully conditioned structures have an exponent of around 30, but the exponent tends to be smaller in the early stages of the conditioning progress [13].

In order to design a smooth conditioning process with low BDR, the operating conditions (gradient, pulse length, and BDR) should be considered. This can be achieved by increasing the gradient and pulse length separately [14, 15].

The BD information of the accelerating structure comprises the reflected signal, pickup signal, and the DC current in the abnormality-diagnosis Faraday cup signal. The BD identification unit identifies the detection signal and determines whether a BD is generated in the accelerating structure during each macro-pulse. Based on the number of BD counts in the macro-pulses within a specific period and the microwave system vacuum level, the control system implemented in the NI PXI architecture based on LABVIEW FPGA technology will automatically adjust the pulse output amplitude of the klystron modulator beam voltage to increase the microwave injection power. The real-time acquisition and storage of the BD signal waveforms are of great practical significance for studying the physical mechanism of BDs and determining the BD position during the BD event in the accelerating structure. The BD RF pulse waveform is a spike micro-pulse whose amplitude changes sharply with time and therefore has a very wide spectral structure and large phase change. To obtain a high time resolution, the sampling frequency for obtaining the information of the BD waveform should be sufficiently high. In order to achieve a wide baseband signal spectrum, the IF should also be sufficiently high. In order to use the existing mature digital *I*/*Q* algorithm, the sampling frequency and the sampled signal frequency should follow the *I*/*Q* sampling. The bandwidth of the RF signals used for BD detection does not need to be as high as those of the device under test. Compared to the faster ADC NI 5772 (1.6 GS/s), the NI 5761 costs less and has more channels per card. The signals for BD detection are thus digitized using the 250 MS/s NI 5761 with 14-bit ADCs. The faster ADC NI 5772 will be installed in a future

facility upgrade in the PXI crate, which still has remaining slots.

The schematic of the BD processing is shown in Fig. 2. The NI 5761 is used in *I*/*Q* oversampling mode. The IF frequency is 25.5 MHz, and the clock sampling is 4 times the IF frequency, i.e., 102 MHz. In this mode, adjacent sampling data would be quadruple-sampled at the IF frequency.

After sampling by the ADC, the signal goes through the digital down converter (DDC), which generates the base-band *I*/*Q* signal. After IQ down-conversion, the data rate is reduced to half. The signals then pass through the finite impulse response (FIR) filter and are separated into two parts. One part is processed by the coordinate rotation digital computer (CORDIC) algorithm to obtain the phase and amplitude, which are useful for real-time waveform monitoring and for judging whether a BD has occurred. If a BD has occurred, the output of the NI 5673E vector signal generator will be stopped and the triggers for the SSA and klystron held. The other part of the signal from the FIR will be used to save the waveform in RAM at the system repetition rate, and if a BD occurs, the waveform data will be recorded onto the hard disk.

When a BD occurs, the reflection power transmitted back to the klystron will increase to 70–90% of the accelerating structure input power [16]. Figure 3a shows the theoretical principle behind locating the BD. When a BD happens, the BD signal will spread to the input and output of the accelerating structure simultaneously. The effects of the incident, transmitted, and reflected power on a pulse during a BD are shown in Fig. 3b. The transmitted power will be cut off, resulting in a drop in the transmitted power curve. The power curve reflected from the BD will rise sometime later [17].

Using Eq. (2), the group delay from the input of the structure to the breakdown site t_d can be calculated. t_{Rr} is the arrival time of the reflected rising edge, t_{Tf} the arrival time of the transmitted falling edge, and t_{fill} the filling time of the accelerating structure.

$$t_d = (t_{fill} + t_{Rr} - t_{Tf})/2 \quad (2)$$

Equation (3) can then be used to obtain the cell number n_{cell}. l_{cell} is the length of a single cell, and v_g is the group velocity.

$$n_{cell} = v_g t_d / l_{cell} \quad (3)$$

To further diagnose the health of the accelerating structures and analyze the BD, we need to know the location in the cavity where the BD happens. The current LLRF system records the 3 waveforms before the BD, the waveform when the BD occurs, and 1 waveform after the BD to locate the BD. In the future, we will add in an auto-location algorithm to find out which cavity the BD occurred in and a phase-detection algorithm to obtain the BD location in the cavity accurately.

4 RF distribution and timing

In the RF distribution and timing system design, it is necessary to consider the power matching between the units and evaluate the key parameters in the key frequency conversion units that impact the additional phase jitter. These parameters include the additional phase jitter in the process of nonlinear frequency conversion, the isolation between conversion loss and channels, and the phase noise baseline. Therefore, we designed each functional unit as an independent module to better reduce the impact of external interference. In the implementation, the RF components are placed on a dedicated microwave PCB board in which the high-performance microwave substrate material ensures a more uniform distribution of the dielectric and low loss factors. Each functional module is installed in a shielded aluminum alloy shell. The modules are matched and

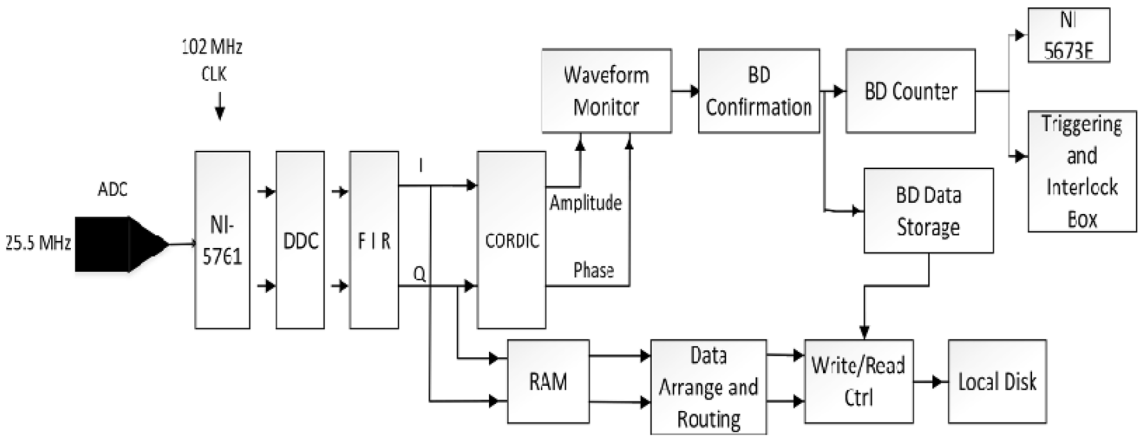


Fig. 2 BD processing schematic

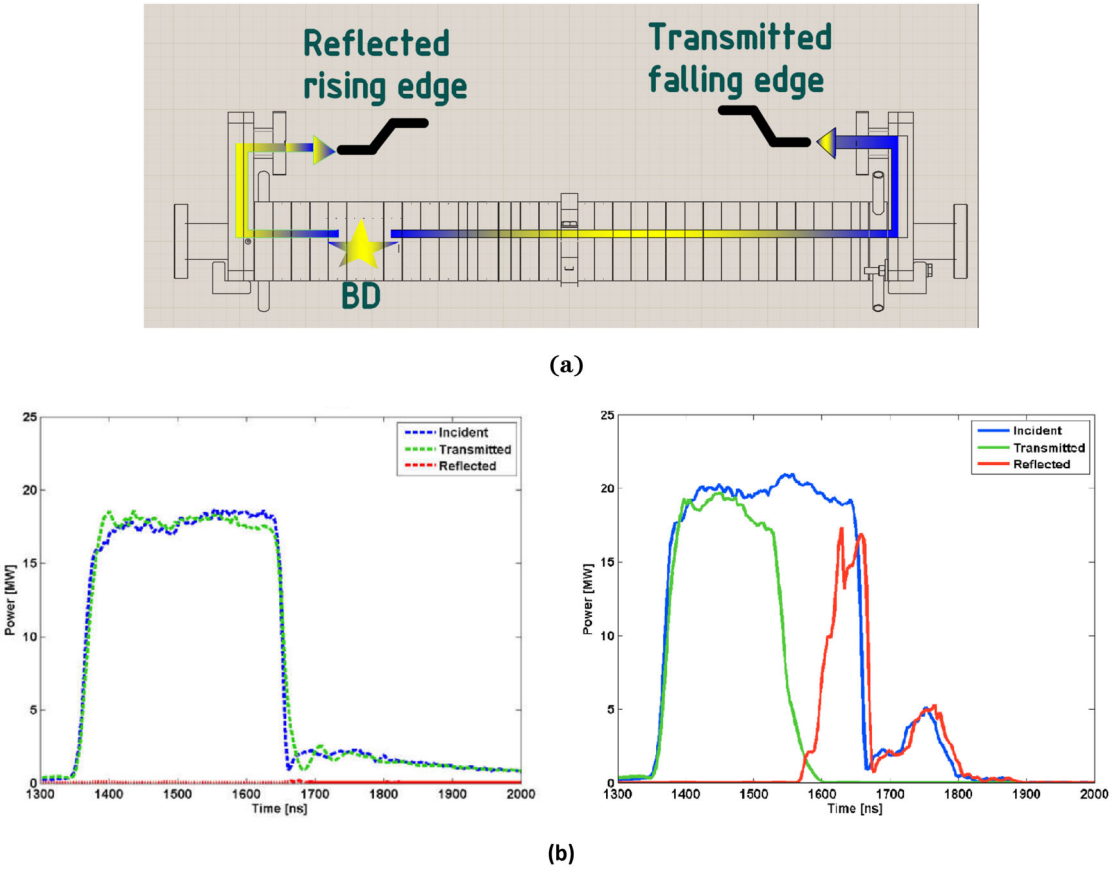


Fig. 3 (Color online) **a** RF signals accompanying a breakdown in the structure. **b** Two pulses during a BD

interconnected through the RF connectors after independent debugging and testing. The compact and uniform heat conduction surface leads to a smaller temperature gradient, which can reduce the influence of the circuit on the impedance matching and working environment. The schematics of the RF-LO box, RF front-end down converter box, and triggering and interlock control box are shown in Fig. 4.

4.1 RF front-end down converter box

The RF frond-end box is responsible for down-converting the pickup RF signals to the IF signals. In Eqs. 4–7, the sampling RF signal is denoted by V_{RF}, the LO signal by V_{LO}, and the IF signal by V_{IF}. After passing through the RF front-end, an IF signal with an amplitude and phase proportional to the original RF signal is obtained, i.e., the basic performance parameters of the RF signal are preserved. This not only makes the design of the digital signal processing module simpler, but also preserves the amplitude and phase information of the original signal to the maximum extent, which can increase the accuracy of further measurements and control.

$$V_{\mathrm{RF}} = \hat{V}_{\mathrm{RF}} \sin(\omega_{\mathrm{RF}} t + \varphi_{\mathrm{RF}}) \tag{4}$$

$$V_{\mathrm{LO}} = \hat{V}_{\mathrm{LO}} \sin(\omega_{\mathrm{LO}} t + \varphi_{\mathrm{LO}}) \tag{5}$$

$$V_{\mathrm{RF}} \otimes V_{\mathrm{LO}} = \frac{1}{2} V_{\mathrm{RF}} \times V_{\mathrm{LO}} \times \{\cos[(\omega_{\mathrm{LO}} - \omega_{\mathrm{RF}})t + (\varphi_{\mathrm{LO}} - \varphi_{\mathrm{RF}})] - \cos[(\omega_{\mathrm{LO}} + \omega_{\mathrm{RF}})t + (\varphi_{\mathrm{LO}} + \varphi_{\mathrm{RF}})]\} \tag{6}$$

$$V_{\mathrm{IF}} = \frac{1}{2} \hat{V}_{\mathrm{RF}} \cdot \hat{V}_{\mathrm{LO}} \cos[(\omega_{\mathrm{LO}} - \omega_{\mathrm{RF}})t + (\varphi_{\mathrm{LO}} - \varphi_{\mathrm{RF}})] \tag{7}$$

For this reason, the 5712 MHz RF signals are down-converted to a 5686.5 MHz LO signal which is in turn converted to a 25.5 MHz IF signal. The IF signal goes through the low-pass filter (LPF) and low-noise amplifier (LNA) and is sampled by the NI 5761 for the conditioning process using quadruple frequency sampling with the 102 MHz clock signal.

4.2 RF-LO box

The RF-LO box provides a clock signal to the digitizers for data acquisition and a LO signal to the RF front-end box. The amplitude and phase stability of the LO signal

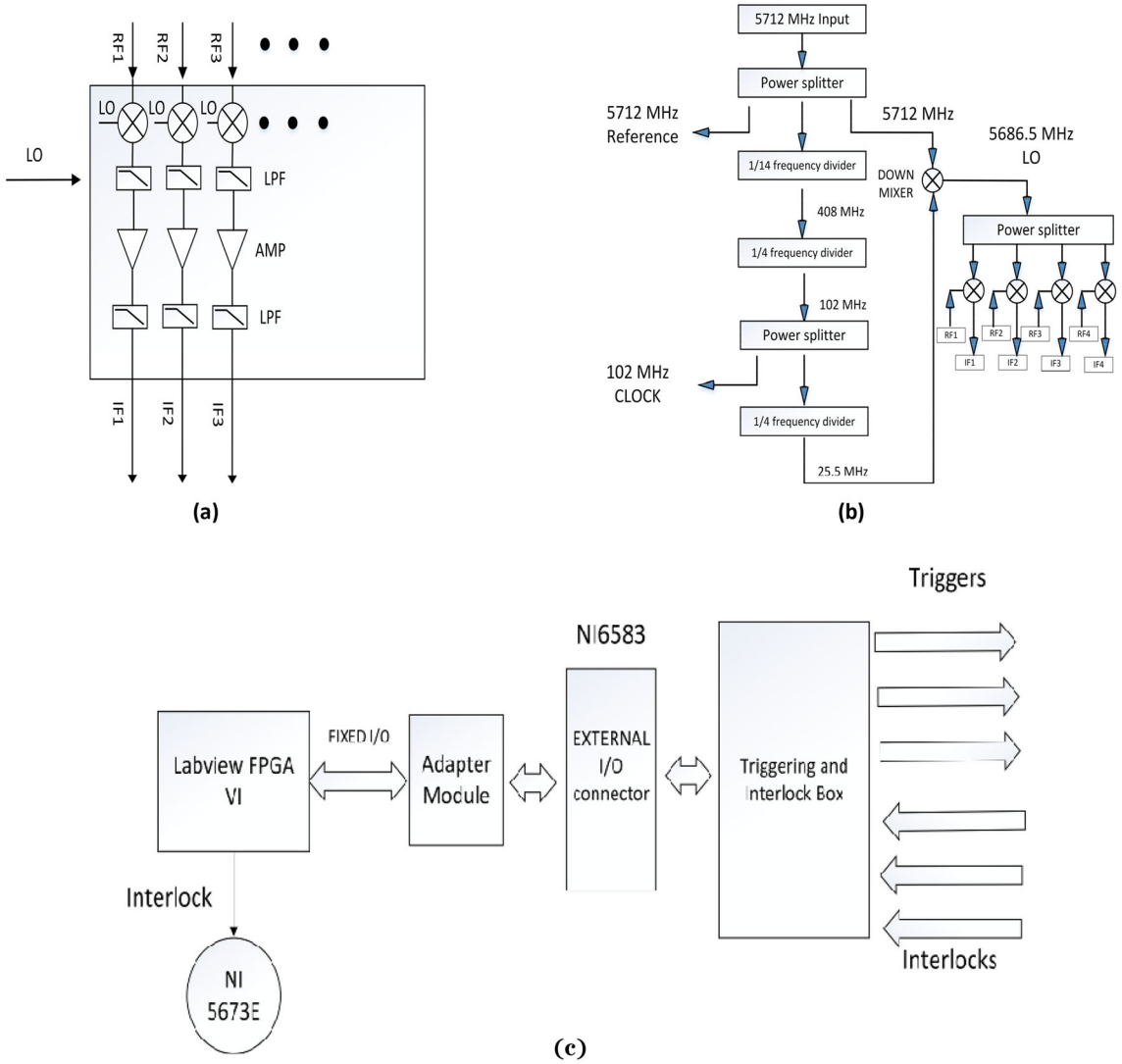


Fig. 4 **a** RF front-end box. **b** RF-LO box. **c** Triggering and interlock control box

and clock signal provided by the RF-LO box impact the performance of the LLRF system directly. The 5712 MHz master oscillator signal provided by the NI PXIe-5673E is divided by 14 to obtain a 408 MHz signal. The 408 MHz is then divided by 4 to obtain a 102 MHz clock signal, which is used as the sampling rate. The 102 MHz signal is in turn divided by 4 and goes through a low-pass filter to generate a 25.5 MHz base signal. At the same time, using a down converter, the master oscillator 5712 MHz signal is mixed with the 25.5 MHz base signal to generate a 5686.5 MHz signal, which can be used as the LO signal.

Previous RF distribution plans implemented in other facilities use 2 RF signal generators locked to a 10 MHz master clock to generate the RF and LO signals. If 10 MHz synchronization is used, phase-locked loop (PLL) or direct digital frequency synthesis (DDS) should be adopted because the difference between the output signal frequency and 10 MHz is very large and is not an integer multiple of the frequency, which may introduce additional phase noise. The near-end phase noise is difficult to control in PLL, and the frequency conversion time is long. The output frequency range in DDS is small, and there can be more spurious signals than expected. For this reason, we usually use a special frequency like 2856 MHz or 119 MHz as the reference signal in the RF-LO box. These frequencies are higher and are integer multiples of the frequency used by the subsystem, which can greatly reduce the complexity of direct synthesis. Finally, the influence of the noise floor of the limiting phase noise in the device is reduced by avoiding the use of high-order frequency division in the system, which may introduce additional phase jitter. This can improve the phase jitter of the entire system. On the other hand, when we multiply or increase the frequency of a signal with good stability, the phase noise is increased,

which is reflected in the deterioration of 20lg$N$. The additional phase jitter is controllable and can approach the theoretical value infinitely closely. However, when we divide the signal frequency, the phase noise should be improved. The frequency division theoretically improves 20lg$N$, but phase jitter will still be introduced because of the local influence of device thermal noise. In general, this limit is about − 153 dbc/Hz at 100 kHz. When the frequency division factor is large enough, the additional phase jitter will be much higher than the theoretical value, especially in the PLL phase discrimination and frequency division processes where the additional impact of the near-end phase noise will be amplified. The newly designed RF-LO box requires only one RF signal generator in our C band LLRF so that all the signals are auto-correlated and additional phase noise can be eliminated in the synchronizing bias.

4.3 Triggering and interlock control box

The triggering and interlock box transfers all the triggers and interlocks from the NI 6583 to the BNC interface. To protect the klystron and accelerating structures from damage, several interlocks are installed in the C band high-gradient test facility. These interlocks include the water, vacuum, modulator status, and BD interlock. When an interlock occurs, the RF output signals will be turned down and the triggers for the modulator and SSA stopped. In this status, the BD interlock will be processed by the FPGA, while the other interlocks will go through the LABVIEW software.

The NI 6583 FPGA extender card is used to distribute the triggering signals and receive the interlock signals. The NI 6583 can provide digital *I*/*O* to interface with single-ended, differential, and serial signals with the FlexRIO PXI FPGA module or the controller. It has 35 *I*/*O* channels which can be individually configured to be input or output channels. To connect the NI 6583 with the other devices, we built a triggering and interlock box to transfer all the triggers and interlocks from the NI 6583 to the BNC interface. Through this trigger box, the triggering signals are distributed to the SSA and klystron. Meanwhile, the interlock signals, such as the vacuum and water interlocks, are sent back to the FPGA for further processing.

5 LABVIEW VI

5.1 LLRF modules

We designed LABVIEW GUIs for the RF pulse generator control module, the BD definition module, the waveform monitor module, the triggering control module, the modulator control module, and the real-time beam voltage monitoring module (Fig. 5).

In the RF pulse generator control module, the power level, pulse length, and phase reversal time of the RF output signal can be controlled. In the BD definition module, the relevant parameters for defining a BD can be controlled. The waveform monitor module displays the real-time waveform of each channel and whether there is an interlock status or not. In the triggering control module, the PXI 6583 module can be used to control the trigger for the klystron and SSA through the timing and interlock box by adjusting the delay and pulse length of the triggers. To communicate with the modulator, we use Ethernet to connect with the modulator control module. The beam voltage control module of the modulator is a Siemens S7-200. We used the OPC server module in LABVIEW to implement the connection with LABVIEW in the modulator control module. All the statuses of the modulator, including the beam voltage and the beam current, are monitored in this module. The real-time beam voltage monitoring module displays the beam voltage curve over a period of time and records the curve to the hard disk.

Differing from the acquisition of the RF single-band or narrowband modulated signal, the real-time BD data require long-period acquisition and storage. The sample rate of our FlexRIO NI 5761 digitizer adapter modules is 250 MS/s. A huge amount of data enters the data buffer using FIFO with large throughput; after filtering, routing, and synchronization, the data will be stored in the RAM. After data integration, routing, and synchronization, the data sequence is controlled by the read/write controller and stored in external memory. The whole data transmission process is completed by the high-speed PXIe bus. When a BD is detected, the 3 pulse waveforms before the occurrence of the BD, the pulse waveform when the BD occurs, and 1 pulse waveform after the BD occurs are saved.

5.2 Conditioning algorithm

To ensure that all the parameters can be modified during the conditioning progress, we designed a conditioning control panel. The parameters in the conditioning panel are the current highest beam voltage, current beam voltage, current vacuum status, final beam voltage, vacuum threshold value, beam voltage decrease when BD occurs, step voltage without BD occurrences, step time interval without BD occurrences, step voltage when recovering to the highest beam voltage, step time interval when recovering to the highest beam voltage, beam voltage decrease when the vacuum breaks, and the BD count per hour threshold value. The interface of the conditioning control panel is shown in Fig. 6a. The basic conditioning algorithm is shown in Fig. 6b. The conditioning process should

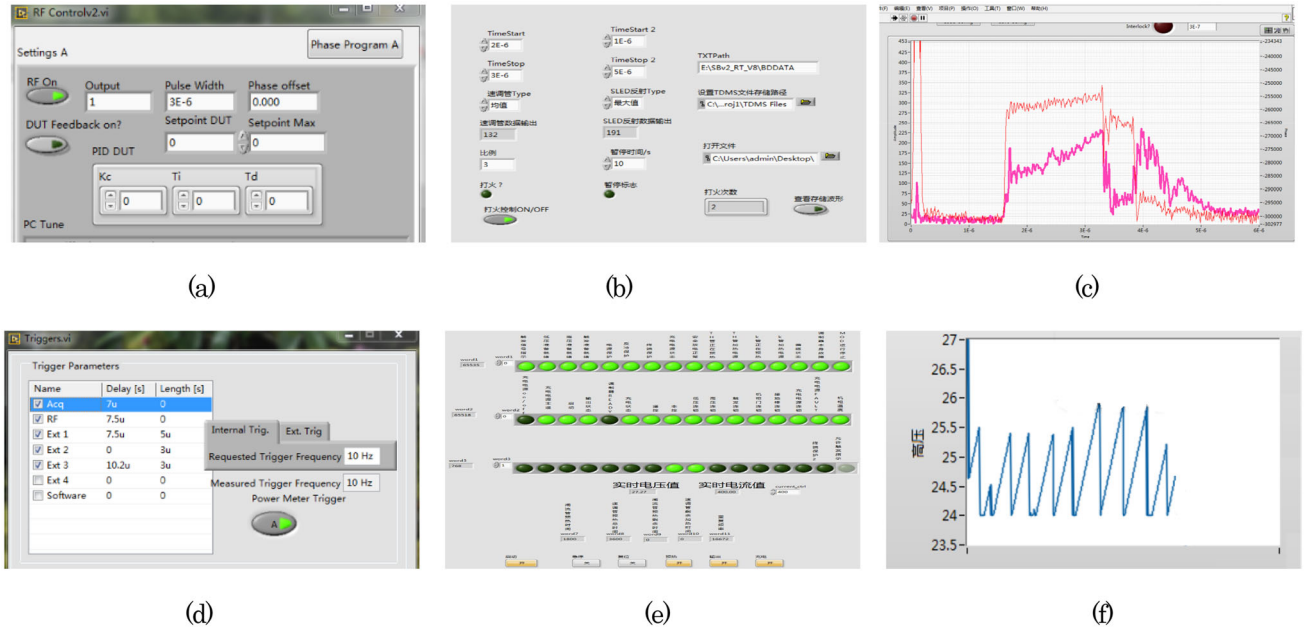
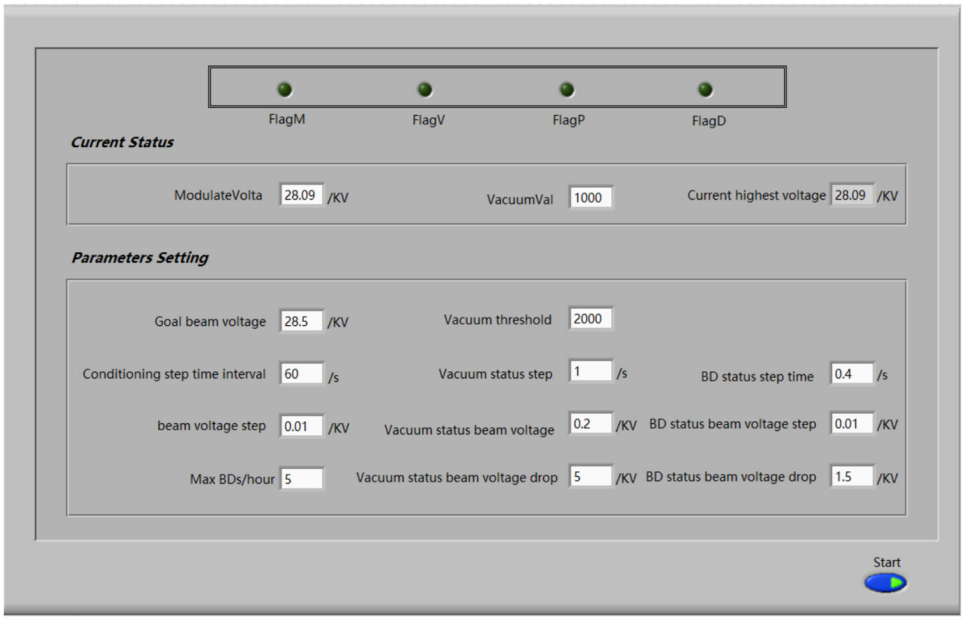


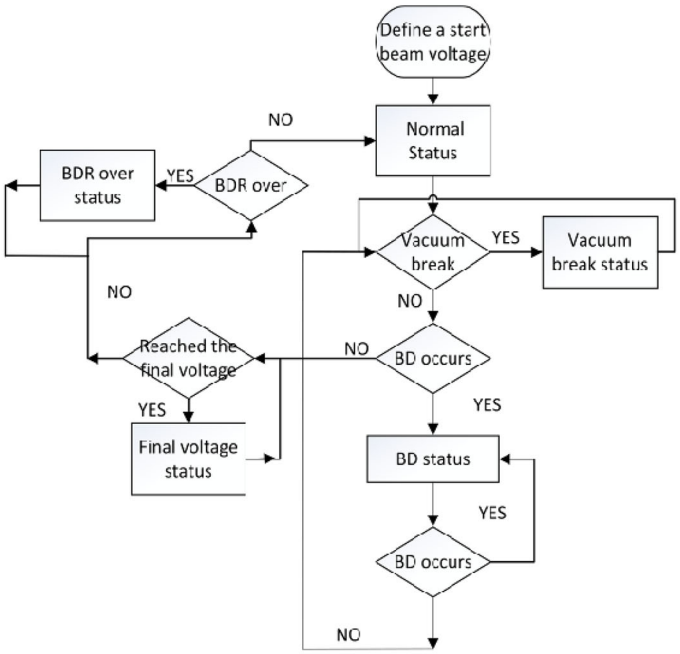
Fig. 5 **a** RF pulse generator control module. **b** BD definition control module. **c** Waveform monitor module. **d** Triggering control module. **e** Modulator control module. **f** Real-time beam voltage monitoring module

follow the rules below. The main parameters in the conditioning process are shown in Table 2.

- Normal status
  - In normal status where no BD occurs, the beam voltage would rise by 0.01 kV every N seconds. (N is normally 10–200 and can be adjusted in the conditioning control panel. N is increased as the beam voltage rises.)
- Vacuum break status
  - If the vacuum read back value is higher than the threshold value V, decrease the beam voltage from the current highest beam voltage N_{vac} (normally 8 kV, adjustable in the conditioning control panel). The RF signal source and the triggers for the modulator and SSA will be stopped for ten seconds, and the system enters the vacuum recovery mode.
  - If no BD and vacuum breaks occur during the vacuum recovery mode, return the beam voltage to the value before the vacuum break occurred. The recovery time interval (adjustable in the conditioning control panel) will be shorter than that in the normal status, and the recovery beam voltage step (adjustable in the conditioning control panel) will be larger than in the normal status. When the beam voltage has recovered to the voltage before the vacuum break occurred, return to normal status.
  - If BD or vacuum break occurs during the vacuum recovery mode, the RF signal source and the triggers for the modulator and SSA will be stopped for ten seconds, after which the system will return to the start of the vacuum recovery mode.
- BD status
  - If BD occurs and the vacuum does not exceed the threshold value V (normally 4×10^{-8} Pa, adjustable in the conditioning control panel) and the BD counts in one hour do not exceed N (adjustable in the conditioning control panel), decrease the beam voltage from the current highest beam voltage of M kV (normally 0.5 kV–1 kV, adjustable in the conditioning control panel, and increased with increasing beam voltage) and stop the RF signal source and the triggers for the modulator and SSA for ten seconds, then recover the beam voltage to the highest value before the BD occurred. The recovery time interval (adjustable in the conditioning control panel) will be shorter than in the normal status, and the recovery beam voltage step (adjustable in the conditioning control panel) will be larger than in the normal status.
  - If there is no BD and no vacuum break during the BD recovery progress, when the beam voltage has recovered to the highest voltage before the BD occurred, return to normal status.
  - If BD occurs during the BD recovery process, the beam voltage will revert to the voltage when the recovery process started, and the RF signal source and the triggers for the modulator and SSA will be



(a)



(b)

stopped for ten seconds, after which the BD recovery process will be restarted again.

- If the vacuum read back value is worse than the threshold value V during the BD recovery progress, decrease the beam voltage from the current highest beam voltage N_{vac} (normally 8 kV, adjustable in the conditioning control panel). The RF signal source and the triggers for the modulator and SSA will be stopped for ten seconds, after which the system enters the vacuum break status.
- BDR over status
  - If there is no BD or vacuum break but the BD count in one hour exceeds N_{BD} (adjustable in the

Table 2 The main parameters in the conditioning process

Conditioning parameter	Value range
Conditioning step time (s)	10–120
Conditioning beam voltage increment step (kV)	0.01
Vacuum threshold value (Pa)	4×10^{-8}
Beam voltage decrease when vacuum break occurs (kV)	5–8
Vacuum break status recovery time interval (s)	0.5–5
Vacuum break status recovery beam voltage step (kV)	0.01–0.2
BD counts	5 per h
Beam voltage decrease when BD occurs (kV)	2–5
BD status recovery time interval (s)	0.5–5
BD status recovery beam voltage step (kV)	0.01–0.2

conditioning control panel), do not increase the beam voltage until the BD count drops to a value under *N*, and then return to normal status.

- Final status
  - If the beam voltage has reached the final voltage, do not increase the beam voltage and return to normal status.

6 Test results

The high-gradient test facility is located in the Jiading Campus of the Shanghai Institute of Applied Physics and shares the same tunnel as SDUV-FEL (Shanghai Deep Ultraviolet-Free-Electron Laser). The conditioning plan is shown in Table 3. The RF power was gradually increased by the conditioning algorithm until the target beam voltage was reached. When the beam voltage reached the beam voltage value of the target gradient, the next conditioning step was applied. There was no need to reduce the beam voltage to the value at the very beginning of the first conditioning process. Here, we reduced the beam voltage to 31 kV, increased the RF pulse length and shift time simultaneously, and repeated the conditioning process until the next target value was reached.

Table 3 The conditioning plan for C band structures

Pulse length (ns)	Shift time (ns)
1000	200
1400	280
1800	360
2200	440
2500	500

As shown in Table 3, the initial pulse length and shift time were 1000 ns and 200 ns, respectively. These values can guarantee a thorough pulse compression process under about half the filling time of the accelerating structure. The pulse length and shift time were then increased separately [18, 19].

Figure 7a shows the recorded data during the conditioning process. All the waveform data entered the data buffer FIFO and were stored in the RAM after filtering, routing, and synchronization. When a BD occurred, 3 waveforms before the BD, the waveform when the BD occurred, and 1 waveform after the BD were recorded. The recording interval is related to the repetition rate of the whole operating system.

In the recorded BD data, we can see clearly that when a BD occurred, the reflected power jumped to a high level. The reflected power protection interlock was released immediately, and the RF output and pulse trigger signals for the klystron and SSA held simultaneously for 10 s. After 10 s, the RF output signal and triggers for the klystron and SSA has recovered to the status before the BD occurred.

In the beam voltage rising trend graph in Fig. 7b, the abscissa is the time and the ordinate is the current highest beam voltage. The BDR is inversely proportional to the electric field strength, so when the beam voltage was low (the klystron output power was low), the probability of BD was not high and the conditioning could progress smoothly. When the beam voltage rose to about 23 kV, the conditioning progress slowed down because of the absorbed gas in the waveguide. After most of the absorbed gas has been released from the waveguide, the beam voltage continued to rise slowly until it was close to the target beam voltage. At this time, the output microwave power of the klystron was very high, and the electric field in the accelerating structure was large enough to cause continuous BD. When we found that there were too many continuous BD occurrences within a certain period of time during the conditioning process, we reduced the beam voltage and restarted

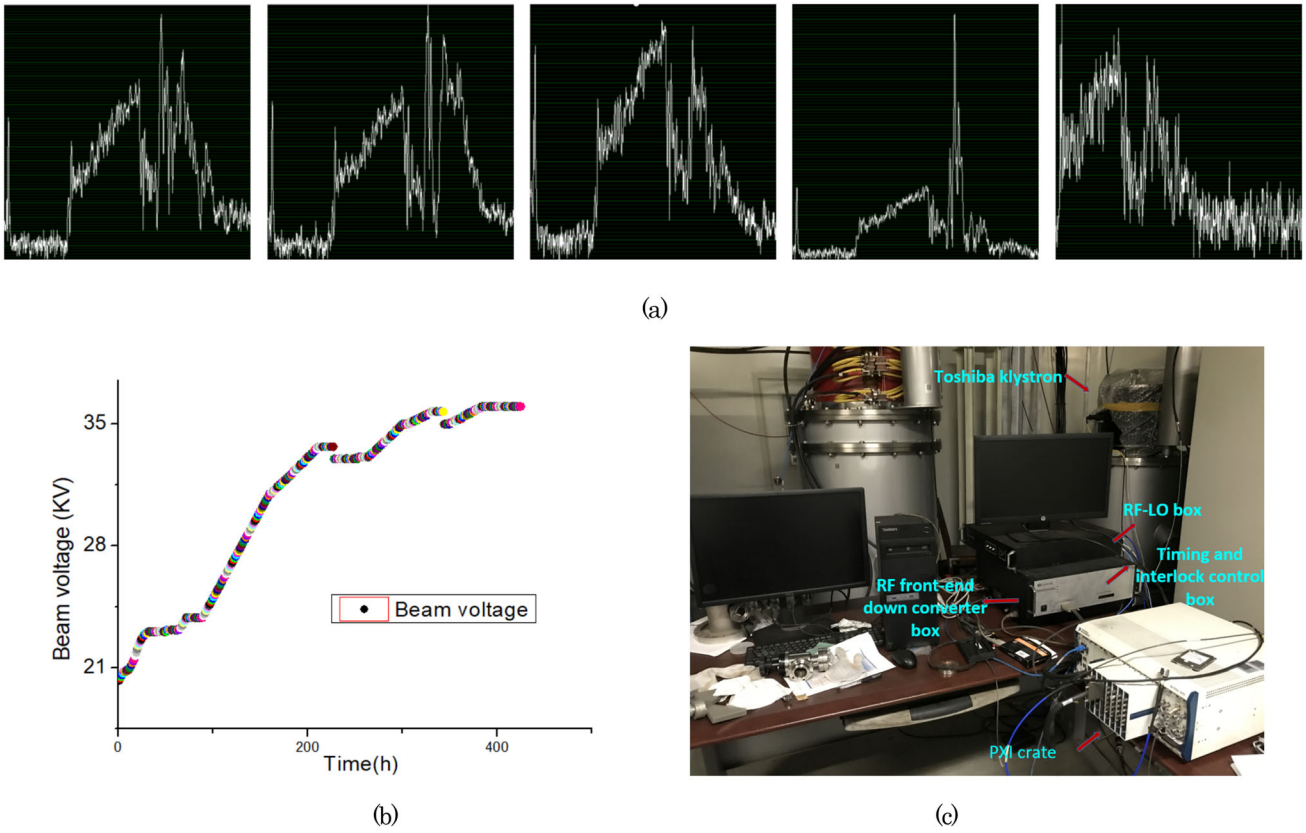


Fig. 7 (Color online) **a** BD waveform storage. **b** Entire beam voltage rising trend. **c** Site photograph

the conditioning from a lower beam voltage until we could pass through the beam voltage points where the BD had occurred frequently with a low BDR.

The gradient of the C band accelerating structure can be calculated by Eq. (8), in which E is the gradient in MV/m and P is the power delivered to the C band accelerating structure in MW [20, 21]:

$$E = 40\sqrt{\frac{P}{90}}. \tag{8}$$

When the beam voltage reached the goal voltage corresponding to the gradient required by the SXFEL-LINAC theoretical design (Table 4) and the accelerating structure could operate with a low BDR (less than 10^{-4} breakdowns per pulse) for more than 24 h, we considered the accelerating structure to be fully conditioned and ready for installation in SXFEL-LINAC.

After thorough conditioning, 3 C band accelerating structures and one pulse compressor were installed in the SXFEL-LINAC and are currently operating in good condition.

7 Conclusion

The LLRF part of a high-gradient test facility has been developed for the SXFEL-LINAC. The auto-conditioning algorithm has been proven to be suitable for the C band accelerating structure conditioning process. Three C band accelerating structures and 1 pulse compressor have been pre-conditioned and installed in the SXFEL-LINAC and

Table 4 SLED output power vs average gradient (MV/m)

Beam voltage (kV)	SLED output power without attenuation (MW)	Average gradient (MV/m)
36	102.5651926	42.70106793
35.5	99.31160484	42.01832507
35	94.84184633	41.06187122
34.5	91.41132415	40.31240761
34	88.1048873	39.57662325

are operating in good condition. The whole LLRF system is still in the design improvement stage. In the future, we will add functions such as a BD auto-locator to this LLRF system.

References

1. C. Feng, H.X. Deng, Review of fully coherent free-electron lasers. Nucl. Sci. Tech. **29**, 160 (2018). https://doi.org/10.1007/s41365-018-0490-1
2. M. Altarelli, From 3rd- to 4th-generation light sources: free-electron lasers in the X-ray range. Crystallogr. Rep. **55**, 1145–1151 (2010). https://doi.org/10.1134/S1063774510070072
3. M.W. Guetg, A.A. Lutman, Y. Ding et al., Generation of high-power high-intensity short X-ray free-electron-laser pulses. Phys. Rev. Lett. **120**, 014801 (2018). https://doi.org/10.1103/PhysRevLett.120.014801
4. Z.T. Zhao, D. Wang, L.X. Yin et al., Shanghai soft X-ray free-electron laser facility. Chin. J. Lasers **46**(1), 0100004 (2019). https://doi.org/10.3788/CJL201946.0100004 (**in Chinese**)
5. Z.T. Zhao, C. Feng, K. Zhang, Two-stage EEHG for coherent hard X-ray generation based on a superconducting linac. Nucl. Sci. Tech. **28**, 117 (2017). https://doi.org/10.1007/s41365-017-0258-z
6. Z.T. Zhao, D. Wang, Q. Gu et al., Status of the SXFEL facility. Appl. Sci. **7**, 607 (2017). https://doi.org/10.3390/app7060607
7. Z. Wang, C. Feng, Q. Gu et al., Generation of double pulses at the Shanghai soft X-ray free electron laser facility. Nucl. Sci. Tech. **28**, 28 (2017). https://doi.org/10.1007/s41365-017-0188-9
8. J.G. Wang, B. Liu, Development of readout electronics for bunch arrival-time monitor system at SXFEL. Nucl. Sci. Tech. **30**, 82 (2019). https://doi.org/10.1007/s41365-019-0594-2
9. Z.Q. Geng, Beam-based optimization of SwissFEL low-level RF system. Nucl. Sci. Tech. **29**, 128 (2018). https://doi.org/10.1007/s41365-018-0460-7
10. M. Hou, Z.S. Zhou, RF power test and conditioning of the new accelerating structures for the BEPC II-Linac. High Energy Phys. Nucl. Phys. **29**(1), 80–85 (2005). https://doi.org/10.1088/1009-0630/7/5/006
11. J.W. Wang, G.A. Loew, Progress report on new RF breakdown studies in an S-band structure at SLAC, *Presented at the 1987 Particle Accelerator Conference* (Washington, DC, 1987). https://www.osti.gov/servlets/purl/6161270
12. M. Jacewicz, R. Ruber, V. Ziemann, J.W. Kovermann, Instrumentation for the 12 GHz stand-alone test-stand to test CLIC acceleration structures, in *Proceedings of IPAC2011* (San Sebastian, 2011). https://ir.ihep.ac.cn/handle/311005/232320
13. A. Degiovanni, W. Wuensch, Comparison of the conditioning of high gradient accelerating structures. PhysRevAccelBeams (2001). https://doi.org/10.1103/PhysRevAccelBeams.19.032001
14. J.H. Tan, W.C. Fang, D.C. Tong et al., Design, RF measurement, tuning, and high-power test of an X-band deflector for Soft X-ray free electron lasers (SXFEL) at SINAP. Nucl. Inst. Methods Phys. Res. A **930**, 210–219 (2019). https://doi.org/10.1016/j.nima.2019.03.093
15. X.X. Huang, A. Grudiev, Z.T. Zhao et al., CLIC380: RF design and parameters of 2017 re-baselined 380 GeV CLIC linac accelerating structure. Nucl. Inst. and Methods A **916**, 230–237 (2019). https://doi.org/10.1016/j.nima.2018.11.104
16. B. Woolley, *High Power X-band RF Test Stand Development and High Power Testing of the CLIC Crab Cavity* (Lancaster University, Lancaster, 2015), p. 173
17. W. Wuensch, *Advances in the understanding of the physical processes of vacuum breakdown*, Report No. OPEN-2014-028; Report No. CLIC-Note-1025, CERN, 2014. https://doi.org/10.1142/9789814602105_0003
18. W.C. Fang, *C-band high-gradient accelerating structure for compact X-ray free electron lasers* (The University of Chinese Academy of Sciences, Shanghai Institute of Applied Physics, 2012)
19. Z.B. Li, A. Grudiev, W.C. Fang et al., Radio-frequency design of a new C-band variable power splitter. Nucl. Sci. Tech. **30**, 100 (2019). https://doi.org/10.1007/s41365-019-0611-5
20. S.P. Zhong, M.H. Zhao, Q. Gu et al., Waveguide phase length measurement and adjustment of 150 MeV Linac. SSRF. Nucl. Tech. **32**(7), 501–504 (2009) (**in Chinese**)
21. W.C. Fang, L. Wang, Z.T. Zhao, Conceptual study and design of A C-band photocathode injector. Radiat. Detect. Technol. Methods **3**, 39 (2019). https://doi.org/10.1007/s41605-019-0117-z