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Comparison of D-flip-flops and D-latches: influence on SET susceptibility of the clock distribution network

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Abstract As technology scales down, clock distribution networks (CDNs) in integrated circuits (ICs) are becoming increasingly sensitive to single-event transients (SETs). The SET occurring in the CDN can even lead to failure of the entire circuit system. Understanding the factors that influence the SET sensitivity of the CDN is crucial to achieving radiation hardening of the CDN and realizing the design of highly reliable ICs. In this paper, the influences of different sequential elements (D-flip-flops and D-latches, the two most commonly used sequential elements in modern synchronous digital systems) on the SET susceptibility of the CDN were quantitatively studied. Electrical simulation and heavy ion experiment results reveal that the CDN-SET-induced incorrect latching is much more likely to occur in DFF and DFF-based designs. This can supply guidelines for the design of IC with high reliability.

Keywords Clock distribution network · D-flip-flop · D-latch · Reliability · Single-event transient · Susceptibility

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1 Introduction

It has been shown that clock distribution networks (CDNs) are becoming increasingly vulnerable to transient faults known as single-event transients (SETs) [1–4] due to scaling down of technology [5]. In the deep submicron regime, the clock network contributes significantly to the chip-level soft error rate (SER) [5–8] and radiation particle strikes on the CDN can even prove to be catastrophic [9]. Because one clock node generally feeds more than one sequential element, a radiation strike on one such node may cause multiple errors to be propagated [5]. An abnormal behavior in the whole system may be generated if the clock is altered by radiation effects [6]. However, few research efforts have addressed the problem of radiation particles striking on the CDN in an integrated circuit (IC) [5, 7–9]. Understanding the factors that influence the susceptibility of the CDN is crucial for radiation hardening of the CDN and thus for the design of a highly reliable IC.

Latches and flip-flops are the two most commonly used sequential elements in modern synchronous digital systems [10–12]. There have been many publications addressing the topic of comparative analysis of latches and flip-flops for high-performance, low-power, and area-efficient systems [13–15]. A latch is smaller, faster, and less power-consuming than a flip-flop. Nowadays, there is an increase in designs based on latches [13–16] instead of flip-flops in the shift register [13, 14] and other synchronous sequential circuits [15] to achieve power reduction, area reduction, and higher performance.

Due to their different trigger modes, different types of sequential elements have significant influences on the SET susceptibility of the CDN. Using their simulation methodology, Seifert et al. [7] compared the clock node

SERs in the master–slave flip-flop (M/S FF) and pulsed latch, both of which are essentially edge-triggered sequentials. In this paper, we quantitatively study the influences of D-flip-flops (DFFs) and D-latches, which can replace DFFs in some cases [15], on the SET susceptibility of the CDN by electrical simulations and heavy ion irradiation experiments. We comparatively study the incorrect data latching caused by SETs on CDNs in the DFF-based design and optimized design in which some FFs were replaced by D-latches. This study will supply information for the design of IC with high reliability.

2 CDN-SET-induced incorrect latching

SETs on the CDN do not always result in incorrect data latching in the receiving sequential elements, which is called as CDN-SET-induced incorrect latching in this paper. As shown in Fig. 1, whether the CDN-SET-induced incorrect latching will occur strongly depends on the type of the receiving sequential element. Therefore, the type of the sequential element has a significant influence on the SET susceptibility of the CDN.

Radiation on the CDN may introduce two new clock edges on the clock signal (radiation-induced clock race) or cause the clock edge to deviate from its expected transition time (radiation-induced clock jitter). In edge-sensitive sequential elements such as DFFs, if a new trigger edge appears or jitter of the trigger edge occurs, the data input is different from its storage state and the setup and hold times are satisfied. Consequently, a CDN-SET-induced incorrect latching occurs. In level-sensitive sequential elements (such as D-latches), when an effective level occurs on the clock signal during its hold period and the data input is different from its storage state, a CDN-SET-induced incorrect latching occurs. According to the trigger modes of the sequential elements, the duration of the CDN-SET-induced incorrect latching in edge-sensitive elements is usually much longer than that in level-sensitive sequential elements.

3 Simulation and experimental setups

The dynamic analysis method proposed in [17] is adopted in this paper. In all simulations, the current induced by ion strike was modeled as a double-exponential function current source, which could represent the electrical effect of particle striking [18–20]. In HSPICE simulations, the equation for the current pulse is

$$I(t) = \begin{cases} 0 & t < td1 \\ Ipeak\left[1 - e^{\frac{-(t-td1)}{\tau_1}}\right] & td1 < t < td2 \\ Ipeak\left[e^{\frac{-(t-td2)}{\tau_2}} - e^{\frac{-(t-td1)}{\tau_1}}\right] & t > td2 \end{cases} \quad (1)$$

where $Ipeak$ is the maximum current to be approached, $td1$ is the onset of rise in current, $td2$ is the onset of fall in current, τ_1 is the rise time constant, and τ_2 is the fall time constant.

The double-exponential function usually has a rapid rise time and gradual fall time [20]. In our simulations, τ_1 and τ_2 were set to 2 ps and 10 ps, respectively. This setting was made by referring to [20]. The maximum current $Ipeak$

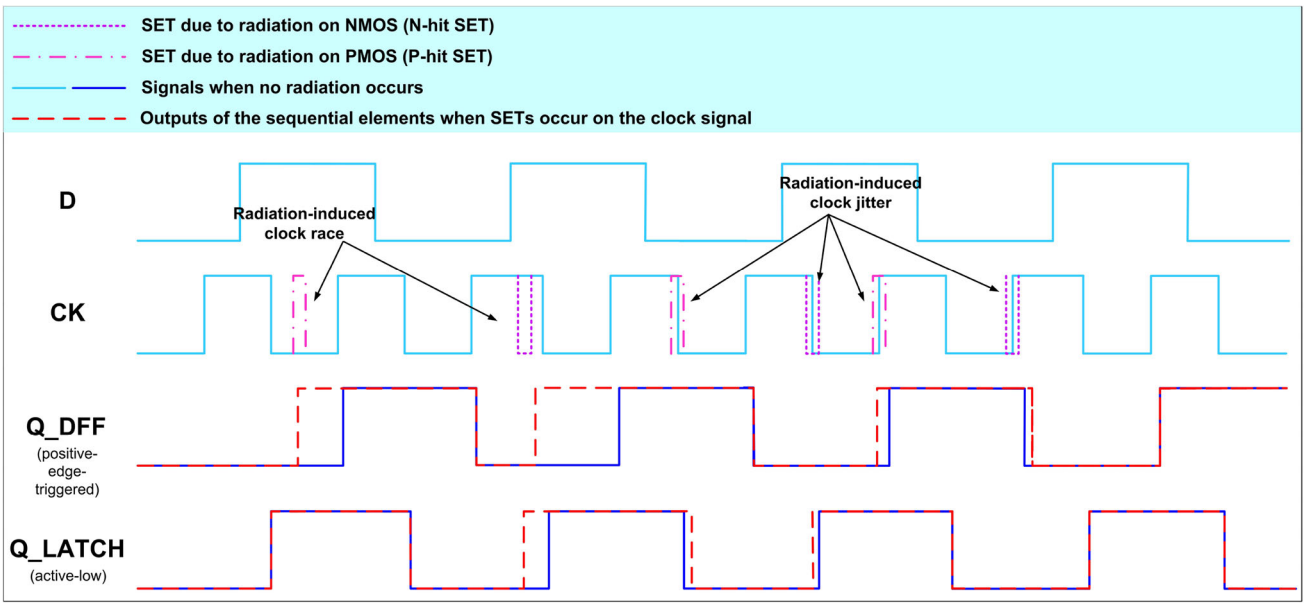

Fig. 1 (Color online) SETs on the clock signal and the CDN-SET-induced incorrect data latching in different sequential elements

was set to produce a full-swing voltage transient. Because *Ipeak* is usually related to factors such as size of the circuit and supply voltage, it was set to different values in the simulations for a single sequential element and in the simulations for the case study circuit. In all simulations, $td1$ was random during the simulation time, and ($td2$ - $td1$) was random in a certain range to produce the SET voltage pulses with different widths.

Functional schematics of the DFF and D-latch studied in this paper are shown in Fig. 2. Figure 2a, b depicts an unhardened positive-edge-triggered, static DFF and an unhardened active-low D-type transparent latch, respectively. For a fair comparison, the DFF and D-latch with similar drive capabilities were selected in the electrical simulations and heavy ion irradiation experiments. All simulations in Sects. 3.1 and 3.2 are based on layout extracted netlists.

3.1 CDN-SET-induced incorrect latching in a single sequential element

The circuits shown in Fig. 3 are used for comparative study of the incorrect data latching caused by SET on the clock signal in a single sequential element. In the simulations of the circuits shown in Fig. 3, *Ipeak* was set to 1 mA.

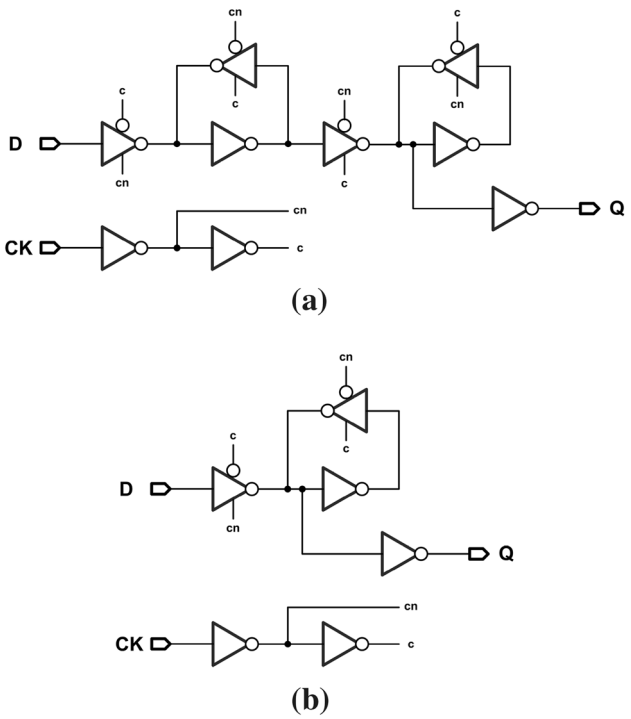

Fig. 2 Functional schematics of the sequential elements studied: **a** unhardened positive-edge-triggered DFF, **b** unhardened active-low D-type transparent latch

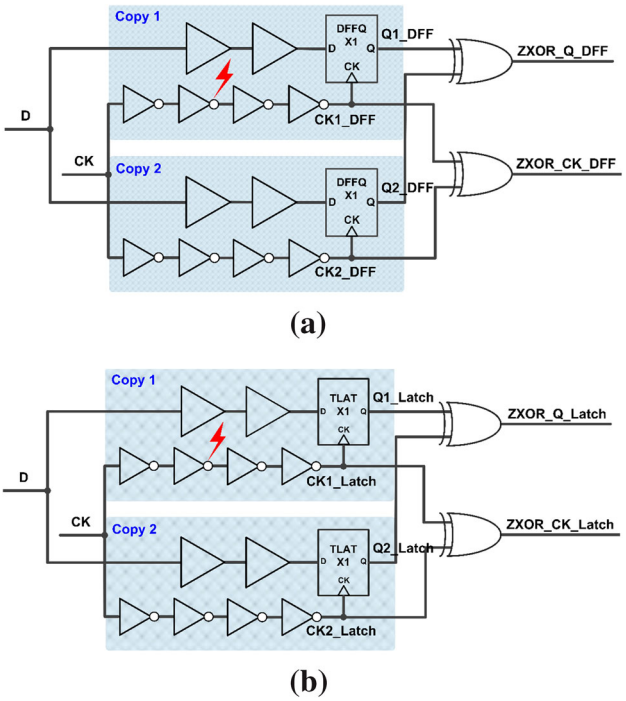

Fig. 3 (Color online) Circuits used for comparative study of the CDN-SET-induced incorrect latching in a single sequential element

As shown in the figures, in the simulations, an SET was injected in copy 1 and the signals in copy 2 could be treated as reference signals. As shown in Fig. 3a, two clock signals in the two copies (CK1_DFF and CK2_DFF) were connected to two inputs of one XOR cell. From the output ZXOR_CK_DFF of this XOR cell, we could determine whether there was an effective SET occurring on CK1_DFF and the pulse width of the effective SET. Similarly, the outputs of the two copies (Q1_DFF and Q2_DFF) were connected to two inputs of another XOR cell. From the output ZXOR_Q_DFF of this XOR cell, we could determine whether CDN-SET-induced incorrect data latching occurred and how long it lasted. The circuit shown in Fig. 3b, which is used for simulations of the D-latch, is similar to that in Fig. 3a.

In the simulations, the clock input CK in Fig. 3a, b was stimulated by one clock signal. The data inputs D in the two circuits were also stimulated by one data signal. Both the clock signal and data signal changed periodically. Considering that the clock signal usually operates at the highest speed, we set the data cycle to double of the clock cycle.

3.2 Comparative study in a case circuit

Based on the dynamic analysis method in [17, 21], we evaluated the SET susceptibility of the CDN in a DFF-based design and in an optimized design of a case circuit.

The two designs were identical except for the type of the sequential elements. This can make the comparative study result more accurate. By analyzing the function and timing behavior of each flip-flop, we replaced some positive-edge-triggered flip-flops in the case circuit with active-low D-latches in the optimized design according to [15]. In the simulations, both designs worked in real time, the injection location of the SET traversed all clock nodes on the CDN, the injection time of the SET was random, and the SET pulse width was random within a certain range. The IC operation in the real radiation environment might be hindered by radiation particles at any position and at any time. The pulse width of the SET occurrence varies with the type of the radiation particles, supply voltage, temperature, angle of incidence, and so on. Therefore, our simulations could more realistically reflect the IC operation after radiation in the aerospace and therefore could make the obtained information more truthful and accurate.

The DFF-based design of a case circuit was implemented first by Encounter from Cadence using 65-nm bulk complimentary metal-oxide semiconductor (CMOS) technology. Then, the DFFs that could be replaced by D-latch were replaced by D-latches with similar drive capabilities. Because the area of the D-latch is less than that of the DFF with similar drive capability, the replacement would not introduce violation or short in the design. In this way, we could get the optimized design, which was exactly the same with the DFF-based design.

For the sake of higher simulation accuracy, the files including the detailed standard parasitic format (DSPF) files of all designs were extracted and used for simulations. According to [17], two selfsame copies of the DSPF file of the DFF-based (optimized) design were included in one HSPICE netlist. As shown in Fig. 4, two duplicates of the output Q of the same sequential element were connected, respectively, to the two inputs of one XOR cell (Q_XOR1 to Q_XORn) to study the CDN-SET-induced incorrect latching in each sequential element. The "n" in "Q_XORn" is the total number of sequential elements connected to the clock leaf nodes in the case circuit.

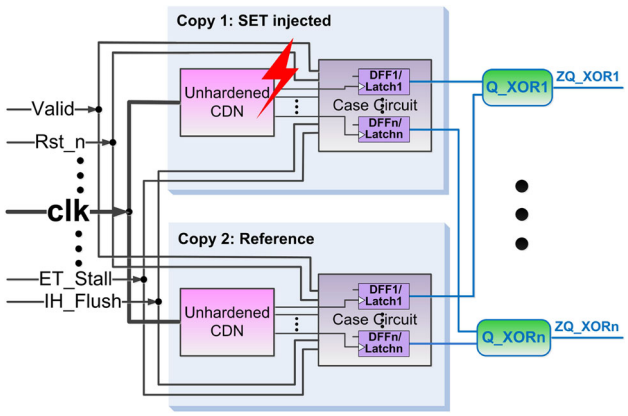

Fig. 4 (Color online) Dynamic SET sensitivity analysis method for CDN

In each simulation, the same inputs of the two copies were stimulated by one signal, and an SET was injected at one clock node in copy 1. Because there was no SET injection in the other copy, its signals could be treated as reference signals. If the SET propagating to the leaf clock nodes induced an incorrect data latching in the receiving sequential element, a pulse would appear at the output of the corresponding XOR cell. The duration of the pulse represented the duration of incorrect latching.

In the simulations of the case circuit, *Ipeak* was set to 725 μA. The simulations were controlled by a shell script. All the simulations traversing all clock nodes on the CDN could be implemented automatically by running the script. Even if the simulations were interrupted for some reason, we could restart the simulations by modifying the node list. Information, such as the name of the sequential element with CDN-SET-induced incorrect latching and the duration of the incorrect latching, would be recorded. By comparing the numbers and durations of incorrect latching in the DFF-based design and optimized design, we can obtain the relative SET susceptibility of the CDN in each design.

3.3 Heavy ion irradiation experiment setup

To further investigate the influence of the type of the sequential element on the SET susceptibility of the CDN, we designed a test chip in 130-nm bulk CMOS technology. This test chip was fabricated at Semiconductor Manufacturing International Corporation (SMIC). This test chip includes eight test chains. Four of the chains, which were numbered 1, 3, 5, and 7, are used for the comparative study. The constructions of these four chains are shown in Table 1 and Fig. 5.

The test chains were designed by referring to the shift register with latches in [14] and that with flip-flops in [22]. The differences between the four test chains are in terms of the presence of SET target (combinational logic element at the data input of the sequential element) and the kind of sequential element that is adopted. For the first chain (Number 1 in Table 1 shown in Fig. 5a), which is referred to as SETtarget_Latch_chain, there are buffers at the data inputs of the D-latches. For the second chain (Number 3 in Table 1 shown in Fig. 5b), which is referred to as SET-target_DFF_chain, there are buffers at the data inputs of the DFFs. For the third and fourth chains (Numbers 5 and 7 in Table 1 shown in Fig. 5c, d), respectively, which are referred to as Latch_chain and DFF_chain in the test chip, there is no combinational logic at the data inputs of the D-latches and DFFs.

Table 1 Constructions of the four test chains

No. of chains	Combinational logic	Clock inverter	Sequential logic
1	Buffer	Unhardened	D-Latch
3	Buffer	Unhardened	DFF
5		Unhardened	D-Latch
7		Unhardened	DFF

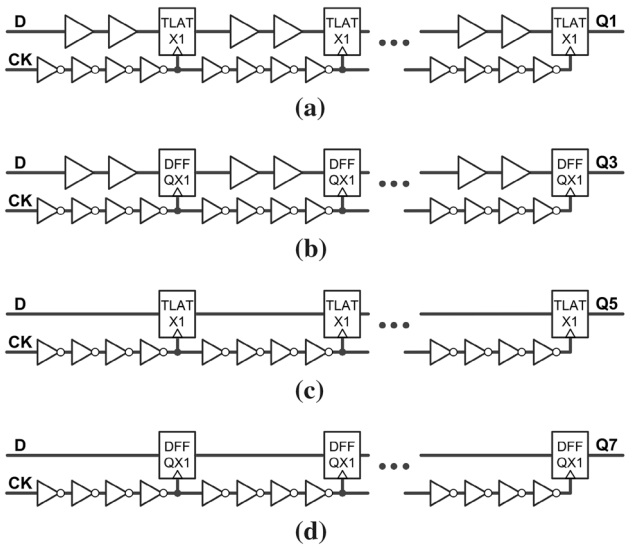

Fig. 5 Schematic of the four test chains used for the comparative study

In the four test chains, all sequential elements were hardened by the dual interlocked storage cell (DICE) [23] technique. All data inputs of the sequential elements were hardened by the time redundancy technique [24, 25]. In this way, we were able to rule out the influence of single-event upsets (SEUs) in the sequential elements and the incorrect data latching caused by SETs on the data signals. In the heavy ion irradiation experiments, the test approach proposed in [22] was adopted to rule out the influence of the SEUs in the sequential elements and the incorrect data latching caused by SETs on the data signals.

4 Results and discussion

4.1 Simulation results of the single sequential element

The simulations were performed on the DFF and D-latch with 130-nm CMOS technology. As shown in Fig. 3a, b, in each simulation, an SET was injected at the output of one clock inverter in one copy. The injection time of the SETs was random in the range less than 1000 ps. This range was set by referring to the work in [26]. In each simulation, the appearance of the pulse at the signal XOR_Q_DFF (XOR_Q_Latch) and its effective pulse width were recorded. We can obtain the duration of incorrect data latching according to the effective pulse width. Two thousand simulations (1000 P-hit simulations and 1000 N-hit simulations) were performed, respectively, on the DFF and D-latch.

The total number of CDN-SET-induced incorrect data latching for DFF and D-latch is shown in Fig. 6. As shown in the figure, in the 2000 simulations, the CDN-SET-induced incorrect data latching occurred 246 times in the active-low D-latch. However, the total number of CDN-SET-induced incorrect latching in DFF reached up to 698. This means that compared with D-latch, DFF is more sensitive to SETs on the clock signal, especially in the P-hit instance. This was mainly because of a 0-to-1 upset that occurred on the clock signal in the P-hit instance, which is opaque for the active-low D-latch when the clock is high. Unless the P-hit-induced SET happens to occur at or near the falling edge of the clock signal, which will cause the falling edge to lag behind its expected falling transition time, and the data input of the D-Latch is different from its stored state, the P-hit-induced SET will cause the time to start latching slightly behind the expected time in the D-Latch.

In the N-hit instance, when radiation-induced clock race occurs or radiation-induced clock jitter causes the falling transition time of the clock signal to be earlier than the expected time, and the data input of the D-Latch is different from its stored state, an incorrect latching will occur in D-Latch. However, when an incorrect data latching occurred in D-latch, an incorrect latching also usually

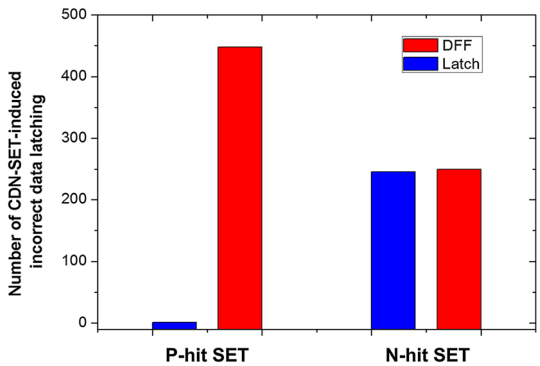

Fig. 6 (Color online) Total number of incorrect data latching in the simulations for the DFF and D-latch

occurred in DFF simultaneously, and duration of the CDN-SET-induced incorrect latching in DFF was usually much longer than that in D-latch, as listed in Table 2. This is consistent with the analysis in Sect. 2. The duration of the CDN-SET-induced incorrect latching in D-latch is usually less than that in DFF. Moreover, a shorter incorrect latching is less likely to cause incorrect latching in the receiving sequential elements. Therefore, the CDN-SET-induced incorrect latching detected in the receiving sequential elements behind a D-latch will be smaller than that detected in the receiving sequential elements behind a DFF.

4.2 Comparative study results of the case circuit

Two designs of a case circuit were implemented with the 65-nm bulk CMOS technology. Function verification of the two designs was made before the simulations to ensure correct operation of the designs. As mentioned above, the case circuit worked in real time in the simulations. Six sets of traversal simulations were performed on each design. This can make the simulation results more statistical and convictive. In each set of simulations, the SET injection location traversed the 97 clock nodes on the CDN of the case circuit. The pulse width and injection time of the SET were random. The random pulse width of the injected SET was less than 500 ps, which was entirely set by referring to the previous work [27] of our group.

Figure 7 shows the number of incorrect data latching in each sequential element caused by SETs on the CDN in the 1164 $(2 * (97 \times 6))$ simulations. The DFFs and D-latches in which incorrect data latching did not occur are not shown. As shown in the figure, in the 1164 simulations, the CDN-SET-induced incorrect latching occurred 168 times in the DFF-based design and 37 times in the optimized design.

As described in Sect. 4.1, the duration of the CDN-SET-induced incorrect latching in D-latch is usually much less than that in DFF, and a shorter incorrect latching is less likely to cause incorrect latching in the receiving sequential elements. Thus, compared with the simulation results of the single sequential element in Sect. 4.1, the CDN-SET-induced incorrect latching detected in the sequential elements in the optimized design was smaller than that detected in the DFF-based design. These results also showed that SETs on the CDN were more likely to cause incorrect data latching in the DFF-based design than in the optimized design. That is to say, the DFF-based design is more sensitive to SETs on the CDN than the optimized design.

4.3 Heavy ion irradiation experiment results

Heavy ion broad-beam experiments were performed on the test chip described in Sect. 3.3. The layout and die micrograph of the test chip are shown in Fig. 8. The cross sections of each test chain were measured in three test

Table 2 Durations of incorrect data latching in both sequential elements due to N-hit SET on the clock signal

Duration of CDN-SET-induced incorrect data latching in D-latch (ns)	Duration of CDN-SET-induced incorrect data latching in DFF (ns)
49.05	248.1
11.06	210.7
9.118	208.3
52.07	251.4
99.04	298.4
30.13	229.1
59.08	258.4
63.08	262.4
2.127	201.9
13.06	212.6
18.06	217.7
21.12	220.2
51.15	250.5
16.05	215.1
56.04	255.6
88.13	287.7
4.042	203.2
12.14	211.8
67.12	266.3
70.16	270.0

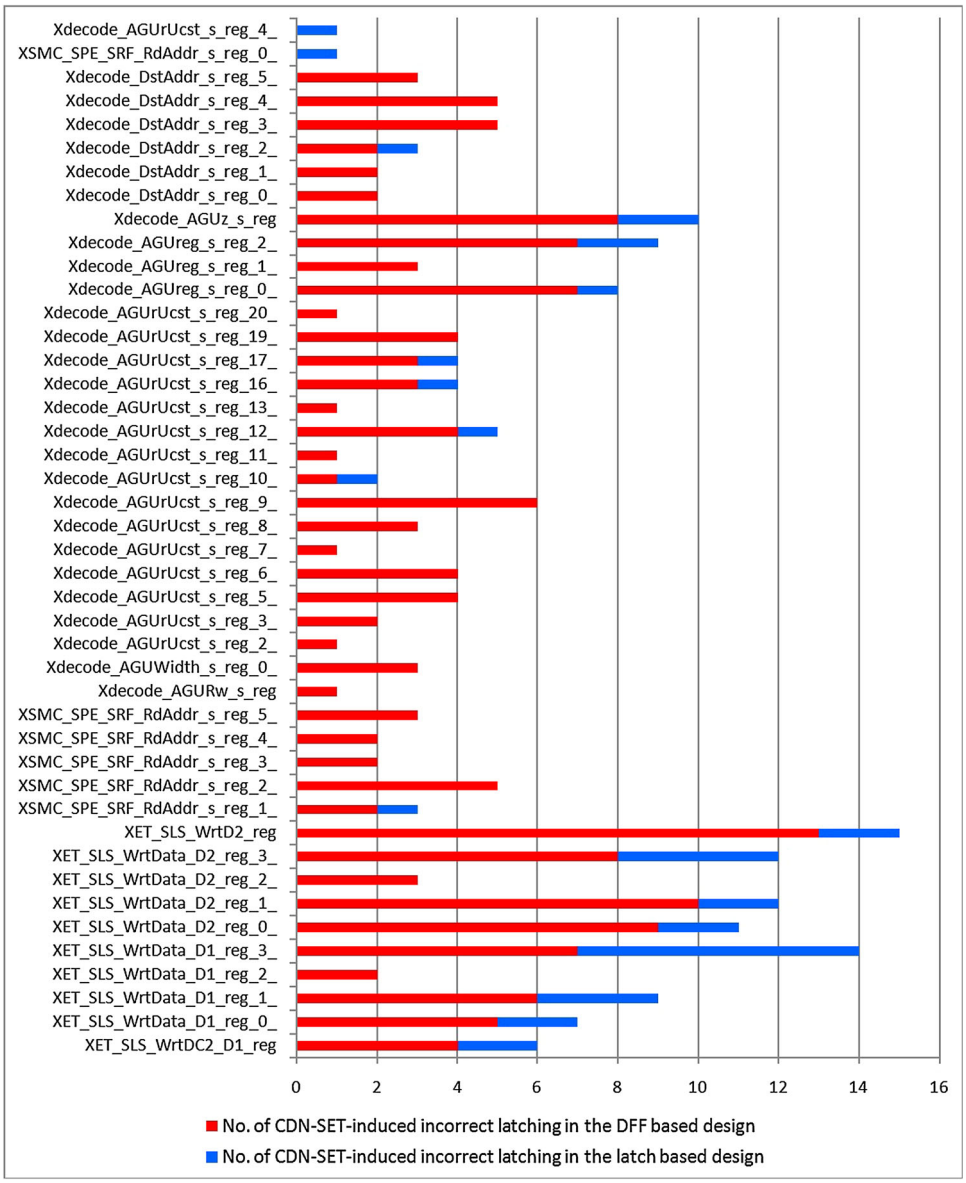

Fig. 7 (Color online) Number of CDN-SET-induced incorrect data latching in the DFF-based design and optimized design

modes for the ions of bismuth (Bi), germanium (Ge), and chlorine (Cl) at normal incidence. The heavy ion experiment for Bi was performed at the Heavy Ion Research Facility in Lanzhou (HIRFL), China, and the experiments for Ge and Cl were performed at the HI-13 Tandem Accelerator in China Institute of Atomic Energy in Beijing.

It may be recalled from Sect. 3.3 that all the sequential elements and their data inputs in the four test chains were hardened by design to rule out the influence of SEUs that may occur in the sequential elements and incorrect data latching caused by SETs on the data signals. To fully eliminate this influence, we considered the test modes 00 and 11 in which the data patterns were a constant value of 0 and 1, respectively. Because the data pattern is static in these two test modes, the SETs on the CDN will not induce incorrect data latching of the sequential elements. Because there was no SET target in chains 5 and 7, all upsets detected in the test modes 00 and 11 were SEUs initiated in the sequential elements. For test chains 1 and 3, which had SET targets, the total cross sections detected in the test modes 00 and 11 gave us the cross sections for the SET targets and sequential elements together without the influence of the CDN. We could obtain the contribution of the SET targets alone by subtracting the DFF (D-latch) cross section component measured in chain 7 (5) from the total cross sections of chain 3 (1). In the test mode 01, a "010101" pattern was clocked into the devices. For test chains 1 and 3, the total cross sections measured were the sum of the sequential element, clock, and SET target components. For test chains 5 and 7, the total cross sections measured were the sum of the sequential element and the clock components. By subtracting the sequential element

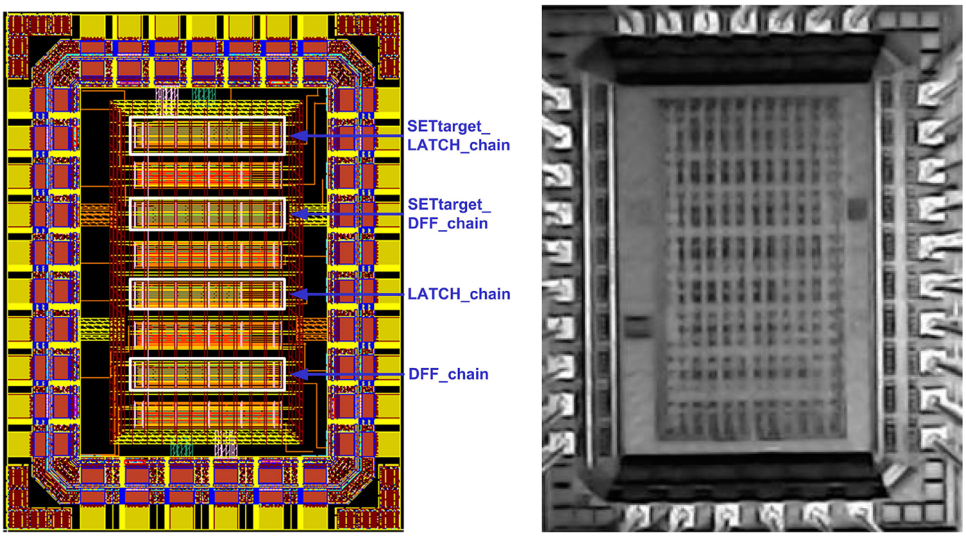

Fig. 8 **a** (Color online) Layout and **b** die micrograph of the test chip

and SET target components, we could obtain the upsets caused by SETs on the CDN.

Cross sections of the four test chains experimentally measured are shown in Fig. 9. The data were collected using Bi with LET of 99.8 MeV-cm^2/mg, Ge with LET of 37.6 MeV-cm^2/mg, and Cl with LET of 15.2 MeV-cm^2/mg. In the experiments for Ge and Cl, the total fluence of the beams used in the experiments was 1×10^7 ions/cm^2. In the experiment for Bi, the fluence was 5×10^6 ions/cm^2 due to test time constraint. As shown in the figure, in the test modes 00 and 11, the cross sections of all the four test chains were 0. This was mainly because all sequential elements and all their data inputs were hardened by design. This meant that, in our experiments, the SET targets and sequential elements had no contribution to the cross sections and the cross sections measured in the test mode 01 were the contribution of the CDN.

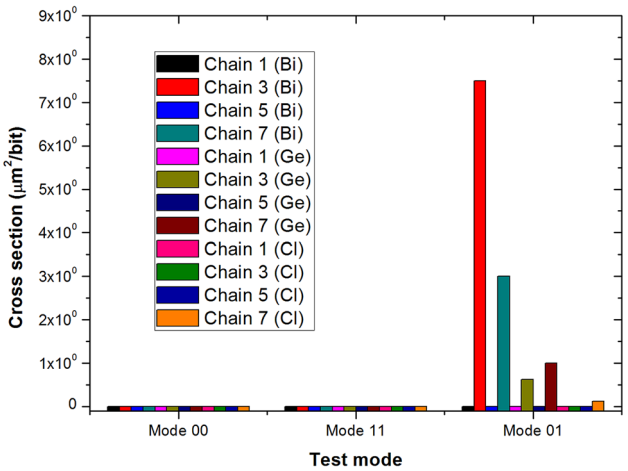

Fig. 9 (Color online) Cross sections for the four test chains experimentally measured at normal incidence. In test modes 00 and 11, the data pattern was a constant value of 0 and 1, respectively. In test mode 01, a "010101" pattern was clocked into the devices

As mentioned in Sect. 4.1, D-latch is much less sensitive to P-hit-induced SET on the clock signal. Moreover, a previous study revealed that the effective sensitive area of PMOS is much larger than that of NMOS [28], and thus 0-to-1 upsets are more likely to occur than 1-to-0 upsets [29]. Therefore, the CDN-SET-induced incorrect latching in D-latch-based chains detected in the heavy ion experiments was further reduced. According to the experimental results in test mode 01, the SEU cross sections induced by SETs on the CDN in the experiments for Bi were 7.5 μm^2/bit and 3 μm^2/bit in test chain 3 (SETtarget_DFF_chain) and test chain 7 (DFF_chain), respectively. In addition, these two cross sections, respectively, were 0.625 μm^2/bit and 1 μm^2/bit in the experiments for Ge. However, no upset was detected in the D-latch-based test chains (chains 1 and 5); i.e., the SEU cross sections induced by SETs on the CDN were 0 in the D-latch-based test chains. This means that compared with the D-latch-based test chains, the DFF-based chains were much more sensitive to SETs on the CDN. The same conclusion can be drawn from the experimental results for Cl, although the cross section measured was small due to low LET of Cl. This further verifies that compared with the D-latch-based design, the DFF-based design is more sensitive to SETs on the CDN.

5 Conclusion

The trigger modes of sequential logic elements vary with their element types. Therefore, whether an SET on the CDN will induce incorrect data latching of the sequential element and how long the incorrect latching will last vary with the sequential element type. Therefore, the type of the sequential element has a great influence on the SET susceptibility of the CDN.

In this paper, we comparatively studied the influence of the most commonly used sequential elements in modern synchronous digital systems, namely DFF and D-latch, on the SET susceptibility of the CDN. Firstly, we compared the influence of a random SET on the clock signal of an individual DFF and D-latch by 1000×2 simulations. Secondly, we comparatively studied the incorrect data latching caused by SETs on the CDN in the DFF-based design and optimized the design in which some FFs were replaced by D-latches, both of which worked in real time. In the 1164 simulations for this comparative study, every clock node on the CDN was traversed, the injection time of the SET was completely random, and the pulse width of the injected SET was random in a certain range. In this way, the simulation could more veritably reflect the influence of the radiation particle on the CDN of an IC in aerospace. Thirdly, we further studied the influence of DFF and D-latch on the SET susceptibility of the CDN by heavy ion broad-beam experiments.

All electrical simulations and heavy ion irradiation experiment results show that the design with DFFs is much more sensitive to SETs on the CDN than the design with latches. That is to say, DFF has a stronger influence on the SET susceptibility of the CDN. The findings have significant implications for the design of highly reliable IC for harsh radiation environments.

As described in Sect. 1, many studies have shown that a latch is smaller, faster, and less power-consuming than a flip-flop. The research results in this paper show that in addition to the above advantages, the sensitivity of D-Latch to SETs on the CDN is also lower than that of DFFs. In addition, because the D-Latch itself has a small area, its total sensitive area [30, 31] will also be smaller and its sensitivity to radiation effect will be lower. The area, power, and performance overheads introduced by radiation hardening techniques will also be smaller.

In view of the advantages of D-Latch described above, IC designers can appropriately select DFFs and D-Latches while designing their circuits. For the completed DFF-based designs, designers can replace some of the DFFs with their corresponding D-latches by analyzing the function and timing behavior of each DFF in their designs. This can improve the circuit performance with regard to area, power consumption, and radiation resistance, which are key factors for a high-reliability IC operating in an extremely harsh radiation environment.

References

1. B.M. Gadlage, Comparison of heavy ion and proton induced combinatorial and sequential logic error rates in a deep submicron process. IEEE Trans. Nucl. Sci. **52**, 2120–2124 (2005). https://doi.org/10.1109/TNS.2005.860678
2. D.G. Mavis, P.H. Eaton, SEU and SET modeling and mitigation in deep submicron technologies. in *IEEE IRPS*, (Phoenix, AZ, June 2007), 293–305. https://doi.org/10.1109/RELPHY.2007.369907
3. N.N. Mahatme, S. Jagannathan, T.D. Loveless et al., Comparison of combinational and sequential error rates for a deep submicron process. IEEE Trans. Nucl. Sci. **58**, 2719–2725 (2011). https://doi.org/10.1109/TNS.2011.2171993
4. N.N. Mahatme, I. Chatterjee, B.L. Bhuva, et al., Analysis of soft error rates in combinational and sequential logic and implications of hardening for advanced technologies. in *IEEE IRPS*, (Anaheim, CA, May 2010), 1031–1035. https://doi.org/10.1109/IRPS.2010.5488680
5. S. Chellappa, L.T. Clark, K.E. Holbert, A 90-nm radiation hardened clock spine. IEEE Trans. Nucl. Sci. **59**, 1020–1026 (2012). https://doi.org/10.1109/TNS.2012.2183647
6. R. Chipana, F.L. Kastensmidt, SET susceptibility analysis of clock tree and clock mesh topologies. in *IEEE ISVLSI*, Tampa, FL, 559–564 July 2014. https://doi.org/10.1109/ISVLSI.2014.33
7. N. Seifert, P. Shipley, M.D. Pant, et al., Radiation-induced clock jitter and race. in *IEEE IRPS*, (San Jose, CA, April 2005), 215–222. https://doi.org/10.1109/RELPHY.2005.1493087
8. A. Mallajosyula, P. Zarkesh-Ha, A robust single event upset hardened clock distribution network. in *IEEE IIRW*, S. Lake Tahoe, CA, 121–124 October 2008. https://doi.org/10.1109/IRWS.2008.4796101
9. R. Dash, R. Garg, S.P. Khatri, et al., SEU hardened clock regeneration circuits. in *IEEE ISQED*, (San Jose, CA, March 2009), 806–813. https://doi.org/10.1109/ISQED.2009.4810396
10. N. Weste, D.M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th edn. (Addison-Wesley Publishing Company, New York, 2010), p. 376
11. S. Heo, R. Krashinsky, K. Asanovic, Activity-sensitive flip-flop and latch selection for reduced energy. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **15**, 1060–1064 (2007). https://doi.org/10.1109/TVLSI.2007.902211
12. B.S. Kong, S.S. Kim, Y.H. Jun, Conditional-capture flip-flop for statistical power reduction. IEEE J. Solid-State Circuits. **36**, 1263–1271 (2001). https://doi.org/10.1109/4.938376
13. S. Dinesh, C. Ananth, Area power and speed optimized serial type daisy chain memory using modified CPG with SSASPL. in *ICCICCT*, (Kumaracoil, India, December 2015), 344–349. https://doi.org/10.1109/ICCICCT.2015.7475302
14. B.D. Yang, Low-power and area-efficient shift register using pulsed latches. IEEE Trans. Circuits Syst. I, Reg. Papers. **62**, 1564–1571 (2015). https://doi.org/10.1109/TCSI.2015.2418837
15. T.Y. Wu, Y.L. Lin, Storage optimization by replacing some flip-flops with latches. in *EURO-DAC*, (Geneva, Switzerland, September 1996), 296–301. https://doi.org/10.1109/EURDAC.1996.558220

16. T. Dua, K.G. Sharma, T. Sharma, An efficient novel latch design for sequential applications. in *ICRAIE*, Jaipur, India, 1–4 May 2014. https://doi.org/10.1109/ICRAIE.2014.6909109
17. P.P. Hao, S.M. Chen, Single-event transient susceptibility analysis and evaluation methodology for clock distribution network in the integrated circuit working in real time. IEEE Trans. Device Mater. Rel. **17**, 539–548 (2017). https://doi.org/10.1109/TDMR.2017.2733218
18. Q. Zhou, K. Mohanram, Gate sizing to radiation harden combinational logic. IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **25**, 155–166 (2006). https://doi.org/10.1109/TCAD.2005.853696
19. A. Dharchoudhury, S.M. Kang, H. Cha, et al., Fast timing simulation of transient fault in digital circuits. in *IEEE/ACM ICAD*, (San Jose, CA, November 1994), 719–726. https://doi.org/10.1109/ICCAD.1994.629902
20. A.B. Dolores, H.R. William, Z.W. Ian et al., Modeling of single event transients with dual double-exponential current source: implications for logic cell characterization. IEEE Trans. Nucl. Sci. **62**, 1540–1549 (2015). https://doi.org/10.1109/TNS.2015.2449073
21. P.P. Hao, S.M. Chen, Z.Y. Wu et al., On-chip relative single-event transient/single-event upset susceptibility test circuit for integrated circuits working in real time. IEEE Trans. Nucl. Sci. **65**, 376–381 (2018). https://doi.org/10.1109/TNS.2017.2784569
22. D.L. Hansen, E.J. Miller, A. Kleinosowski et al., Clock, flip-flop, and combinatorial logic contributions to the SEU cross section in 90 nm ASIC technology. IEEE Trans. Nucl. Sci. **56**, 3542–3550 (2009). https://doi.org/10.1109/TNS.2009.2031972
23. T. Calin, R. Velazco, M. Nicolaidis, et al., Topology-related upset mechanisms in design hardened storage cells. in *IEEE RADECS*, (Cannes, France, September 1997), 484–488. https://doi.org/10.1109/RADECS.1997.698979
24. D.G. Mavis, P.H. Eaton, Soft error rate mitigation techniques for modern microcircuits. in *IEEE IRPS*, (Dallas, TX, April. 2002), 216–225. https://doi.org/10.1109/RELPHY.2002.996639
25. J.E. Knudsen, L.T. Clark, An area and power efficient radiation hardened by design flip-flop. IEEE Trans. Nucl. Sci. **53**, 3392–3399 (2006). https://doi.org/10.1109/TNS.2006.886199
26. B. Narasimham, B.L. Bhuva, R.D. Schrimpf et al., Characterization of digital single event transient pulse-widths in 130-nm and 90-nm CMOS technologies. IEEE Trans. Nucl. Sci. **54**, 2506–2511 (2007). https://doi.org/10.1109/TNS.2007.910125
27. P.C. Huang, S.M. Chen, J.J. Chen et al., A novel uniform vertical inverter chains (UniVIC) SEMT test structure for heavy-ion-induced charge sharing measurement. IEEE Trans. Nucl. Sci. **62**, 3330–3338 (2015). https://doi.org/10.1109/TNS.2015.2486774
28. S.M. Chen, Y.K. Du, B.W. Liu et al., Calculating the soft error vulnerabilities of combinational circuits by re-considering the sensitive area. IEEE Trans. Nucl. Sci. **61**, 646–653 (2014). https://doi.org/10.1109/TNS.2014.2298889
29. C.H. Chen, P. Knag, Z.Y. Zhang, Characterization of heavy-ion-induced single-event effects in 65 nm bulk CMOS ASIC test chip. IEEE Trans. Nucl. Sci. **61**, 2694–2701 (2014). https://doi.org/10.1109/TNS.2014.2342872
30. T.D. Loveless, J.S. Kauppila, S. Jagannathan et al., On-chip measurement of single-event transients in a 45 nm silicon-on-insulator technology. IEEE Trans. Nucl. Sci. **59**, 2748–2755 (2012). https://doi.org/10.1109/TNS.2012.2218257
31. J.S. Kauppila, T.D. Haeffner, D.R. Ball et al., Circuit-level layout-aware single-event sensitive-area analysis of 40-nm bulk CMOS flip-flops using compact modeling. IEEE Trans. Nucl. Sci. **58**, 2680–2686 (2011). https://doi.org/10.1109/TNS.2011.2172692