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Design of a 20-Gsps 12-bit time-interleaved analog-to-digital conversion system

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Abstract The time-interleaved analog-to-digital conversion (TIADC) technique is an effective method for increasing the sampling rate in a waveform digitization system. In this study, a 20-Gsps TIADC system was designed. A wide-bandwidth performance was achieved by optimizing the analog circuits, and a sufficient effective number of bits (ENOB) performance guaranteed using the perfect reconstruction algorithm for mismatch error correction. The proposed system was verified by tests, and the results indicated that a − 3 dB bandwidth of 6 GHz and the ENOB performance of 8.7 bits at 1 GHz and 7.6 bits at 6 GHz were successfully achieved.

Keywords Time-interleaved technique · High-speed A/D conversion · High bandwidth · Mismatch error correction

1 Introduction

Waveform digitization is a significant technique, especially when high-speed signals are involved in physics experiments, such as SiPM detectors [1], and many circuits for waveform digitization are developed [2–4]. In the traditional signal measurement method, the readout electronics are usually based on amplification and shaping circuits [5, 6], and some other techniques are also involved, such as the charge-to-time conversion [7]. Comparing with the traditional method, the input signal is directly sampled in a waveform digitization system. The original signal waveform is reconstructed by a series of sampling points, by which further details regarding charge and time can be obtained by analyzing it. Moreover, there is no baseline pile-up in a waveform digitization system, and the dead time is significantly shorter than that of the traditional method. Owing to these advantages, waveform digitization has recently become a popular research topic. In a high-speed waveform digitization system, the sampling rate is one of the most important characteristics, which directly determines how detailed the input waveform can be depicted on the time axis. The TIADC technique is an effective method for increasing the sampling rate. In a TIADC system, multiple analog-to-digital converters (ADCs) are employed. Assuming the number of ADCs is denoted as M, all having a sampling rate of F_s while the sampling clock phase of each is shifted by a step size of $2\pi F_s/M$, an equivalent sampling rate of $M \times F_s$ can be achieved by interleaving the entire sampling data.

Because there is more than one ADC in a TIADC system, the mismatch error introduced by different ADCs will inevitably deteriorate system performance. Several correction methods have been studied and developed to

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neutralize the influence of the mismatch error, and both foreground methods [8–10] and background methods [11–13] are involved. The perfect reconstruction correction algorithm is an effective foreground correction method, where the finite impulse response (FIR) filters are used to correct the ADC sampling data. In addition, an improved perfect reconstruction correction algorithm was developed, where a broadband correction is achieved using only one group of filter coefficients [10]. This method is especially suitable for error correction of the pulse waveform measurement owing to the broad range of the frequency spectrum.

In recent years, several high-speed TIADC systems have been developed [10, 14]. In addition to the requirement of a high sampling rate, many other features are required for a high performance of a TIADC system; a few of the key parameters are susceptible to the analog circuits used in the TIADC design. For instance, the bandwidth performance is an important parameter that not only refers to the ADC but is also susceptible to the analog buffers, as well as the signal transmission line. Thus, the analog transmission circuit is critical for the system. Moreover, the sampling clock circuit should also be precisely designed owing to the aperture jitter directly influencing the signal-to-noise ratio (SNR) performance, especially in the high-frequency range. Therefore, the analog circuit design is significant for developing a TIADC system with high-speed performance.

In this study, a 20-Gsps 12-bit TIADC system is designed, which mainly focuses on the analog signal transmission and clock generation circuits. Simulations were conducted on these circuits to guarantee their high performance. The sampled data were received by an FPGA and transferred to a PC for further analysis. The system performance was tested, and the results indicated that the − 3 dB bandwidth was up to 6 GHz, and an ENOB performance of 7.6 bits at 6 GHz was achieved after performing the perfect reconstruction correction.

The remainder of this paper is organized as follows. The proposed design regarding the hardware circuit of a 20-Gsps TIADC system is introduced in Sect. 2, which is followed by the presentation of the error correction algorithm in Sect. 3. The test results are provided and discussed in Sect. 4. Finally, the conclusions are summarized in Sect. 5.

2 20-Gsps TIADC system design

The structure of the proposed 20-Gsps TIADC system is shown in Fig. 1a, which employs two 10-Gsps 12-bit ADCs for interleaved sampling. There are four sub-ADC banks in each ADC, and thus, the entire system can be regarded as an eight-channel 2.5-Gsps TIADC system. Because ADCs function in a dual-edge sampling mode, the sampling clock of each ADC is required to be 5 GHz for a 10-Gsps sampling, which indicates that the sampling clock period is 200 ps; both the rising edge and falling edge are used for sampling. For an equivalent 20-Gsps sampling, the time skew between the two 5-GHz sampling clocks should be 50 ps. In this case, there are four clock edges in total, which are spread in an equal time interleave of 50 ps. Hence, the phase skew between the two sampling clocks originating from the clock generating circuit should be 90°.

The proposed system can be divided into the following three parts: (1) an analog signal circuit, responsible for transmitting a high-speed input signal to the ADC; (2) a clock generation circuit, responsible for generating a high-performance sampling clock for ADCs and other clocks for data interface and digital circuits; and (3) a digital circuit, responsible for high-speed data receiving, buffering, and uploading to a PC, and is mostly implemented through a field-programmable gate array (FPGA).

2.1 High-bandwidth analog signal transmission circuit

The structure of the analog signal transmission circuit is shown in Fig. 1b. The input signal is split into two channels by a power splitter, and a transformer is employed for each channel to convert a single-ended signal to a differential signal to meet the input requirement of the ADC. The analog signal transmission circuit plays a significant role in the determination of system bandwidth and signal imbalance, which is a critical source of mismatch error. Therefore, the power splitter and transformer should be carefully chosen.

The most concerned parameters of a power splitter include the bandwidth, insertion loss, amplitude imbalance, and return loss. Generally, power splitters can be divided into the following two types: Wilkinson and resistive. The Wilkinson power splitter achieves the lowest insertion loss by splitting the input signal power into multi-channel outputs, thus providing an ideal − 3 dB output for a 1:2 Wilkinson power splitter. However, a high-performance Wilkinson power splitter, having both a wide frequency range down to DC frequencies and a low-amplitude imbalance, has a complex circuit structure and is used as a block module rather than a surface mount device, which is not suitable for integrated systems. In contrast, a resistive power splitter splits the input signal based on the signal amplitude. It usually has a simple circuit structure and can be easily integrated into a surface mount device. It simultaneously provides a broadband response down to the DC range and a low-amplitude imbalance. The main drawback of the resistive power splitter is that the ideal insertion loss

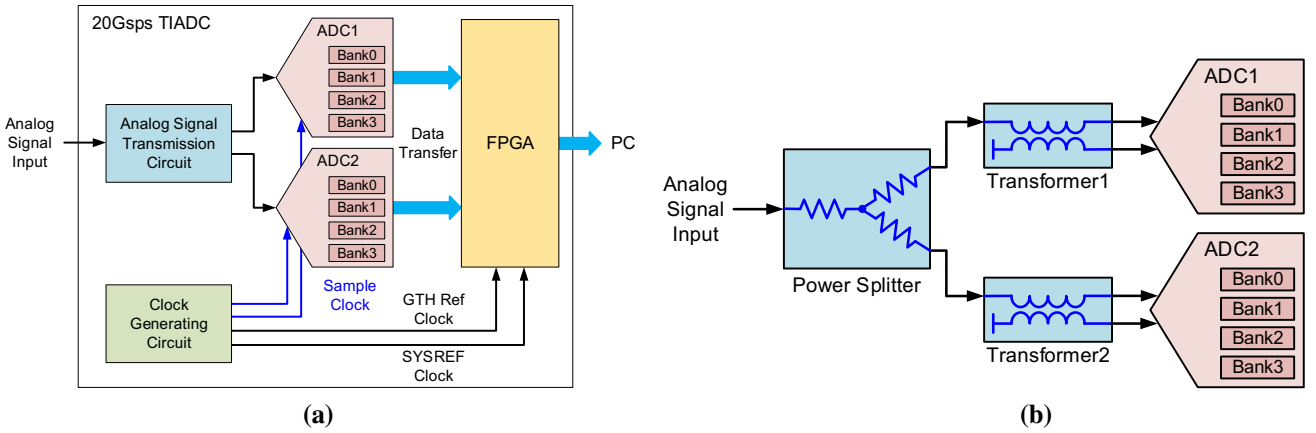


Fig. 1 **a** Structure of the proposed 20-Gsps 12-bit TIADC system. **b** Structure of an analog signal transmission circuit

is − 6 dB, which is larger than that of the Wilkinson power splitter.

Based on these characteristics, the type of power splitter chosen should be thoroughly considered. Several parameters of a few typical surface mount power splitters are listed in Table 1, where column "Type" R and W indicate a resistive and Wilkinson power splitter, respectively; the corresponding S-parameters of the insertion and return losses are shown in Fig. 2a and b, respectively.

Owing to the requirement for a wide frequency range for a pulse waveform measurement, the bandwidth range of an analog device should not only encompass the DC frequencies but also a certain part of the high-frequency band. A lower insertion loss can ensure a larger dynamic range of the measurement, which should not be too large. Moreover, the return loss can cause a harmonic distortion of the waveform; therefore, it should be minimized. The amplitude imbalance of a power splitter is the main source of the gain error between the two ADC channels, and a large gain error can decrease the efficiency of the mismatch error correction. Considering the aforementioned, the PD-0030SM was selected for use as the front-end power splitter in this study.

A transformer is employed to transform a single-ended signal into a differential signal. Owing to the existence of an internal differential 100-Ω termination resistor between the ADC input pins, and considering the fact that the characteristic impedances of the power splitter and transmission line are equal to 50 Ω, a transformer with a resistor ratio of 1:2 is required for impedance matching. The BAL-0009SMG was chosen to be used as the coupling transformer owing to its wide bandwidth ranging from 0.5 kHz to 9 GHz. The key parameters are listed in Table 2.

Considering the transmission requirement of high-frequency signals up to the frequency of the GHz-order, the dielectric of a printed circuit board (PCB) and the trace of a transmission line can significantly influence the signal quality. In this system, Megtron 6 is used as the PCB dielectric, which can support the transmission of signals with a frequency of up to 25 GHz. The transmission lines are designed to have the same lengths, and similar corner shapes for the two channels to meet the requirement for signal consistency.

The *S*-parameters of the transmission line sections are extracted using the ANSYS software. A simulation setup of the proposed analog signal transmission circuit was constructed, as illustrated in Fig. 3a. In the proposed system, there is a short transmission line from the input SMA connector to the power splitter, and the transmission lines from the power splitter to the two transformers are the same. Finally, there is a differential transmission line from each transformer to each ADC. The simulation result of the insertion loss is shown in Fig. 3b, where the dashed lines refer to the insertion loss without considering the transmission lines, and the solid lines refer to the transmission lines. At low frequencies, the insertion loss is not significantly influenced by the transmission lines. However, at high frequencies, the transmission lines introduce a non-

Table 1 Parameters of several typical power splitters

Model	Type	Bandwidth	Insertion loss (dB)	Amplitude unbalance (dB)
PD-0030SM	R	DC–30 GHz	∼ − 6	0.25
SCRP-2-682W+	R	DC–6.8 GHz	∼ − 9.6	0.3
MPD-0226SM	W	2 GHz–26.5 GHz	∼ − 4	0.2
RPS-2-30+	W	10 MHz–3 GHz	∼ − 3.6	0.6

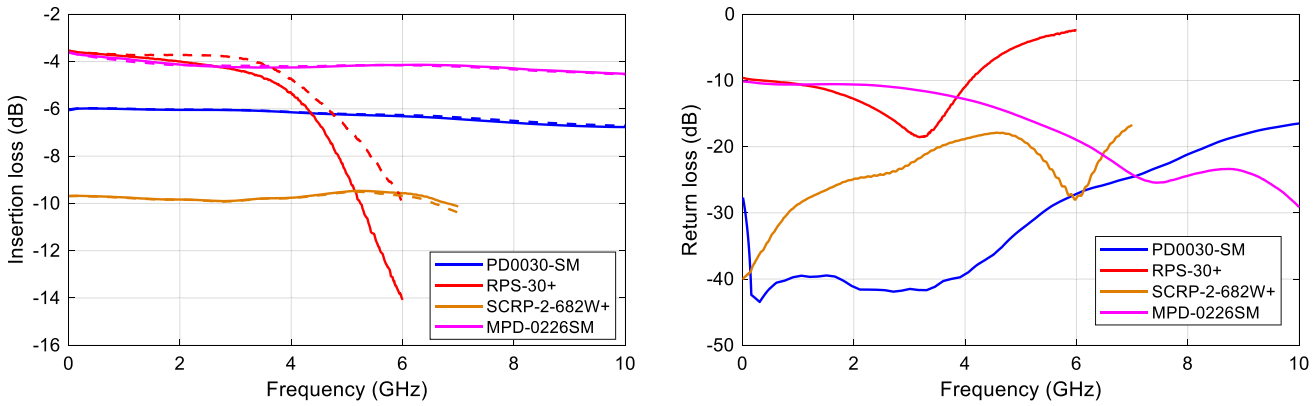


Fig. 2 (Color online) **a** Insertion losses of a few typical power splitters. **b** Return losses of a few typical power splitters

Table 2 Transformer parameters

Model	Bandwidth	Insertion loss for single output	Amplitude unbalance
BAL-0009SMG	0.5 kHz–9 GHz	− 7.5 dB	± 0.6 dB

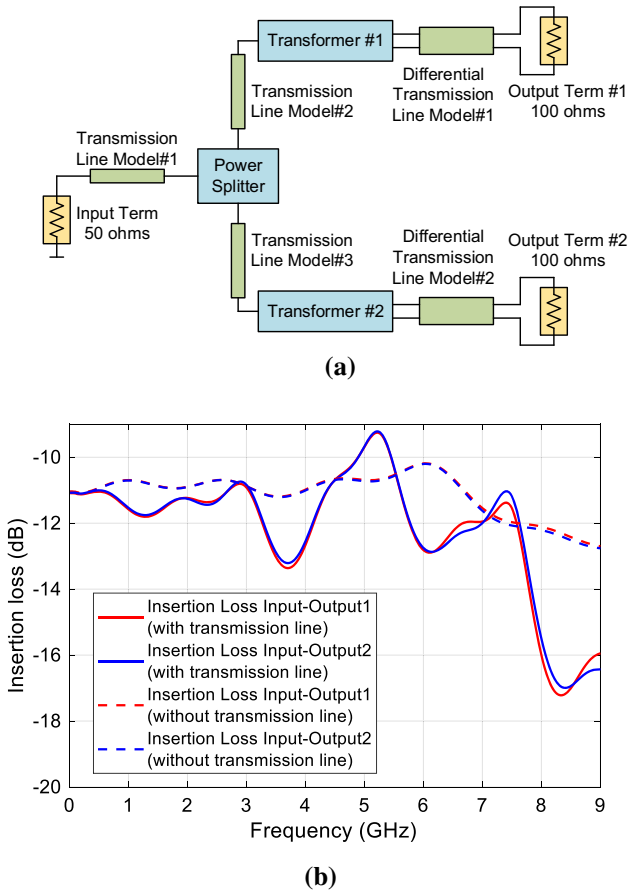


Fig. 3 (Color online) **a** Simulation circuit of the analog signal transmission circuit. **b** Insertion loss of the analog signal transmission circuit

negligible insertion loss. According to the simulation results, the − 3 dB bandwidth of the analog signal transmission circuit is approximately 7.5 GHz.

2.2 High-performance clock generation circuit

In an ADC sampling system, the sampling clock jitter can deteriorate the SNR performance. In addition, the aperture jitter caused by the time uncertainty of the ADC conversion can contribute to the deterioration of the SNR performance. The total jitter results from the square root of the quadratic sum of the sampling clock jitter and the aperture jitter. The jitter leads to an uncertainty in the sampling position and is reflected in the form of an amplitude noise of sampling points. This can cause a deterioration of the SNR, which is given by the following:

$$\mathrm{SNR} = -20\log(2\pi f_{\mathrm{in}} t_{\mathrm{jitter}}), \quad (1)$$

where f_{in} denotes the input signal frequency, and t_{jitter} denotes the total jitter. To achieve an improved system bandwidth performance, a high-performance clock generation circuit is highly recommended. For instance, if a 7.6-bit ENOB is expected at a 6-GHz input signal, the maximum tolerable jitter is calculated to be approximately 112 fs.

The structure of the clock generation circuit is shown in Fig. 4a. A high-performance phase-locked loop (PLL) (LMX2852) is employed as a 5-GHz sampling clock generator, and an ultra-low phase noise oscillator is used to generate the reference clock for the PLL.

The sources of the phase noise mainly include the reference oscillator, PLL phase detector, voltage-controlled oscillator (VCO), and PLL output divider. The frequency

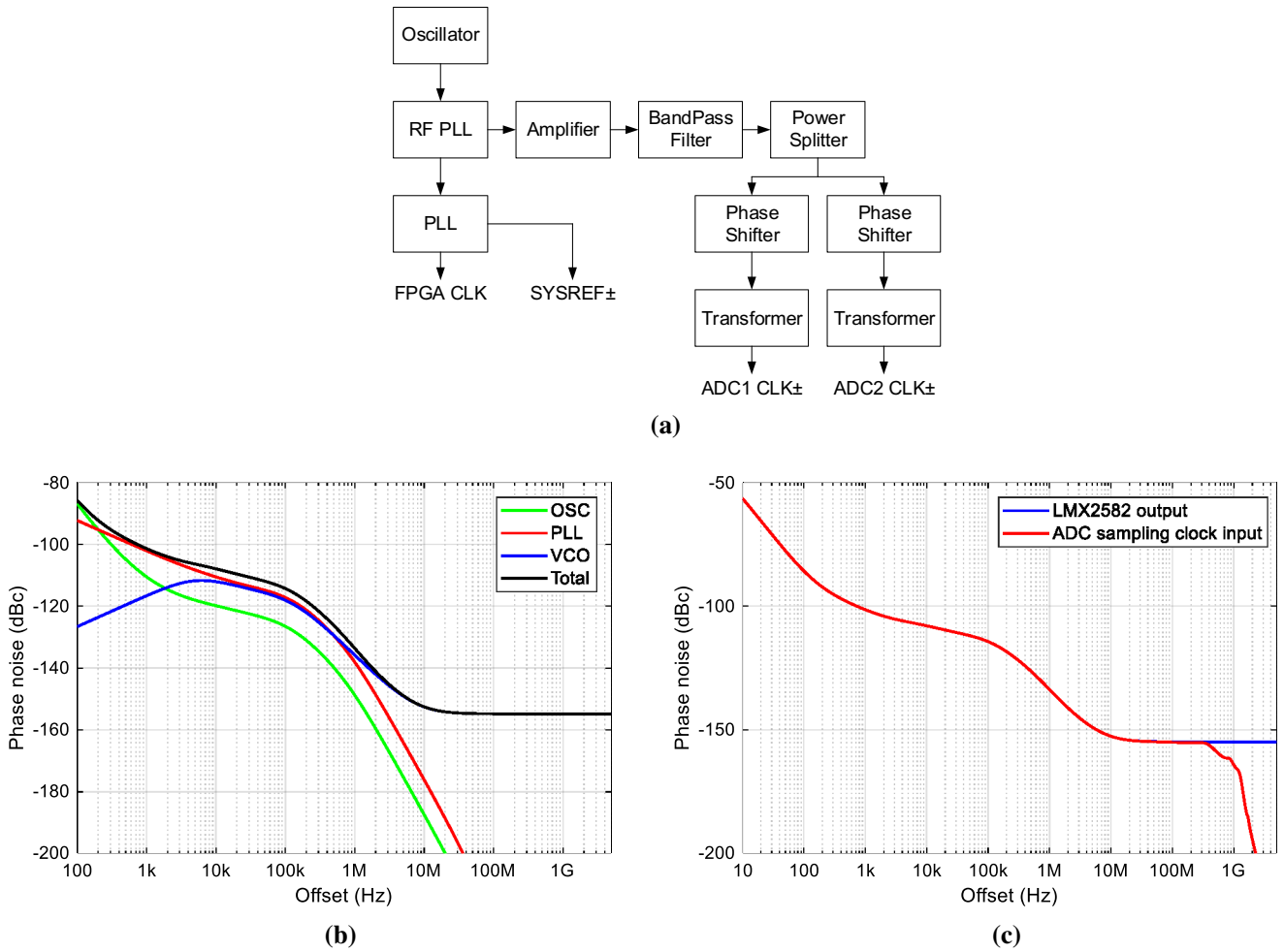


Fig. 4 (Color online) **a** Structure of the analog signal transmission circuit. **b** Simulation results of phase noise. **c** Phase noise simulation result of the ADC sampling clock

range of the VCO in LMX2582 is 3550–7100 MHz, which indicates that a 5-GHz sampling clock can be generated from the VCO directly while the PLL output divider is bypassed. Hence, the white noise of the PLL output divider can be avoided, which mainly aggravates the phase noise at frequency points distant from the center clock frequency. The simulation results of the phase noise of different parts of the PLL are shown in Fig. 4b. The phase noise of the OSC contributes the most at the near-end offset frequencies, while PLL and VCO contribute the same at the middle offset frequency range. At far-end offset frequencies, VCO is the only source of the phase noise.

The clock jitter can be calculated as follows:

$$t_{\text{jitter}} = \frac{\sqrt{2A}}{2\pi f_{\text{o}}}, \tag{2}$$

where A denotes the area of the integrated phase noise power and f_{o} denotes the output clock frequency of the PLL. The phase noise power integration region is set to be 0.1 kHz–5 GHz, and the output clock jitter has an estimated value of 81.47 fs.

Additional clock transmission circuits have been employed to ensure an improved performance for a larger margin of clock jitter. Band-pass filters (BPFs) are commonly used for noise filtering. The parameters of the two BPF types are listed in Table 3. The insertion losses in the stop-band of both BPFs are sufficiently high to achieve effective filtering. Furthermore, a narrow pass-band of 4900–5200 MHz can be achieved by cascading two BPFs after the PLL output, which eliminates the phase noise.

After the sampling clock is filtered, a power splitter splits the clock for two ADC channels, and a phase shifter of each clock path shifts the clock phase to adjust the phase difference between the two clocks to 90°. The phase shifter requires a small phase step size for the phase adjustment to ensure high precision because it directly affects the skew error, which should be minimal. Finally, a transformer with a resistor ratio of 1:2 couples the sampling clock from a single-ended to a differential pair. All the devices need to

Table 3 Parameters of two types of BPF

BPF type	Pass-band (MHz)	Insertion loss @ pass-band (dB)	Insertion loss @ stop-band (dB)
BFCN-4800+	4400–5200	~ 0.7	> 25
BPGE-542R+	4900–5920	~ 0.9	> 30

have a low insertion loss at 5 GHz. Meanwhile, an RF amplifier is inserted prior to the BPFs to compensate for the insertion loss of the BPFs and other devices to guarantee a sufficiently large clock amplitude at the ADC input end.

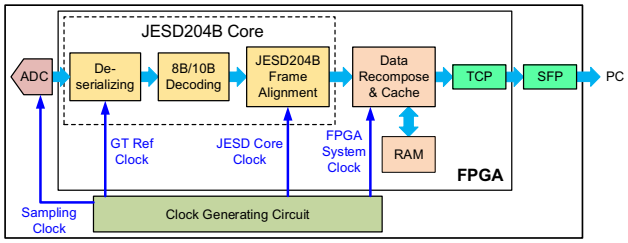
The phase noise simulation was conducted on the entire clock transmission circuit; the results are shown in Fig. 4c, which indicates that the phase noise of the sampling clock is effectively eliminated by the clock transmission circuit. In particular, when the offset frequency is greater than 300 MHz, the phase noise decreases sharply owing to the existence of the BPFs. Using Eq. (2), the expected jitter of the sampling clock at the ADC input end is calculated to be 60.71 fs. Note, the estimated jitter value does not consider aperture jitter, which is one of the internal characteristics of the ADC and cannot be directly obtained. The best SNR and ENOB performance achieved in the simulations without considering any other noise factors, such as aperture jitter, quantization error, and harmonic distortion, is shown in Table 4.

2.3 Data interface and digital circuit

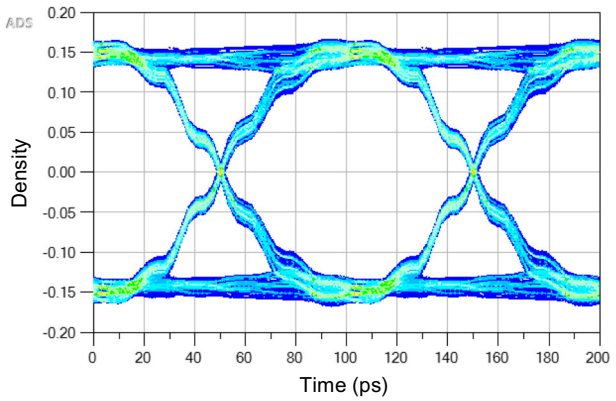
The block diagram of the digital circuit is shown in Fig. 5a. The digital circuit is responsible for data transformation, buffering, and uploading. The line rate of the original data of a single 10-Gsps, 12-bit ADC is up to 128 Gbps after an internal 60b/64b coding in the ADC. To achieve this high-speed data transformation, the JESD204B interface, which is a high-speed serial interface protocol, is employed for the data transformation from ADC to FPGA. Two JESD204B links are set for each ADC, and there are eight lanes per link. The line rate of each JESD204B lane was calculated to be 10 Gbps after the 8b/10b coding. An FPGA with greater than 32 Gigabit transceivers is responsible for receiving and deserializing the data. A system reference clock of 250 MHz is provided by the

Table 4 The best SNR and ENOB performances achieved in the clock simulation

f_{in}	SNR (dB)	ENOB (bits)
350 MHz	77.5	12.6
1 GHz	68.4	11.1
3 GHz	58.8	9.5
6 GHz	52.8	8.5



(a)



(b)

Fig. 5 (Color online) **a** Block diagram of a digital circuit. **b** Eye diagram simulation result of the 10-Gbps JESD204B lane

clock generation circuit for the JESD frame alignment. The FPGA is also responsible for data caching and transferring to the PC through the SFP using the TCP protocol.

To estimate the data transfer performance of the JESD204B lanes, the *S*-parameters of the PCB traces of the JESD lanes were extracted using the ANSYS software, and eye diagram simulations were conducted. The simulation result of one of the JESD lanes is shown in Fig. 5b, where the eye diagram is widely open, which indicates that the data interface can ensure effective data transfer at a line rate of 10 Gbps.

3 Perfect reconstruction correction of 20-Gsps TIADC system

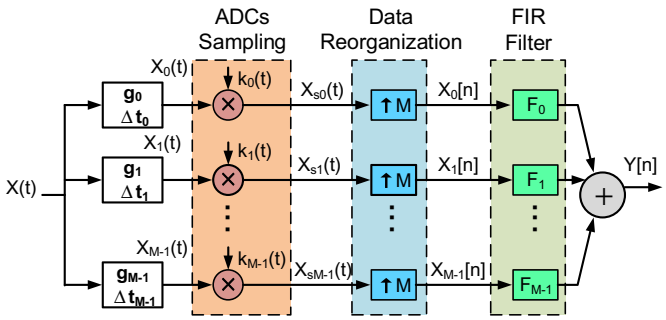
3.1 Perfect reconstruction correction algorithm

As previously indicated, TIADC systems suffer from mismatch errors, including the gain error, skew error, and offset error. In the proposed 20-Gsps TIADC system, a

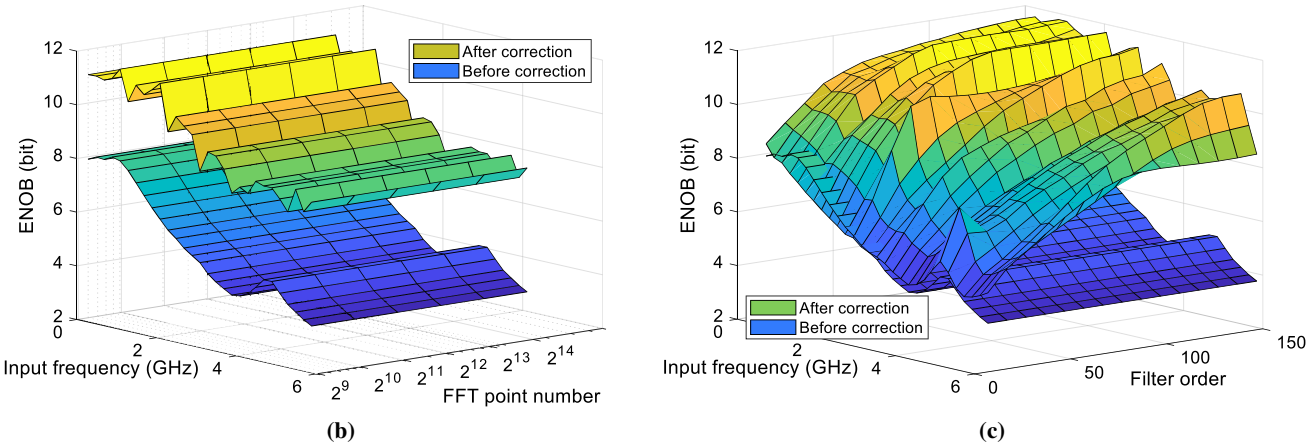
perfect reconstruction algorithm [10] was implemented in a wide range of the frequency band to mitigate the mismatch error and enhance system performance. The correction procedure of this algorithm is based on an FIR filter and can be achieved by either software or hardware modification. The block diagram of the system mismatch error and the corresponding correction process are presented in Fig. 6a. Each of the channels suffers from a certain group of mismatch error parameters; after sampling, the data of each channel are reorganized by an up-sampling of M-times, and an FIR filter is applied for each channel. Finally, the data array of the M channels are summed as a time-interleaved data array after correction.

Considering the correction process, if the input signal in the time domain is denoted as $x(t)$, the mismatch error can be expressed as follows:

1. The signal sampled at the ADC input end is denoted as $g_m x(t)$, where g_m denotes the gain error parameter of the mth channel. The expression of g_m in the frequency domain is denoted as $\widetilde{g}_m(\omega)$ and is obtained by the Fourier transform, which is correlated with the frequency. The gain error is mainly caused by the signal splitting circuit inconsistency and ADC inconsistency. For the zeroth channel, the gain error can be defined as $g_0 = 1$.
2. The ideal sampling time of the mth ($m = 0, 1\ldots M-1$) channel can be expressed as $nMT_s + mT_s$, where T_s denotes the sampling period of the TIADC system. For the convenience of derivation, a mT_s time advance for the mth channel input signal is considered while the sampling times of all the channels are aligned to nMT_s. Thus, the sampling function of the mth channel can be expressed as $k_m(t) = \sum_{n=-\infty}^{+\infty}\delta(t - nMT_s)$, and the ideal input signal after sampling can be expressed as $x_{s\_m\_ideal} = x(t + mT_s)$. In an actual circumstance, the sampled signal can be expressed as $x_{s\_m} = x(t + mT_s + \Delta t_m)$, where Δt_m denotes the skew mismatch parameter of the mth channel. The Fourier transform expression of Δt_m in the frequency domain can be denoted as $\Delta_{t_m}^{\sim}(\omega)$, which is also correlated with the signal frequency. For the zeroth channel, the skew mismatch parameter can be defined as $\Delta t_0 = 0$.
3. The offset stage added to the sampling signal for the mth ADC channel is defined as the offset error, and it changes the signal expression to $x(t) + \Delta o_m$, where



(a)



(b) (c)

Fig. 6 (Color online) **a** Mismatch error of sampling and its correction. **b** Correction performance dependence on the FFT point number. **c** Correction performance dependence on the filter order

Δo_m usually denotes a constant independent of the signal frequency.

When considering the three mismatch errors simultaneously, the sampling process of the mth ADC channel can be regarded as multiplying the sampling function $k_m(t) = \sum_{n=-\infty}^{+\infty}\delta(t - nMT_s)$ with the signal function $x_m(t) = g_m x(t + mT_s + \Delta t_m) + \Delta o_m$. Thus, the expression of the recomposed sampling array in the frequency domain can be expressed as follows:

$$X_s(j\omega) = \frac{1}{MT_s}\sum_{k=-\infty}^{+\infty}\sum_{m=0}^{M-1}\left[\widetilde{g_m}\left(\omega - k\frac{2\pi}{MT_s}\right)e^{j\left(\omega - k\frac{2\pi}{MT_s}\right)\left[mT_s + \widetilde{\Delta t_m}\left(\omega - k\frac{2\pi}{MT_s}\right)\right]}X\left(j\left(\omega - k\frac{2\pi}{MT_s}\right)\right)F_m(j\omega) + 2\pi\Delta o_m\delta\left(\omega - k\frac{2\pi}{MT_s}\right)\right]. \quad (3)$$

In an ideal TIADC system, where $g_m = 1$, $\Delta t_0 = 0$, and $\Delta o_m = 0$, $F_m(j\omega)$ equals e^{-jwmT_s}, which corresponds to the frequency response of an mT_s time delay for the mth channel, an ideal expression $X_{s\_ideal}(j\omega)$ can be derived as the correction target. In a non-ideal TIADC system, the offset error is usually corrected by measuring the offset of the noise waveform or by random chopping [15, 16]; therefore, this part of the error can be omitted during the derivation. Considering the other two types of mismatch errors, $F_m(j\omega)(m = 0, 1 \ldots M - 1)$ acts as an FIR filter for each ADC channel to obtain an ideal frequency domain expression $X_{s\_ideal}(j\omega)$ from $X_s(j\omega)$. Further details regarding this algorithm can be found in a previous study [10].

During the correction process, the gain error and skew error of each channel at the frequency calibrated by the sine fitting are calculated first. Then, a series of mismatch error parameters at all frequencies are obtained by interpolation, and the numerical expression of $F_m(j\omega)$ in the Nyquist zoom is calculated. Finally, an N-order FIR parameter in the time domain for each channel is calculated by the inverse fast Fourier transform (IFFT) and windowing, and thus, in total, $M \times N$ FIR filter parameters are obtained. The obtained parameters are used to generate an FIR filter, which is exerted on the sampling array to conduct the mismatch error correction.

3.2 Simulations

To evaluate the effectiveness of the mismatch error correction algorithm and determine suitable values of the key algorithm parameters, simulations of the 20-Gsps TIADC were conducted. There were four sub-ADC banks in a single ADC, and the mismatch errors between them could not be ignored. Thus, it was more effective to apply the correction process to eight interleaved channels of the proposed system, rather than only two separated ADCs.

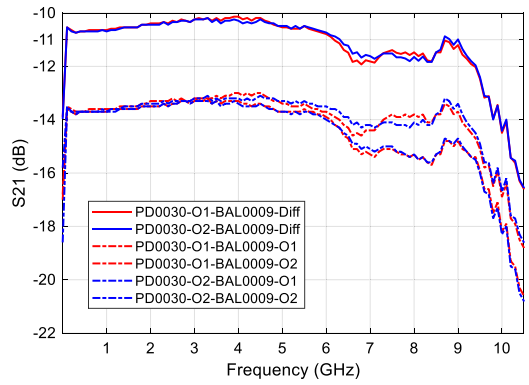
Fig. 7 (Color online) **a** The S_{21} parameter of the analog signal transmission circuit. **b** Bandwidth performance of the 20-Gsps TIADC system. **c** Frequency spectrum of the single ADC before correction. **d** Frequency spectrum of ADC1 and ADC2 before correction. **e** Frequency spectrum of the single ADC after correction. **f** Frequency spectrum of the ADC1 and ADC2 after correction. **g** The ENOB performance of the 20-Gsps TIADC system

According to the calibration results of the gain error and skew error, the simulations were conducted to study the key parameters of the algorithm. The first parameter studied was the FFT point number, which determined the intensity of the numerical expression of $F_m(j\omega)$. The correction performance for a different FFT point number is presented in Fig. 6b, where the FFT point number changed from 512 to 16,384. This shows that the correction effect was similar when the FFT point number was set within the indicated range.

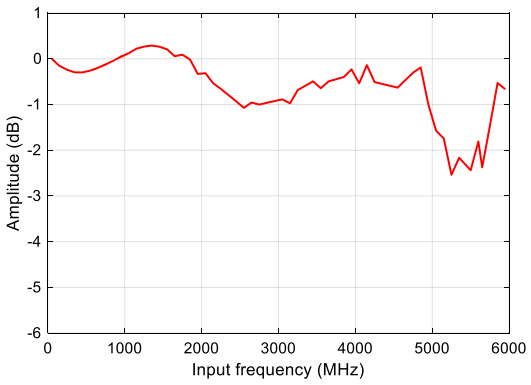
Next, the FIR filter order N was studied. Because the IFFT result is an infinite array and there must be a truncation when an FIR filter is used, the filter order is a significant parameter that determines the precision of the frequency response of the FIR filter relative to the frequency response of an ideal filter. Hence, it is directly correlated with the correction effect. The simulation results of the ENOB performance for different FIR filter orders are presented in Fig. 6c, where N is swept from 10 to 150. As presented in Fig. 6c, the correction effect was significantly sensitive to the filter order N. Particularly, the ENOB performance improved remarkably with the value of N when N was less than 100. Consequently, the simulation results indicate that the proposed correction algorithm is effective and provides an apparent improvement in the ENOB performance.

4 Test result

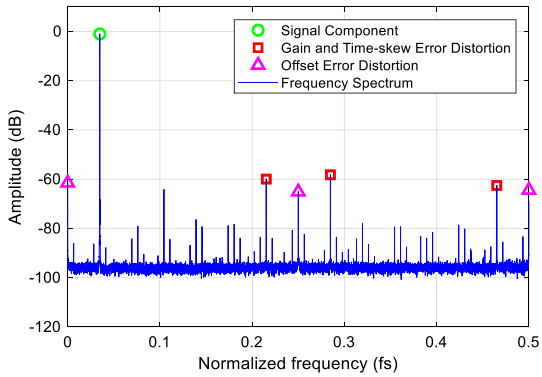
Tests were conducted to verify the system design performance. The results are summarized below.


S21 (dB)
Frequency (GHz)
PD0030-O1-BAL0009-Diff
PD0030-O2-BAL0009-Diff
PD0030-O1-BAL0009-O1
PD0030-O1-BAL0009-O2
PD0030-O2-BAL0009-O1
PD0030-O2-BAL0009-O2

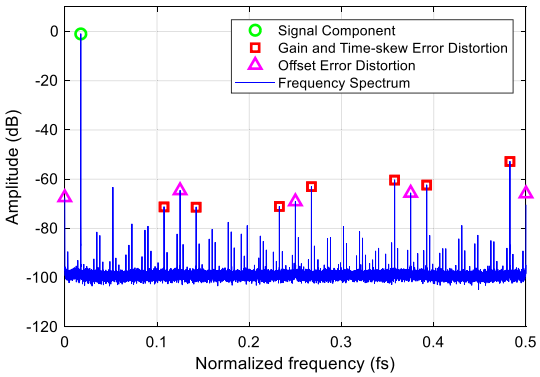
(a)


Amplitude (dB)
Input frequency (MHz)

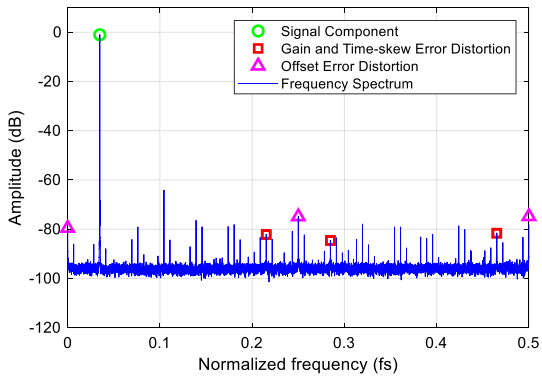
(b)


Signal Component
Gain and Time-skew Error Distortion
Offset Error Distortion
Frequency Spectrum
Amplitude (dB)
Normalized frequency (fs)

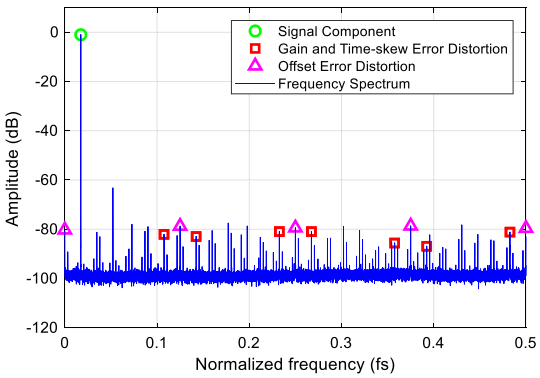
(c)


Signal Component
Gain and Time-skew Error Distortion
Offset Error Distortion
Frequency Spectrum
Amplitude (dB)
Normalized frequency (fs)

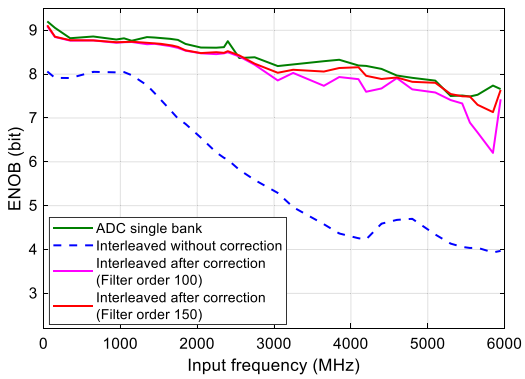
(d)


Signal Component
Gain and Time-skew Error Distortion
Offset Error Distortion
Frequency Spectrum
Amplitude (dB)
Normalized frequency (fs)

(e)


Signal Component
Gain and Time-skew Error Distortion
Offset Error Distortion
Frequency Spectrum
Amplitude (dB)
Normalized frequency (fs)

(f)


ENOB (bit)
Input frequency (MHz)
ADC single bank
Interleaved without correction
Interleaved after correction
(Filter order 100)
Interleaved after correction
(Filter order 150)

(g)

4.1 Analog signal transmission circuit

First, the test was conducted on an analog signal transmission circuit to verify its performance. A test board, including a power splitter and transformer, was constructed. There were four single-ended outputs of the transformers. The S_{21} parameter from the input signal to each transformer output was tested using a network analyzer.

Theoretically, the differential output power can be calculated as the summation of both single-ended powers. As a result, the S_{21} parameter from the input signal to each transformer's differential output was calculated. The test results are shown in Fig. 7a, where the $-$ 3 dB bandwidth of the analog signal transmission circuit was wider than 7.5 GHz.

4.2 System performance

In the next phase of the test, the dynamic performance of the 20-Gsps 12-bit TIADC system was tested according to the IEEE standard. The input signal was generated by an RF signal generator with an output frequency ranging from DC frequencies to 6 GHz.

First, the bandwidth performance was tested. The output power of the signal generator was a constant value, and the output frequency was changed to measure the output amplitude at different frequencies. The test results are shown in Fig. 7b, where the $-$ 3 dB bandwidth of the entire system was up to 6 GHz. The bandwidth performance curve had a similar shape to that of the simulation result on the insertion loss of the analog transmission circuit when the transmission lines were included, as shown in Fig. 3b. Hence, the insertion loss of the transmission lines can be assumed to be the primary cause of the change in gain between 5 and 6 GHz.

Next, the ENOB performance was tested. The output frequency of the signal generator was adjusted to ensure that the signal amplitude sampled by the ADC was $-$ 1 dBFS approximately. By exerting the FFT on the test result, the frequency spectrum was obtained, and the signal-to-noise and distortion ratio (SINAD), as well as the ENOB performance, were calculated as follows:

$$\mathrm{SINAD} = 10\lg\frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}} + P_{\mathrm{harmonics}}} \approx 6.02\mathrm{ENOB} + 1.761. \tag{4}$$

The output frequency spectrum for the 347-MHz input is shown in Fig. 7c (single ADC) and Fig. 7d (interleaved ADC1 and ADC2), where remarkable peaks can be observed at certain frequencies, which corresponds to the mismatch errors. For a single-frequency input signal with an angular frequency of ω_0, the gain error and skew error appeared at a frequency of $\omega_0 \pm k\frac{2\pi}{MT_s}(k \le M/2)$. The offset error appeared at the frequency of $k\frac{2\pi}{MT_s}(k \le M/2)$, which is a fixed frequency point without any correlation with the input signal frequency. The ENOB of the interleaved sampling result was approximately 8 bits at 347 MHz. Compared to the ENOB of a single ADC bank, which was 8.7 bits at 347 MHz, the mismatch error caused a deterioration as expected and a correction process was necessary.

Next, the correction effect was tested and verified. A four-channel correction was conducted for a single ADC, and an eight-channel correction was performed for the interleaved ADC1 and ADC2. The frequency spectrum at the 347-MHz input after the error correction is shown in Fig. 7e (single ADC) and Fig. 7f (interleaved ADC1 and ADC2), where the mismatch error peaks are observed to be significantly eliminated by the correction algorithm. The ENOB was approximately 8.7 bits at 347 MHz after the error correction.

Finally, to verify the system performance in a wide frequency band, we also performed a frequency sweep from 50 MHz to 6 GHz. By adjusting the amplitude of the signal generator, it was ensured that the signal amplitude sampled by the ADC was approximately $-$ 1 dBFS at each frequency in the frequency band during the test. The ENOB performance before and after correction is shown in Fig. 7g, where the dashed line indicates the ENOB performance prior to correction. During the correction process, the FIR filter order was changed between 100 and 150 for a correction performance comparison. Before the error correction, the ENOB performance was approximately 8 bits at frequencies lower than 1 GHz. However, as the signal frequency increased, the performance deteriorated immediately and was up to 5 bits at frequencies greater than 3.2 GHz. Following the error correction, the ENOB performance was 8.7 bits at 347 MHz, 8 bits at 4 GHz, and 7.6 bits at 6 GHz, which sufficiently coincided with the results of a single ADC.

Consequently, the proposed system has a wide-bandwidth performance and sufficient ENOB performance. The perfect reconstruction mismatch error correction algorithm can be considered to be effective in the proposed system.

5 Conclusion

In this study, a 20-Gsps 12-bit TIADC system was designed and tested. A high-quality analog signal transmission circuit and clock generating circuit were designed to enhance the system performance. A mismatch error correction method based on the perfect reconstruction correction algorithm was developed, and its efficiency was

verified by tests. The test result showed that the sampling system bandwidth was up to 6 GHz, while the ENOB performance was 8.7 bits at 1 GHz, 8 bits at 4 GHz, and 7.6 bits at 6 GHz, and was significantly improved by the mismatch error correction process.

Author contributions All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by Ruo-Shi Dong, Wen-Tao Zhong and Yi-Chun - Fan. The first draft of the manuscript was written by Ruo-Shi Dong, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

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