

Fast pulse sampling module for real-time neutron–gamma discrimination

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Abstract An adaptable and compact fast pulse sampling module was developed for the neutron–gamma discrimination. The developed module is well suited for low-cost and low-power consumption applications. It is based on the Domino Ring Sampler 4 (DRS4) chip, which offers fast sampling speeds up to 5.12 giga samples per second (GSPS) to digitize pulses from front-end detectors. The high-resolution GSPS data is useful for obtaining precise real-time neutron–gamma discrimination results directly in this module. In this study, we have implemented real-time data analysis in a field programmable gate array. Real-time data analysis involves two aspects: digital waveform integral and digital pulse shape discrimination (PSD). It can significantly reduce the system dead time and data rate processed offline. Plastic scintillators (EJ-299-33), which have proven capable of PSD, were adopted as neutron detectors in the experiments. A photomultiplier tube (PMT) (model #XP2020) was coupled to one end of a detector to collect the output light from it. The pulse output from the anode of the PMT was directly passed onto the fast sampling module. The fast pulse sampling module was operated at 1 GSPS and 2 GSPS in these experiments, and the AmBe-241 source was used to examine the neutron–

gamma discrimination quality. The PSD results with different sampling rates and energy thresholds were evaluated. The figure of merit (FOM) was used to describe the neutron–gamma discrimination quality. The best FOM value of 0.91 was obtained at 2 GSPS and 1 GSPS sampling rates with an energy threshold of 1.5 MeV_{ec} (electron equivalent).

Keywords Real time · Neutron–gamma discrimination · Domino Ring Sampler 4 · Plastic scintillators

1 Introduction

Neutron detection is very important in many fields including homeland security, nuclear weapon detection, and medical science [1]. It is necessary to discriminate neutrons from gamma rays in mixed neutron–gamma fields. Gamma rays and neutrons could be discriminated in the intensity of their tail components of the light pulse output from organic plastic scintillators. The pulse of a neutron has a relatively high intensity slow tail component [2, 3]. A neutron detector equipped with EJ-299-33, which is the first commercial plastic scintillator with pulse shape discrimination (PSD) capability, was developed in this study [4–9]. A photomultiplier tube (PMT XP2020) is coupled to the plastic scintillator to collect the output light and amplify the electrons generated by the photocathode. We first developed a fast pulse sampling module based on the DRS4 chip as the data acquisition system for real-time neutron–gamma discrimination. The DRS4 chip has nine channels and every channel has 1024 sampling cells. DRS4 can provide sampling rates between 0.7 and 5.12 giga samples per second (GSPS) at an affordable cost [10–15].

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Fast pulse sampling can give maximum information about particles that interact with detectors.

In some high-radiation fields, the total data rate can become very high, in the order of gigabit per second. It is difficult to store and process such data offline. Solving this problem at the data acquisition site by using real-time data analysis is an effective approach [12]. Owing to variation in the IC manufacturing process, offsets of 1024 sampling cells in each channel of DRS4 show different values [10, 11]. The DC offset calibration is required to obtain accurate PSD results between neutrons and gamma rays. In this work, a new online DRS4 DC offset calibration method using a field programmable gate array (FPGA) was developed. This new method makes real-time data analysis possible in the fast pulse sampling module. After DC offsets calibration, a digital charge comparison algorithm was implemented in the FPGA for real-time PSD. This module was specifically designed to allow real-time digital neutron–gamma discrimination. The final PSD results show that the fast pulse sampling module is well suited for low-cost and low-power consumption PSD applications.

2 Experimental methodology

2.1 Experimental setup

Neutron–gamma discrimination experiments were performed using the neutron–gamma source AmBe-241 at the Institute of High Energy Physics. Figure 1 shows an overview of the experimental architecture. Plastic scintillators (EJ-299-33) were used as neutron detectors. EJ-299-33, which has been proven capable of PSD [3–7], is a relatively new scintillator used for neutron detection. It exhibits some advantages over traditional liquid organic scintillators, such as increased durability and flexibility in manufacturing detectors of various sizes and shapes. Compared with the standard plastic and liquid scintillators such as EJ-301, the EJ-299-33 scintillator exhibits a decreased light output and discrimination capability [5, 6].

XP2020 PMTs were coupled to EJ-299-33 scintillators to collect the output scintillation light. Pulses from the anodes of the PMTs were passed onto this module directly

through coaxial lines without any signal amplification and shaping circuits. In the fast pulse sampling module, a DRS4 chip recorded the input signals continuously at 1 GSPS and 2 GSPS sampling rates in internal switched capacitor arrays (SCA). The recorded content of each sampling cell was read out and digitized with an external 14-bit resolution analog-to-digital converter (ADC) at a relative low frequency (33 MHz) [10, 11]. The digitized waveform was then sent into the FPGA for real-time data analysis. Finally, the neutron–gamma discrimination results were transmitted to the backend PC using the UDP protocol.

2.2 Design of fast pulse sampling module

Figure 2 is the actual image of the fast sampling module. Figure 3 shows a functional block diagram of the fast sampling module. The fast pulse sampling module has four input channels on a 10 cm × 6 cm PCB. The four analog inputs are AC coupled and have an input range of 1 V peak to peak [10]. On the input side, the single end signals were converted into differential signals by TH4508 to meet the DRS4 input requirements. The differential signals were continuously sampled in DRS4. The sampling rate of the DRS4 can be programmed to 0.7–5.12 GSPS by adjusting reference clock frequencies.

A local trigger for each channel was generated by a fast comparator and then fed into FPGA. The local trigger threshold was adjusted by setting DAC values. The DAC also provided BIAS and ROFS DC voltage for the DRS4 chip [10]. A global trigger logic was built in the FPGA, which allowed for achieving significant background noise reduction with the smart trigger logic. The global trigger logic can be altered by reprogramming the FPGA firmware. After the global trigger was met in FPGA, the DRS4 chip stopped sampling the input signals and the contents of the frozen sampling cells were read out through the read shift registers and digitized with an external ADC. There is an unavoidable dead time of about 33 μs when using the full readout mode. To reduce the dead time, it is possible to read only a subset of all sampling cells by the ROI mode [10]. In real-time data analysis, only 700 out of all 1024 samples in one waveform were used for PSD. We can read

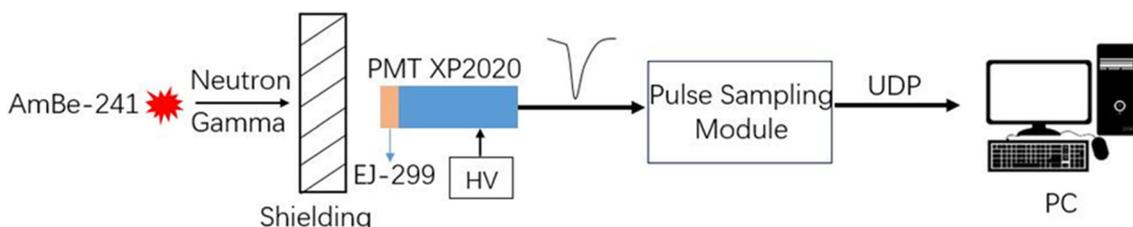
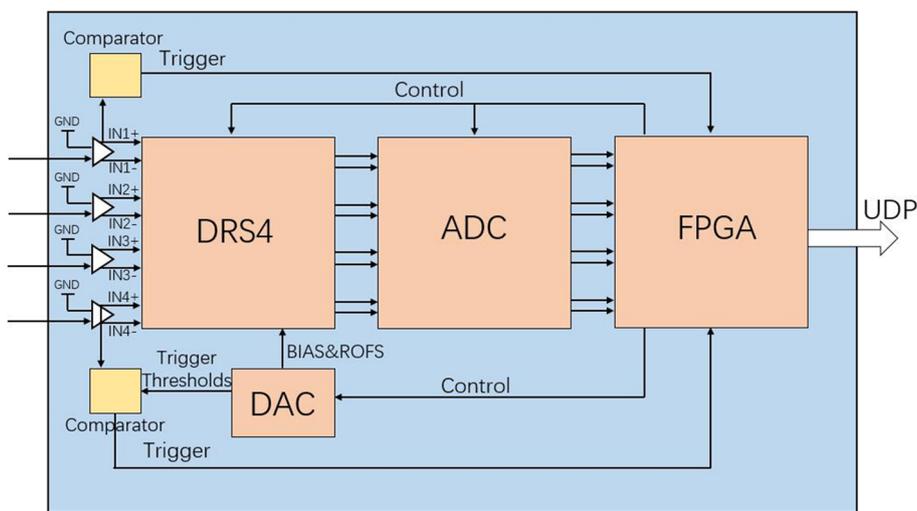


Fig. 1 Overview of the experimental architecture. A lead brick was used as the shielding

Fig. 2 Image of DRS4 module PCB



Fig. 3 Block diagram of fast sampling module



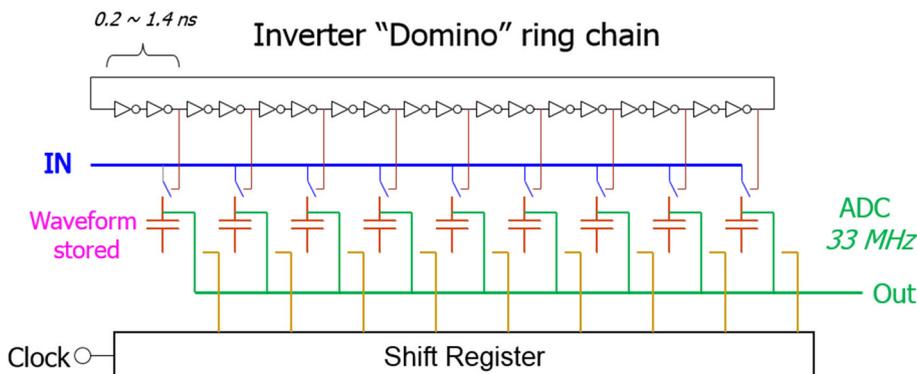
out only 700 samples by the ROI mode. Therefore, the dead time can be reduced by 30%.

2.3 Online offset calibration

The DRS4 chip contains a ring buffer with 1024 samples for each channel, as shown in Fig. 4. The ring buffer is

built as a chain of capacitors. The input signal is fed continuously to these capacitors. There are different offsets of 1024 sampling cells to a certain DC input owing to variations in the IC manufacturing process [13–15]. The uncalibrated data has a noise level on the order of approximately 10 mV RMS, as shown in Fig. 5 (left side) [8]. A DC offset calibration is required for accurate PSD.

Fig. 4 Simplified schematics of DRS4 domino wave circuit



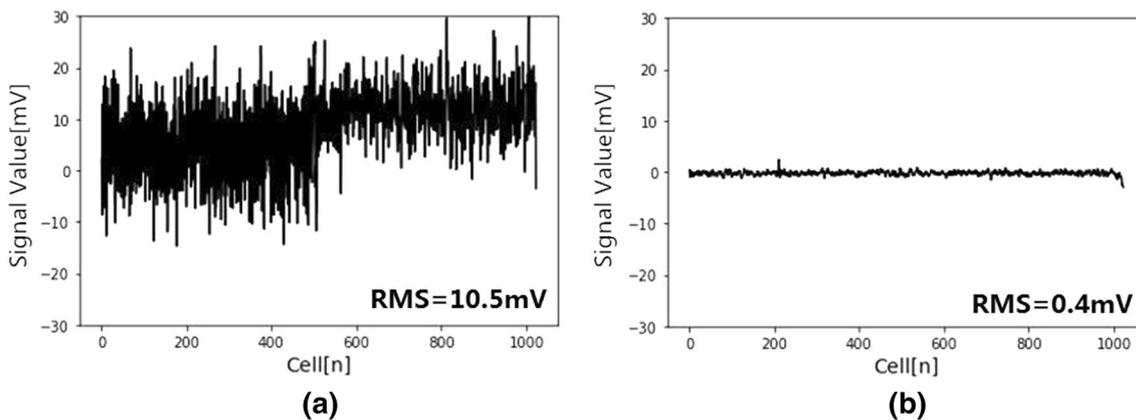
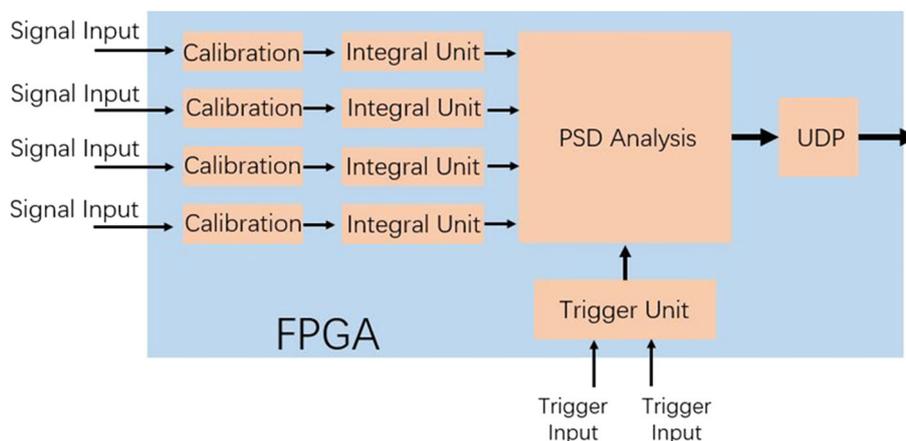


Fig. 5 **a** 0 V DC voltage sampled before DC offset correction; noise level is 10.5 mV RMS. **b** 0 V DC voltage sampled after DC offset correction; noise level is 0.4 mV RMS

Fig. 6 Data processing flow in FPGA



The offset in a cell has negligible variation; therefore, it is easy to correct the offsets by using averaged values. In this work, an online DC offset calibration method using the FPGA was developed. In the offset calibration process, a high precision 0 V DC voltage generated by the on-board 16-bit DAC was connected to all DRS4 inputs and sampled [11]. The offset voltage and gain of each sampling cell were evaluated in the FPGA and then stored in random-access memory (RAM) inside the FPGA. The entire process took some milliseconds. A RAM with a 14-bit width and 1024-bit data depth was deployed for each channel. The address of the RAM corresponded to the serial number of the sampling cell and ranged from 0 to 1023. The offset was removed while the digitized waveform streamed into the FPGA. After offset correction, as shown in Fig. 5 (right side), the noise level was reduced to about 0.4 mV RMS, which, although acceptable, is slightly higher than the 0.35 mV from the DRS4 data sheet [10]. After the offset calibration, the data was sent to the integral unit and the PSD analysis unit in the FPGA (Fig. 6). Although the total data size of one digitized pulse produced by incident neutron or gamma ray is 1792 byte, the PSD result of one

incident particle event is only 8 bytes. Compared with the method that transmits the whole digitized waveform to the backend PC, under the circumstance with counting rate of 10,000 particles per second, the data rate can be reduced to only 80 KB/s when the real-time algorithm is implemented.

2.4 Energy calibration

Compton scattering dominated the interactions of gamma rays within the EJ299 plastic detector owing to the intrinsic property of the plastic scintillator and its small size (1 cm × 1 cm × 5 cm). Therefore, energy calibration was carried out by using the Compton edge energy of Cs-137 and Co-60 gamma sources in each radionuclide energy spectrum. The pulse height distributions are shown in Fig. 7. The Compton edge energy of Cs-137 gamma rays is 477 keV. Energies of Compton edges for Co-60 gamma rays are 963 keV and 1119 keV. Energy calibration was obtained by averaging the two Co-60 Compton edge values because of the small detector size (1 cm × 1 cm × 5 cm). The Compton edge energy was determined where the

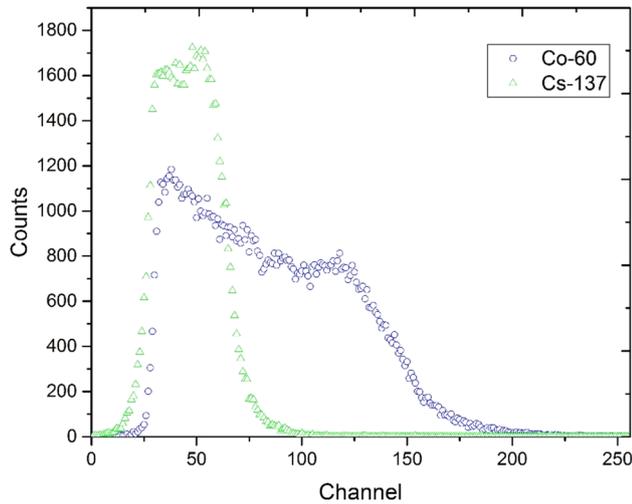


Fig. 7 (Color online) Co-60 and Cs-137 gamma pulse amplitude distribution

voltage amplitude of the Compton plateau reached 70% of its maximum intensity. The energy calibration result obtained is shown in Fig. 8.

2.5 Real-time pulse shape discrimination

The PSD method was developed based on the difference between scintillation lights from neutron and gamma-ray interactions in the EJ299-33 scintillator. The relative ratio of the slow component to the total scintillating light depends on the type of interaction, i.e., recoiling of electrons for gamma rays and recoiling of protons for neutrons [5–7]. Neutrons were identified by a higher slow component fraction compared with that of gamma rays.

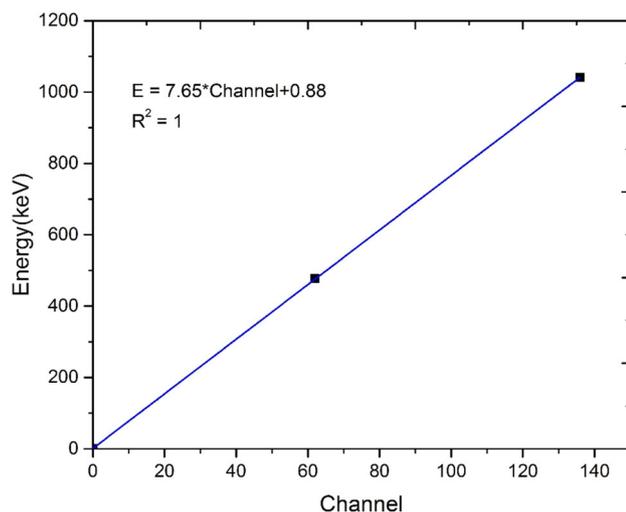


Fig. 8 Detector energy calibration result with Co-60 and Cs-137 gamma sources

The charge comparison method is well suited for the FPGA. Accordingly, it was adopted as the method for PSD in this study [16–18]. Using this method, every signal was integrated at the same time through two separate routes in the integral unit of the FPGA. Figure 9 shows the two integral regions. The long integral region started at the peak of the pulse and extended to approximately 350 ns after the zenith of the pulse (I_{long}). The short integral started at the same position as the first integral and ended at approximately 20 ns after the zenith (I_{short}). The two regions of the integration are critical for this method, because the integration ending point can be optimized to enhance the neutron–gamma discrimination. The integration parameters can be easily modified by reprogramming the FPGA.

After integration, the data was sent to the PSD analysis unit. The PSD is defined as

$$\text{PSD} = \frac{I_{\text{short}}}{I_{\text{long}}}. \quad (1)$$

The ratio $I_{\text{short}}/I_{\text{long}}$ of each channel was calculated in real time in the PSD analysis unit. The data size was reduced significantly after passing through the PSD analysis unit. Finally, the real-time PSD results were transmitted to the post-processing backend by using a gigabit ethernet link. A widely used figure of merit (FOM) method was used to characterize the discrimination capability [18]. The FOM is defined as

$$\text{FOM} = \frac{\Delta X}{(\delta_{\text{gamma}} + \delta_{\text{neutron}})}, \quad (2)$$

where ΔX represents the distance between the gamma and neutron peaks, and δ_{gamma} and δ_{neutron} represent the full width at half maximum of the corresponding peaks. The neutron and gamma peaks were fit with two Gaussian functions.

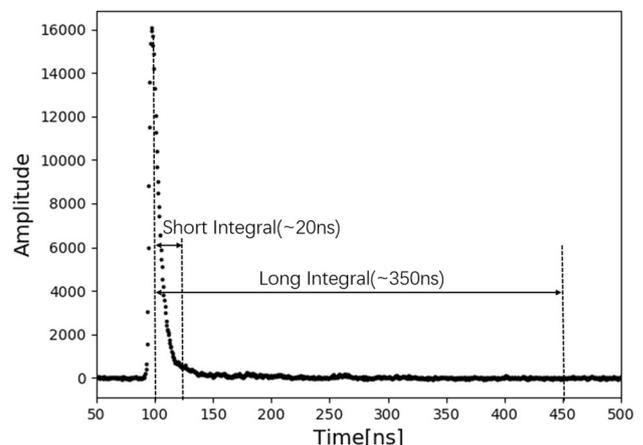


Fig. 9 Sampled signal after calibration. The plot illustrates the two integral regions for gamma–neutron discrimination

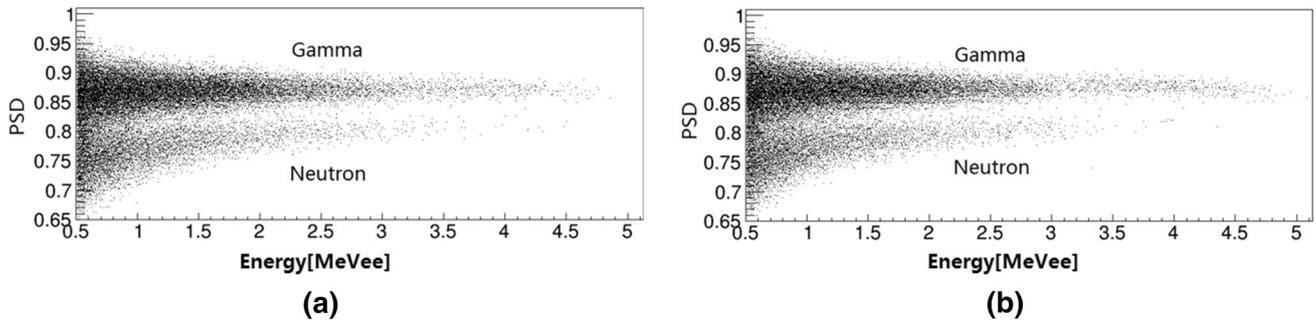


Fig. 10 PSD scatter distribution with 0.5 MeV_{ec} threshold using **a** 1 GSPS and **b** 2 GSPS sampling rates

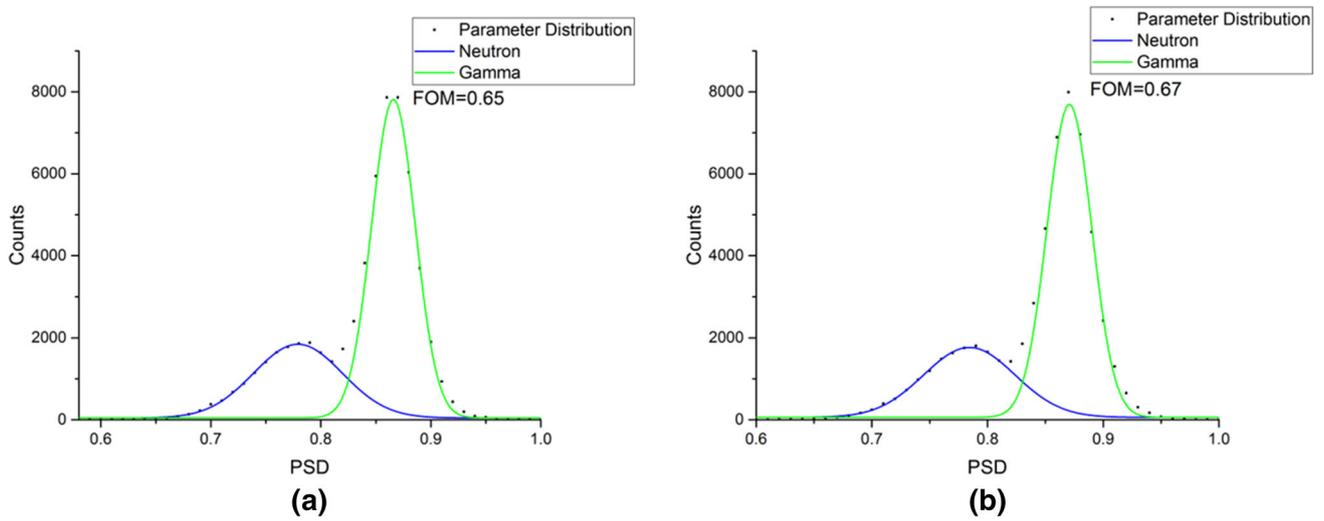


Fig. 11 I_{short}/I_{long} ratio distribution with 0.5 MeV_{ec} threshold, using **a** 1 GSPS and **b** 2 GSPS sampling rates

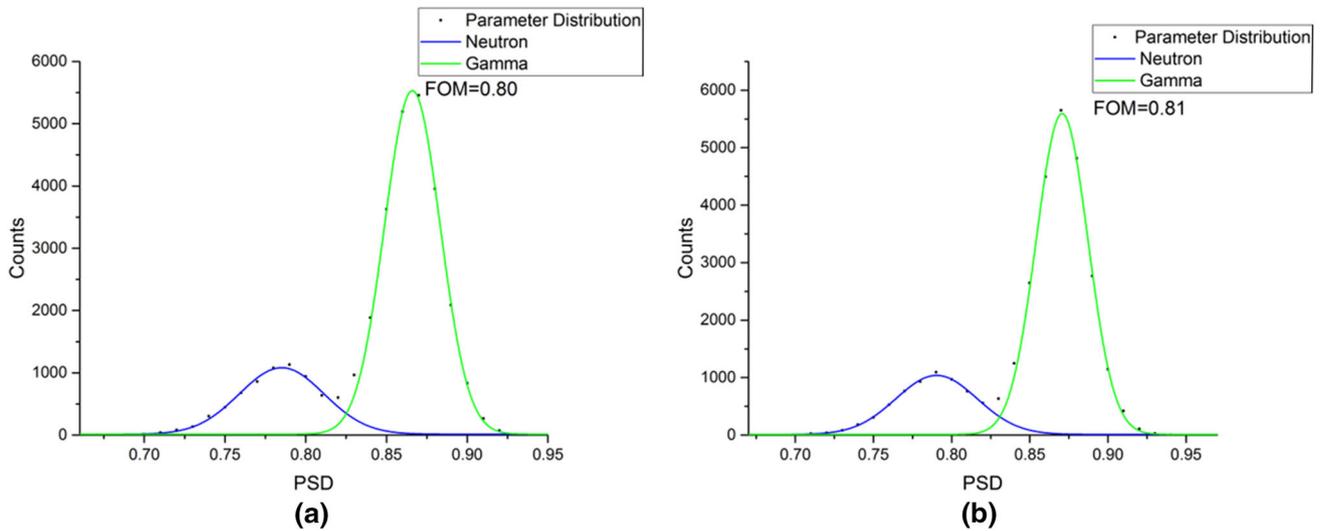


Fig. 12 I_{short}/I_{long} ratio distribution with 1 MeV_{ec} threshold, using **a** 1 GSPS and **b** 2 GSPS sampling rates

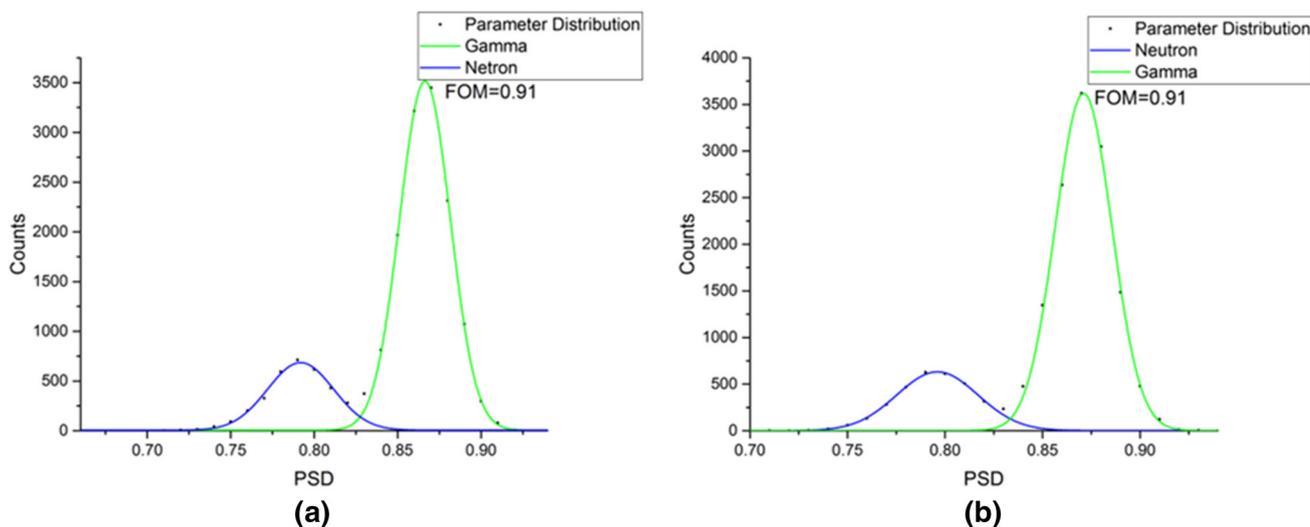


Fig. 13 $I_{\text{short}}/I_{\text{long}}$ ratio distribution with 1.5 MeV_{ee} threshold, using **a** 1 GSPS and **b** 2 GSPS sampling rate

3 Experimental results

The real-time PSD algorithm was implemented in the fast pulse sampling module and evaluated with different sampling rates. Figure 10 shows the PSD scatter plots at different sampling rates with the same energy threshold of 0.5 MeV_{ee}. As shown, two clusters are clearly identified. The lower cluster represents neutron pulses with a higher relative ratio of light in the slow component. The upper cluster represents gamma-ray pulses. The results show that the neutron and gamma-ray regions are clearly identified by visual inspection for 1 GSPS and 2 GSPS sampling rates using the real-time PSD method. This shows that the fast sampling module is capable of real-time neutron–gamma discrimination. However, the record length of DRS4 is limited to about 200 ns at 5.12 GSPS, which is not sufficient for accurate PSD results. The quality of particle identification was further evidenced by the FOM, as illustrated in Figs. 11, 12, and 13.

To calculate the FOM, only the energy points above an energy threshold are counted and shown along the y-axis. The resulting plots show PSD along the x-axis and energy points on the y-axis (Figs. 11, 12, 13). Figures 11 and 12 show that the 1 GSPS sampling rate is certainly capable, although poorly compared to 2 GSPS, of distinguishing neutrons from gamma rays above 0.5 MeV_{ee} and below 1.5 MeV_{ee}. The FOM values are 0.65 and 0.80 with the 1 GSPS sampling rate compared to 0.67 and 0.81 with the 2 GSPS sampling rate at the 0.5 MeV_{ee} and 1.0 MeV_{ee} threshold, respectively. In Fig. 13, with the energy threshold of 1.5 MeV_{ee}, the FOM value of 0.91 was obtained both at 1 GSPS and at 2 GSPS sampling rates. If the FOM is greater than 0.75, the theoretical rejection ratio for gamma rays from neutrons will be greater than 12.5:1 [19].

4 Discussion and conclusions

In this study, the EJ-299-33 plastic scintillator coupled to an XP2020 PMT was used for neutron detection. Pulse output from the PMT was sampled by the fast pulse sampling module, which can offer sampling rates up to 5.12 GSPS based on DRS4. The fast pulse sampling module was optimized and specially designed for real-time neutron–gamma discrimination. In this module, a real-time data analysis algorithm was optimally implemented in the FPGA. We also successfully developed an online DRS4 DC offset calibration method by using the FPGA. The real-time data analysis not only obtained acceptable PSD results between neutrons and gamma rays but also reduced the data rate and system dead time significantly. AmBe-241 was used as the neutron source to evaluate the performance of this module. The best FOM value of 0.91 was obtained both at 2 GSPS and at 1 GSPS sampling rates with an energy threshold of 1.5 MeV_{ee}.

The FOM values with different energy thresholds are acceptable for PSD performance. However, some reported PSD results obtained by using fast flash ADC (FADC) waveform digitizers are better than those obtained in this study [4–7]. We think that the inferior PSD performance was most likely caused by the high level of noise (0.4 mV RMS) introduced by the DRS4 chip because the tail part of a pulse is vulnerable to noise. The noise in our fast sampling module is twice as high as that in general commercial FADC waveform digitizers, e.g., DT5730 (0.2 mV RMS), which is an 8-channel 14-bit 500 MS/s FADC waveform digitizer with 2 V_{pp} dynamic range [20]. The low input dynamic range of DRS4 (1 V_{pp}) possibly resulted in the loss of signal shape information. Because of these reasons, the FOM values did not increase significantly when the

sampling rate was improved. For applications such as handheld devices, minimal power consumption, small device size, and affordability are very necessary. The commercial fast FADC is costly, has low channel density, and consumes relatively high power of a few watts per channel. In some applications, DRS4 is an effective alternative to the FADC, because it can offer fast sampling frequency, high channel density, and low power consumption (17.5 mW per channel) at an affordable cost. The fast pulse sampling module developed in this work is well suited for low-cost and low-power consumption PSD applications.

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