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Development of readout electronics for bunch arrival-time monitor system at SXFEL

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Abstract A bunch arrival-time monitor (BAM) system, based on electro-optical intensity modulation scheme, is under study at Shanghai Soft X-ray Free Electron Laser. The aim of the study is to achieve high-precision time measurement for minimizing bunch fluctuations. A readout electronics is developed to fulfill the requirements of the BAM system. The readout electronics is mainly composed of a signal conditioning circuit, field-programmable gate array (FPGA), mezzanine card (FMC150), and powerful FPGA carrier board. The signal conditioning circuit converts the laser pulses into electrical pulse signals using a photodiode. Thereafter, it performs splitting and low-noise amplification to achieve the best voltage sampling performance of the dual-channel analog-to-digital converter (ADC) in FMC150. The FMC150 ADC daughter card includes a 14-bit 250 Msps dual-channel high-speed ADC, a clock configuration, and a management module. The powerful FPGA carrier board is a commercial high-performance Xilinx Kintex-7 FPGA evaluation board. To achieve clock and data alignment for ADC data capture at a high sampling rate, we used ISERDES, IDELAY, and dedicated carry-in resources in the Kintex-7 FPGA. This paper presents a detailed development of the readout electronics in the BAM system and its performance.

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Keywords Bunch arrival-time monitor (BAM) · Shanghai Soft X-ray Free Electron Laser (SXFEL) · Field-programmable gate array (FPGA) · Signal conditioning · High-speed analog-to-digital converter (ADC)

1 Introduction

With the demand for the free electron laser (FEL) [1–3] pulse performance of modern X-ray FEL facilities such as the Shanghai Soft X-ray Free Electron Laser (SXFEL) [4–6] and Shanghai High repetition rate X-ray Free Electron Laser aNd Extreme light facility (SHINE) in Shanghai, European X-ray Free Electron Laser (European XFEL) [7] in Germany, Linac Coherent Light Source (LCLS) [8] and LCLS II [9] in USA, Swiss Free Electron Laser (SwissFEL) [10–12] in Switzerland, and Free Electron laser Radiation for Multidisciplinary Investigations (FERMI) [13] in Italy, a more stringent stability correction control is imposed on the radio frequency (RF) field amplitude and phase of RF gun and linear accelerator. The RF field stabilization is controlled by low-level radio frequency (LLRF) system based on accurate RF field measurements at the frequency of 2.856 GHz and 5.712 GHz, used for S-band and C-band accelerating structures in SXFEL, respectively. However, the more stable RF field control requirements are limited by the LLRF system control loop, which amplifies the noise as the gain increases [14]. A beam-based longitudinal stability feedback system can further improve the LLRF control accuracy by providing high-resolution real-time bunch arrival-time information from the bunch arrival-time monitor (BAM) system [15–18].

To identify and reduce the main source of bunch arrival-time jitter [19, 20], the BAM stations are placed in front of and behind the magnetic chicane. Bunches with different energies have different travel paths in the magnetic chicane. The higher energy bunches travel shorter path in the inner diameter, and the lower energy bunches travel longer in the outer diameter of the chicane. The shorter traveling path of the electron bunches will be completed in lesser time, whereas the longer traveling path of the electron bunches will be completed in more time. The beam relative energy fluctuation affects the arrival-time jitter of the electron bunches behind the magnetic chicane. The BAM stations placed in these positions were used to evaluate the electron bunches energy fluctuations. A block diagram of the bunch arrival-time monitor is shown in Fig. 1. The ultra-short laser pulse trains are modulated by a wide-bandwidth bipolar RF signal induced by a pickup cavity in the electro-optical intensity modulator (EOM). The laser pulse train is generated from the laser synchronization system having a frequency of 238 MHz. The readout electronics decodes the bunch arrival time by detecting the change in the amplitude of the modulated laser pulse which is proportional to the bunch arrival time. Based on the feedback of bunch arrival-time information calculated by the BAM system, the LLRF system can further reduce beam fluctuations by proper correction of the RF field of RF gun and the linear accelerating structures.

In this paper, we present the design and system architecture of the readout electronics and describe a scheme to achieve high-speed data capture for pulse signals. The performance of the readout electronics is evaluated by the actual measurement of the pulse signal.

2 Readout electronics design and architecture

According to [21], the resolution of the bunch arrival-time measurement is estimated by Eq. (1):

$$\Delta t \approx \frac{2 \times V_{\pi,\mathrm{RF}}}{S \times \pi \times T_{\mathrm{r}}} \times \Delta M. \tag{1}$$

$V_{\pi,\mathrm{RF}}$ and T_{r} are the inherent property parameters of the EOM device in the electro-optical front end. $V_{\pi,\mathrm{RF}}$ is the half-wave voltage. T_{r} represents the modulation depth of the EOM. The parameter S is defined by the RF signal induced by a pickup. ΔM is the laser amplitude noise, which measures the performance of the readout electronics and determines the resolution of the BAM system.

A designed schematic of photodiodes and conditioning circuit in readout electronics is shown in Fig. 2.

The laser pulses (at 238 MHz) from the EOM channel and optical clock channel are conditioned prior to the analog-to-digital converter (ADC) mezzanine board FMC150 [22] (two 14-bit ADC channels, 250 MHz). The average input optical power of a photodiode (ET3500F) is 0.98 mW, which is selected at an EOM bias voltage operating point. The operation point of the EOM is set at 50% of the EOM transmission curve [23]. For the EOM, the bias voltage of − 2.53 V is applied. To prevent the transmission from slipping into the nonlinear region, the modulation voltage is constrained to vary linearly between 20 and 80%. At the operation point, the laser pulse signal is converted into an electrical pulse signal with an amplitude of 67.7 mV at the output of the ET3500F. To reduce signal reflections caused by impedance mismatch, the 50-Ω coaxial cable lines are selected to balance an internal 50-Ω resistor of ET3500F. At the output of the ET3500F, the full

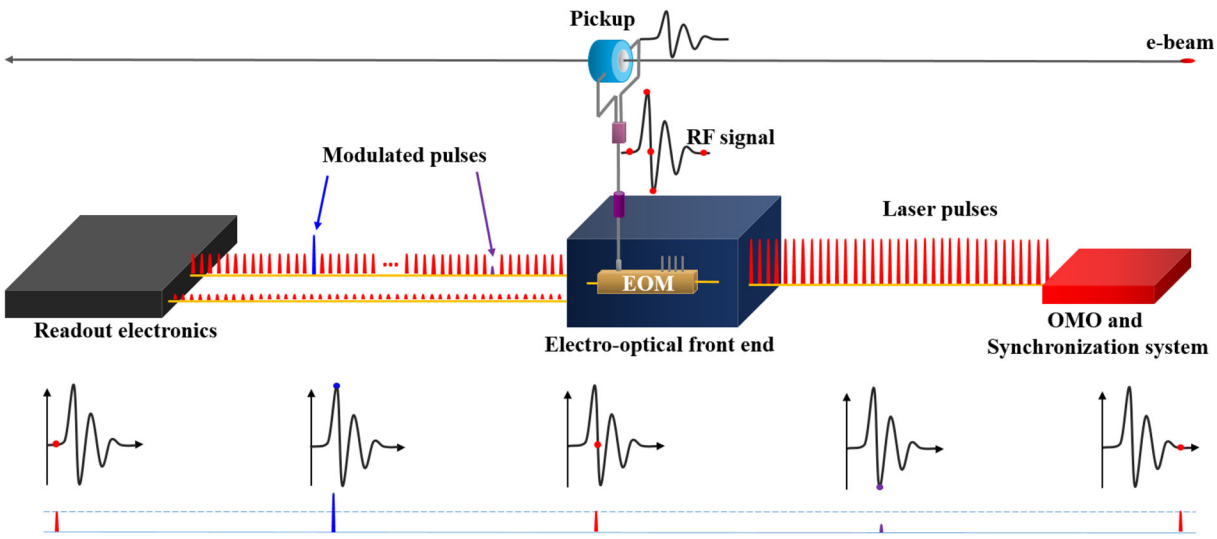

Fig. 1 (Color online) Block diagram of the bunch arrival-time monitor system. *EOM* electro-optical intensity modulator; *RF* radio frequency; *OMO* optical master oscillator

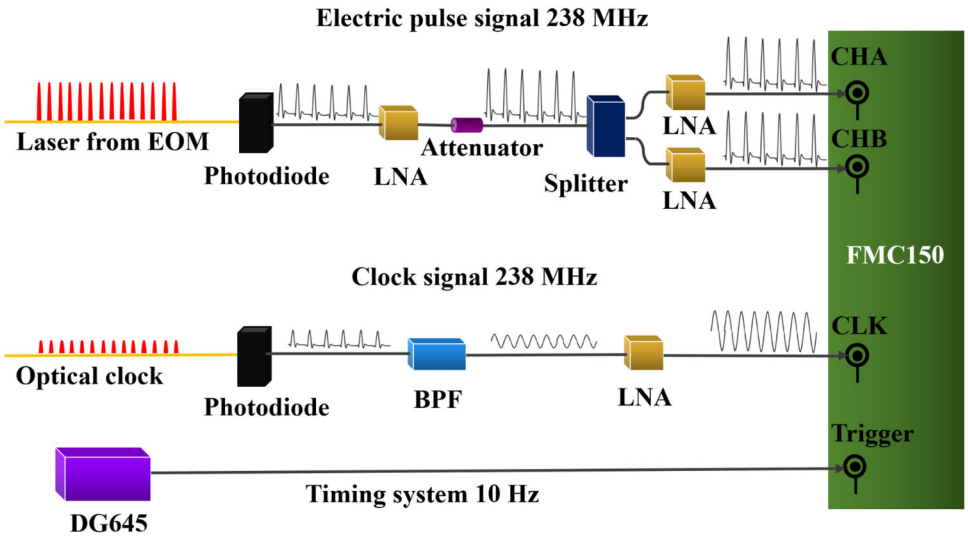

Fig. 2 (Color online) Schematic of photodiodes and conditioning circuit in readout electronics. *EOM* electro-optical intensity modulator; *LNA* low-noise amplifier; *BPF* 238-MHz band-pass filter; *DG645* digital delay generator; *FMC150* FPGA mezzanine card

width at half maxima (FWHM) of the electrical pulse is 682 ps measured by oscilloscope (Agilent Technologies, DSO9064A). The electrical pulse signal is amplified (mini-circuits, ZX60-33LN), attenuated (mini-circuits, VAT-10 +), and split (ATM, P212E) into a dual-channel ADC with amplitude of 295.4 mV, which operate at a quarter of the ADC full range (1.12 V). If the modulation voltage is applied, the amplitude of electrical pulse signal varies in the range from 112 to 448 mV. The bottom of the electrical pulse signals that the output of the photodiode is on the negative axis. Nevertheless, FMC150 is AC-coupled inputs that block the DC offset. In order to obtain the real amplitude of the pulse signals, the readout electronics system needs to simultaneously sample both peak and baseline of the pulse signals. The reference laser pulses are divided into two laser signals, one of which is used as an optical clock signal and the other is used for modulation in the electro-optical front end. In order to remove the influence of the external environment on the two channels, two single-mode fibers, used from the electro-optical front end to the readout electronics, are molded in the thermal insulation sleeve and are of equal length. In the readout electronics, the two channels have a similar structure (Fig. 2). Further, the RF devices are connected to each other using phase-compensated cables, which minimizes the impact of the environment on the relative phase of the two channels. Due to the filtering effort of the input bandwidth of the ADC (500 MHz), the resulting pulses have flat pulse top, followed by a board flat baseline. Thus, it is considered that they are always sampled at the same sample point of the two-channel ADC. Due to 250 MHz maximum sampling frequency of the ADC mezzanine board, each pulse signal with 238 MHz repetition rate can be completely captured without loss. The FMC150 digital data output was connected to a Kintex-7 field-programmable gate array (FPGA) [24] via double data rate low-voltage differential signaling (DDR LVDS) high-speed ADC interface [25].

The transmission of pulse signals to uncompensated single-mode fibers and electronic circuit will cause signal amplitude drift due to pressure, temperature, and voltage. By normalizing to each preceding pulse, slow amplitude drift from the pulse signals can be filtered out. The basic principle of this scheme is shown in Fig. 3 and Eq. (2).

$$A_{\mathrm{norm}.i} = \frac{\mathrm{Peak}_i - \mathrm{Baseline}_i}{\mathrm{Peak}_{i-1} - \mathrm{Baseline}_{i-1}}, \quad (i > 0) \tag{2}$$

Peak_i and $\mathrm{Baseline}_i$ represent the peak value of the i-th laser pulse and the baseline value of the i-th laser pulse, respectively. After a splitter, one of the channels (CHA) is used for peak value capture and the other (CHB) is used for baseline value capture. It is necessary to calibrate the amplitude of the two-channel signals and precise delays must be incorporated so that channel A always samples the peak and channel B has a fixed delay, Δt, relative to channel A. By subtracting the peak and baseline value of the two channels, one can calculate the real pulse amplitude. With the normalized processing to each preceding pulse signal scheme, slow amplitude drifts can be removed from the pulse signals.

3 High-speed data processing in FPGA

Interfacing FPGA to ADC high-speed digital data output is a common engineering design challenge. The precise data and source-synchronous clock alignment may be offset owing to board-level trace length mismatch or delays

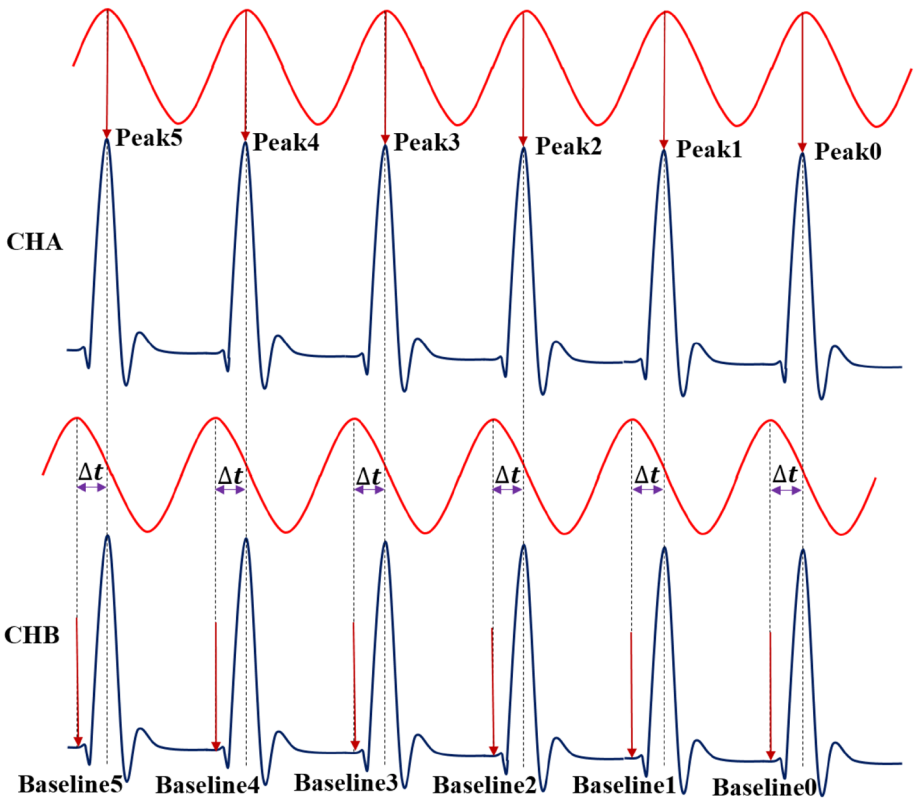

Fig. 3 Signal sampling principle of the readout electronics

inside the FPGA from the pad to the D-input of the synchronous latching element. Therefore, a design challenge is to maintain the precise alignment for correct data capture. A reliable scheme is proposed to dynamically self-align the clock by using dedicated deserializer components (ISERDESE2 and IDELAYE2 in FPGA) [26] and a state machine to keep the clock transition centered in the data-valid window in real time in order to calibrate for temperature, process, and voltage. A simplified schematic of the DDR LVDS high-speed ADC interface and data processing in the FPGA is shown in Fig. 4.

The DDR LVDS interface can be used to meet the high-speed and strong anti-interference ADC digital output. In this mode, two data bits are multiplexed and output on each LVDS differential pair. Even data bits D0, D2, D4, D6, D8, D10, and D12 are output at the rising edge of clk_238MHz_p, and the odd data bits D1, D3, D5, D7, D9, D11, and D13 are output at the falling edge of clk_238MHz_p. Both the rising and falling edges of clk_238MHz_p must be used to capture all the data bits (see Fig. 5).

The input delay and dedicated input serial-to-parallel logic resources are used for data and clock alignment inside the FPGA. IDELAYE2 is a programmable delay developed with a calibrated tap resolution in every I/O block of the Kintex-7 FPGA. The IDELAYE2 delay line has 32 taps of 78 ps when the reference frequency applied to the IDELAYCTRL [27] component is 200 MHz (± 10 MHz). The tap delay resolution is contiguously calibrated by the use of an IDELAYCTRL reference clock. A higher resolution of 52 ps or even 39 ps can be selected for a reference clock of 300 MHz (± 10 MHz) or 400 MHz (± 10 MHz), respectively. As shown in Fig. 5, the width of each bit is approximately 2.1 ns, which almost covers 27 taps for a resolution of 78 ps. The total delay range of an IDELAYE2 cover is approximately 2.5 ns for the 78-ps resolution mode. Therefore, the 78-ps resolution mode is sufficient for the bit clock alignment.

The process of clock and data alignment involves either shifting the clock relative to the data, or vice versa. In order to ensure the clock signal with the low jitter performance and source synchronization with the data, the mixed-mode clock manager (MMCM) input is directly from the ADC board. However, the MMCM can only shift the clock and cannot fix any mismatch between individual signals of the data bus. Therefore, it is considered optimal if the data bits are shifted individually relative to the clock. Fourteen-bit data are divided into seven differential pairs, and the data bits are aligned by seven IDELAYEs. The seven parallel IDELAYE2 outputs are converted from serial to parallel using an ISERDESE2. A data bit and clock auto-calibration state machine monitors the ISERDESE2 outputs and the deserialized and parallel captured clock bits. At system reset, the auto-calibration sequence configures the ADC

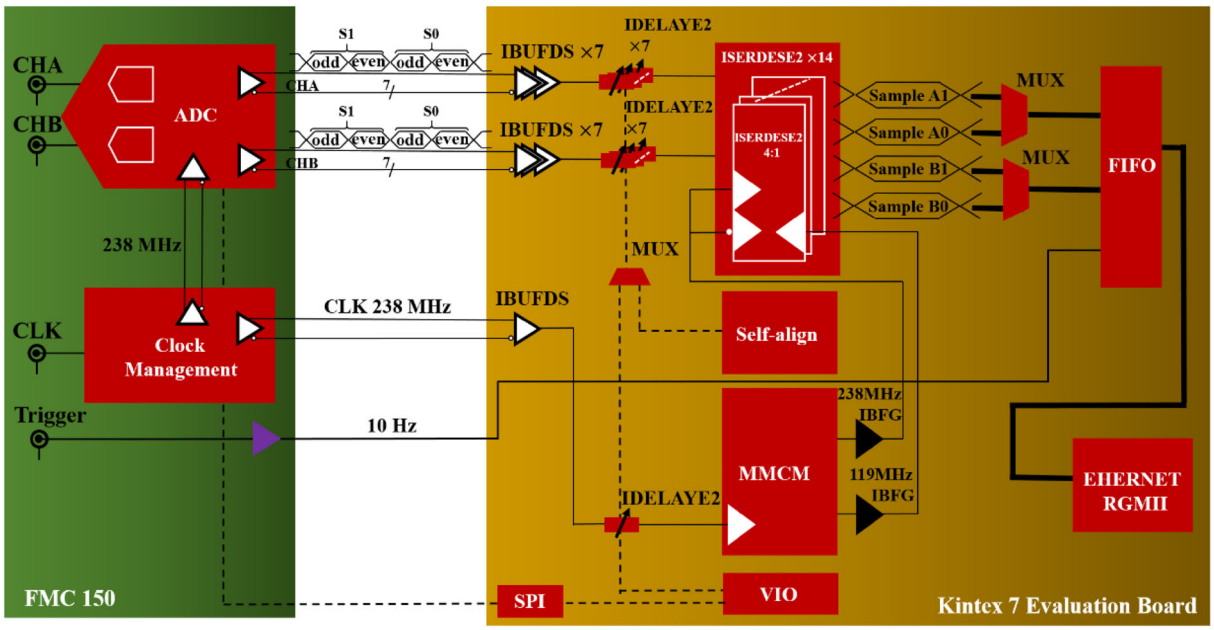

Fig. 4 (Color online) Simplified schematic of DDR LVDS high-speed ADC interface and data processing in FPGA

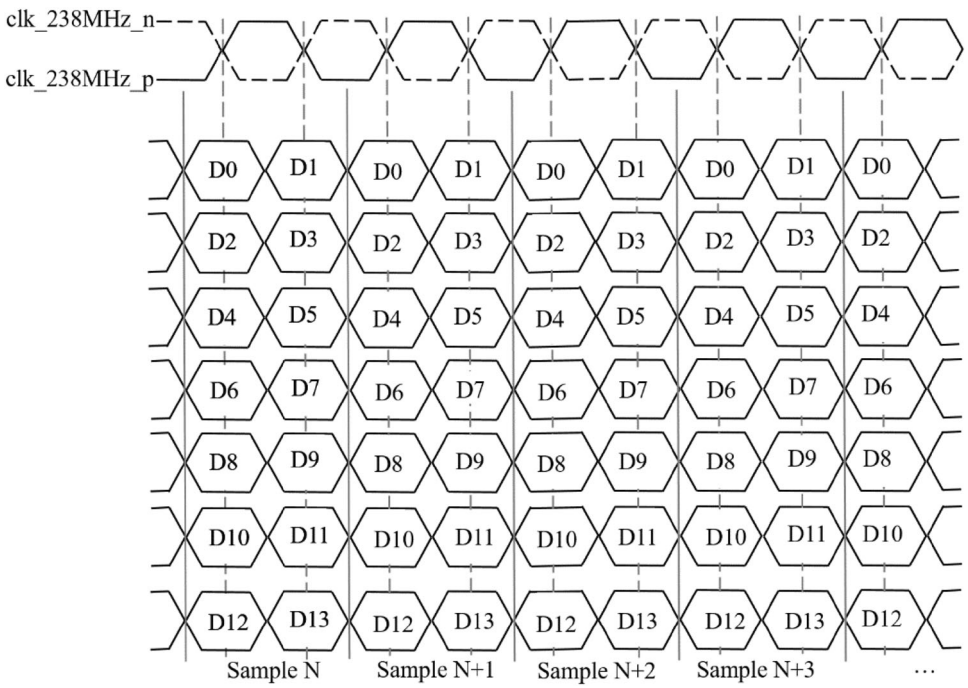

Fig. 5 DDR LVDS interface for bit clock alignment

into the test mode over the SPI port to generate a digital ramp pattern on both channels A and B. The auto-calibration sequence then adjusts IDELAYE2 until the test pattern is captured repeatedly without error. Both ADC channels are automatically set to the normal mode to capture pulse signals after the ramp patterns are captured successfully.

Even data bits (D0, D2, D4, D6, D8, D10, and D12) and odd data bits (D1, D3, D5, D7, D9, D11, and D13) are restored to 14-bit data (D0, D1, D2,…, D13) by MUXs after the ISERDESE2 output. To facilitate subsequent data processing, the 14-bit data are expanded to 16 bits using an REG, and zeros are filled by the last two bits.

In SXFEL, the repetition frequency of the electron bunch is 10 Hz, and the frequency of the laser pulse train is 238 MHz; thus, the modulated laser pulses take a small amount in it. In order to reduce the invalid storage of data and address the difficulty of data processing, we propose to

use trigger signal-enabled data storage in first input first output (FIFO) for filtering invalid data, as shown in Fig. 6. The digital delay generator (DG645) is applied to delay the position of the trigger signal relative to the RF signal induced by the electron bunch. The purpose of DG645 is to always keep the modulated sample in the middle of the entire valid data.

The tri-mode Ethernet media access controller (TEMAC) intellectual property (IP) core [28] is selected for simplifying the design of Ethernet data communications. The clock signal (200 MHz) of the Ethernet logic function module is provided by the crystal oscillator source on the Kintex-7 development board, and this clock is asynchronous with the ADC clock (238 MHz). Therefore, the FIFO module also has a function of signal processing at the clock domain crossing.

4 Test result and analysis

A readout electronics has been assembled to test and evaluate the overall performance of this system. A prototype of the system for field testing is shown in Fig. 7. As described above, the task of the readout electronics is to calculate the normalized amplitude of the laser pulse train, which carries information of the bunch arrival-time jitter. To this end, pulse signals leaving the photodiode are split by a power splitter and transmitted in a symmetrical path to two channels of the FMC150 board. Both ADC channels sample the same pulse signal at the same time; however, they have a slight phase shift relative to the clock signal in such a way that one channel keeps sampling peaks of the pulse signals and the other channel keeps sampling the baselines. The phase offset between the two ADC channel sampling points is adjusted by adding a fixed cable; this offset is calculated by individually scanning each pulse signal of the two channels with an optical delay line (ODL).

To systematically evaluate the performance of the readout electronics system, it is important to measure the whole pulse signal. For convenience of measurement, two laser pulse trains of 238 MHz are split from an optical synchronization system. One link is used as a synchronous clock signal for the ADC and the other as a measured pulse signal. A scanning pulse graph of the whole pulse signal is shown in Fig. 8. In order to perform full pulse signal measurement, the measured phase of the pulse signals is delayed step by step. Two optical delay lines connected in series are used for an accurate phase delay. The range of each optical delay line is 560 ps; thus, it can be accurately adjusted to 1.12 ns. To expand the phase shift range, two RF phase shifters are added in the front of the power splitter; the same can also be achieved by adjusting the fiber length. For each fixed delay sample point, 1024 sampled data were captured in the block RAM and used to calculate the average of this fixed delay point.

In the BAM system, the readout electronics system always samples the flat areas of the peak and the baseline. By subtracting the baseline values from the peak values, the real amplitude values can be calculated and are normalized to each preceding pulse signal. As shown in Fig. 9, the standard deviation of the normalized instantaneous amplitude noise is calculated to be approximately 0.28%.

The aperture uncertainty of the ADC clock signal is required to be evaluated according to its relationship with the ADC system performance. The ADC clock signal is a 238-MHz sinusoidal signal extracted directly from the laser pulse signal. During the evaluation, a Keysight E5052B signal source analyzer was used to measure the phase noise of the ADC clock signal, and the phase noise between 10 Hz and 10 MHz is approximately 188 fs (Fig. 10).

According to the ADS62P49 data sheet, the ADC's aperture jitter is 145 fs. Therefore, a total noise of 237 fs

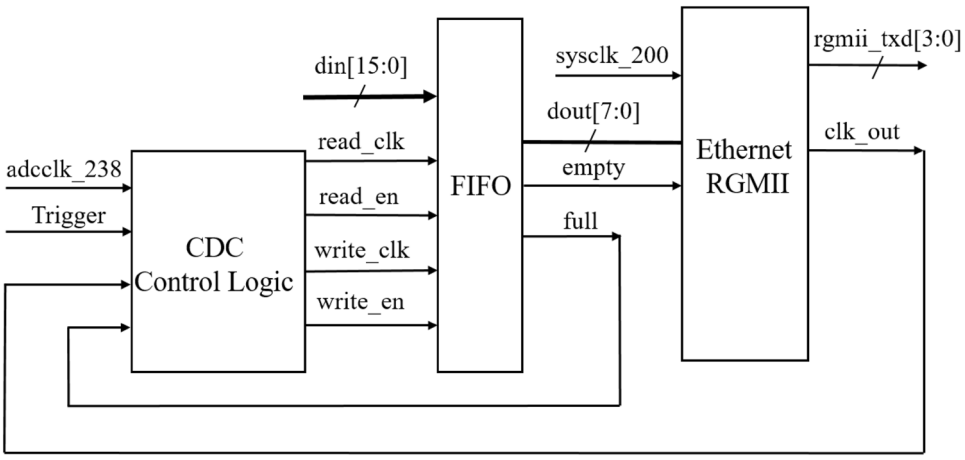

Fig. 6 Data filtering and corresponding clock domain crossing signal processing algorithm

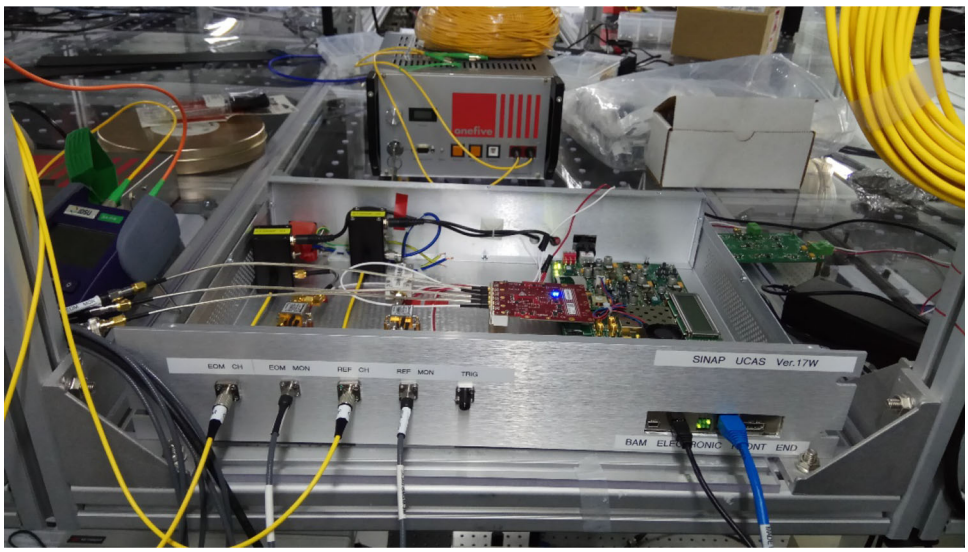

Fig. 7 (Color online) Prototype of the readout electronics and field-testing system

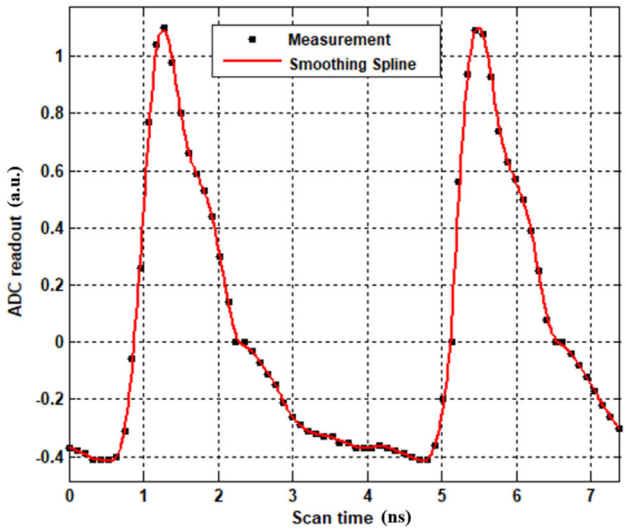

Fig. 8 Whole pulse signal measured with the readout electronics system

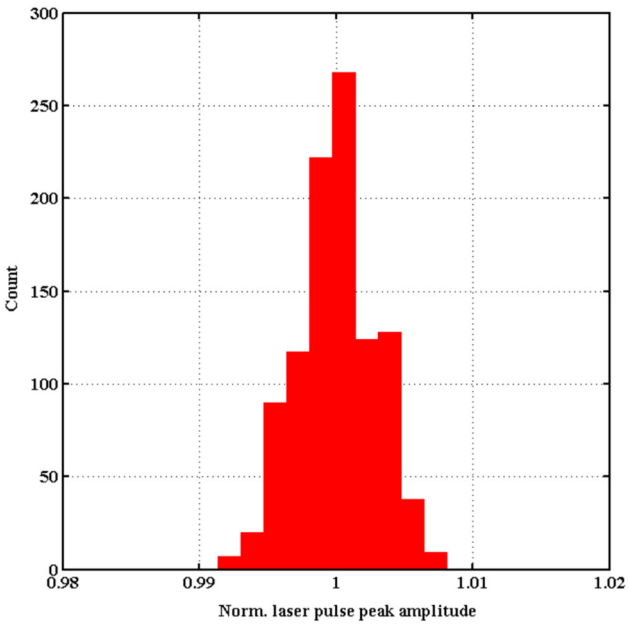

Fig. 9 Normalized amplitude of the pulse signals

can be calculated by combining the ADC's aperture jitter and the clock signal aperture jitter. As the ADC only samples the flat region of the pulse signal, this is considered to be a sufficiently low analog input frequency. Therefore, a total noise of 237 fs is expected, which is sufficient for high-precision data capture of the FMC150 board.

According to the principle of the BAM system, a change in the bunch arrival time will change the voltage (ΔV) that is superimposed on the bias voltage (corresponding to the operation point). In order to evaluate the relationship between the amplitude modulation of the pulse and the amplitude noise of the pulse caused by the relative phase shift between the clock and the pulse during modulation, we added a step-increasing modulation voltage (ΔV) to simulate the fluctuating voltage of the RF signal on the EOM's RF input port (Fig. 11). To avoid the pulse amplitude modulation interference caused by the EOM approaching the nonlinear region, we select an EOM modulation transmission interval of 20–80% as the modulation voltage variation range. Only the modulation voltage of the RF port is changed, while the other conditions are kept constant. By measuring the linear relationship (R^2) of the pulse amplitude with the change in the modulation voltage, it is possible to evaluate the modulation effect caused by the pulse shape change and the phase shift of the clock with respect to the pulse sampling point during the modulation. The modulation voltage input of the RF port

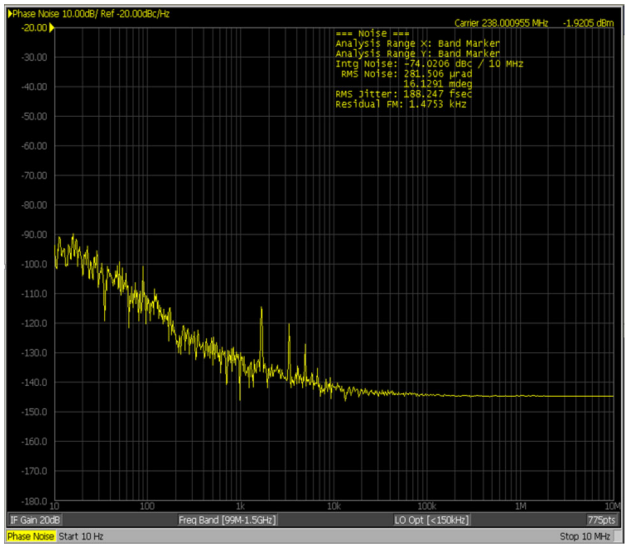

Fig. 10 (Color online) Keysight E5052B signal source analyzer phase noise measurement of the ADC 238-MHz clock signal extracted from laser pulses

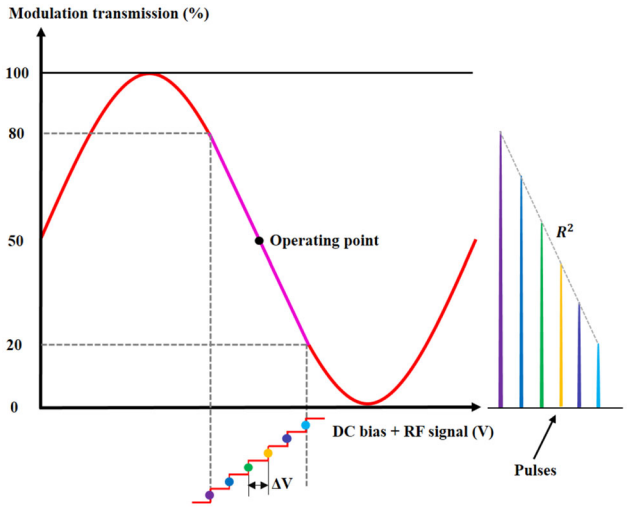

Fig. 11 (Color online) Scheme for evaluating the relationship between the amplitude modulation of the pulse and the amplitude noise of the pulse caused by the relative phase shift between the clock and the pulse during modulation. By adding a step-increasing modulation voltage (ΔV) to simulate the fluctuating voltage of the RF signal on the EOM's RF input port, the relationship and effect can be measured

ranges from − 1.1 V to 1.17 V with increments of 0.07 V. The linear relationship between the superimposed voltage (modulation voltage + bias voltage (− 2.53 V)) and the normalized ADC amplitude of the pulse is shown in Fig. 12. The linear relationship is calculated with $R^2 = 0.9992$. Therefore, the effect of the modulation process on the amplitude noise of the pulse caused by the relative phase shift between the clock and pulse is only 0.08%.

Figure 13 shows the normalized ADC data-collected modulation voltage, which decreases from − 0.28 V to − 0.56 V. Each point is normalized to each preceding pulse. The pink arrow indicates the modulation distinguish point.

5 Conclusion

As an important component of the BAM system, the accuracy of the readout electronics for measuring the modulated laser pulses will affect the resolution of the BAM system. In this paper, we present the system design and architecture with the first prototype of the readout electronics. We proposed a robust scheme to dynamically self-align the clock using the FPGA IDELAYE2 and ISERDESE2 resources to keep the clock transition centered in the data-valid window. Shifting the data bits individually relative to the clock can overcome this limitation; only shifting the clock cannot fix any mismatch between individual signals of the data bus. The amplitude noise of the laser pulses has been evaluated with instantaneous measurements using the readout electronics, and the amplitude noise caused by the relative phase shift between the clock and the pulses was evaluated to be only 0.08%. The standard deviation of the normalized amplitude noise measured in the current system is approximately 0.28%, which is an adequate measurement accuracy for the BAM system in SXFEL.

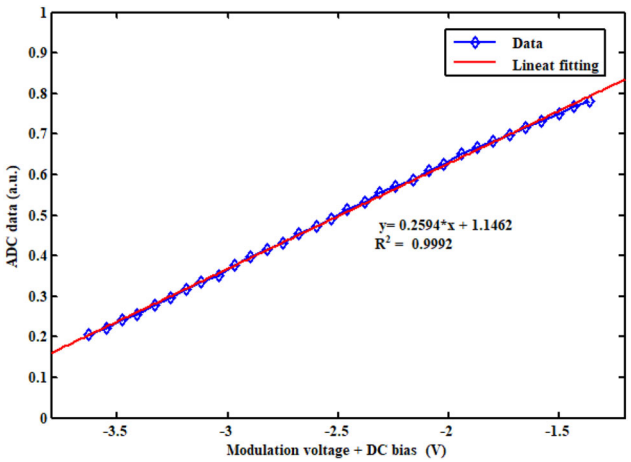

Fig. 12 Linear relationship between the superimposed voltage and the normalized ADC amplitude of the pulse

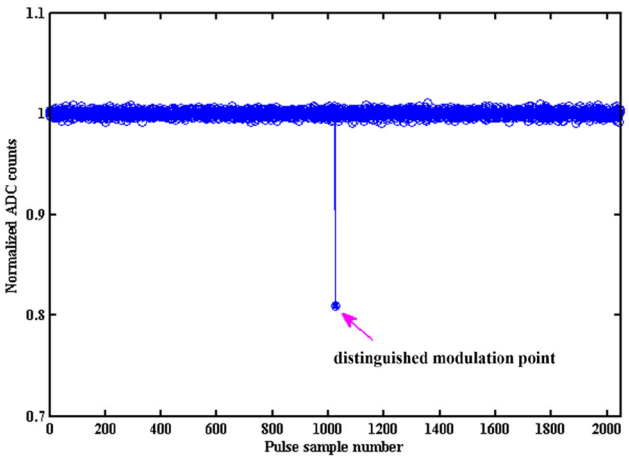

Fig. 13 Normalized ADC data-collected modulation voltage, which decreases from − 0.28 V to − 0.56 V

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