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# Heavy-ion and pulsed-laser single event effects in 130-nm CMOS-based thin/thick gate oxide anti-fuse PROMs

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**Abstract** Single event effects of 1-T structure programmable read-only memory (PROM) devices fabricated with a 130-nm complementary metal oxide semiconductor-based thin/thick gate oxide anti-fuse process were investigated using heavy ions and a picosecond pulsed laser. The cross sections of a single event upset (SEU) for radiation-hardened PROMs were measured using a linear energy transfer (LET) ranging from 9.2 to 95.6 MeV $cm^2$ $mg^{-1}$. The result indicated that the LET threshold for a dynamic bit upset was $\sim$ 9 MeV $cm^2$ $mg^{-1}$, which was lower than the threshold of $\sim$ 20 MeV $cm^2$ $mg^{-1}$ for an address counter upset owing to the additional triple modular redundancy structure present in the latch. In addition, a slight hard error was observed in the anti-fuse structure when employing $^{209}$Bi ions with extremely high LET values ($\sim$ 91.6 MeV $cm^2$ $mg^{-1}$) and large ion fluence ($\sim$ $1 \times 10^8$ ions $cm^{-2}$). To identify the detailed sensitive position of a SEU in PROMs, a pulsed laser with a 5-μm beam spot was used to scan the entire surface of the device. This revealed that the upset occurred in the peripheral circuits of the internal power source and I/O pairs rather than in the internal latches and buffers. This was subsequently confirmed by a $^{181}$Ta experiment. Based on the experimental data and a rectangular parallelepiped model of the sensitive volume, the space error rates for the used PROMs were calculated using the CRÈME-96 prediction tool. The results showed that this type of PROM was suitable for specific space applications, even in the geosynchronous orbit.

**Keywords** Anti-fuse PROM · Single event effects · Heavy ions · Pulsed laser · Space error rate

## 1 Introduction

Programmable read-only memory (PROM), as a one-time write memory, is one of the most stable and reliable devices for data storage. Thus, it has been used extensively in space electronic equipment over the past several decades. PROMs with good radiation tolerance to high-energy cosmic rays are ideal media to store the original code of electronic systems, for example the configuration memory for field-programmable gate array (FPGA) devices [1–3]. In such situations, any error in the PROMs may cause

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erroneous configurations of the target chip and threaten the normal operation of space vehicles in orbit.

In general, the memory cells of PROMs have a natural radiation resistance owing to their unique fabrication processes such as the oxide–nitride–oxide anti-fuse, amorphous silicon anti-fuse, and gate oxide anti-fuse [4–6]. Previous studies on single event effects (SEE) of PROMs verified that the memory cells of PROMs manufactured by the micron and submicron processes are almost immune to upset and latch-up [1, 2, 7]. However, the readout and control circuits rather than the storage elements seem to be very susceptible to SEE because of their complementary metal oxide semiconductor (CMOS) technologies. In [1, 2], at least seven ion-induced errors were observed in peripheral circuits, including dynamic upsets, address errors, and functional interrupts. This showed that the critical procedure for designing a PROM with high radiation tolerance involves effectively mitigating and evaluating the SEE sensitivity of peripheral circuits. Although the error types and mechanisms of SEE in PROMs were analyzed in [1, 2], there is no report that identifies the sensitive positions of the PROM's peripheral circuits as directly based on a positioning irradiation experiment. Moreover, with the feature size scaled down to the deep-submicron or even the nanometer level, a PROM with high density and large capacity was developed in recent years. Considering its wide application prospects in space electronics, the radiation response of these new type PROMs should be characterized in depth.

In this paper, the SEE of 1-T structure PROMs fabricated with a 130-nm CMOS-based thin/thick gate oxide anti-fuse process are analyzed by heavy ions and a pulsed laser. The thin/thick gate oxide anti-fuse technology is simple and compatible with traditional CMOS processes. This provides a possibility of both decreasing the area of the memory cell and increasing the read speed and storage capacity of the device. In previous works, it was demonstrated that bulk silicon epitaxy and deep well processes are effective in mitigating the SEE for this type of PROM in 180-nm and 130-nm processes [8, 9]. Furthermore, this paper focuses on conducting a systematical study of SEE in 130-nm CMOS-based PROM devices. The study includes a heavy-ion test, pulsed-laser mapping experiment, and space error rate prediction. In detail, error types such as the dynamic bit upset and address counter upset, the effectiveness of error detection and correction (EDAC)—and triple modular redundancy (TMR)—hardened strategies, the heavy-ion response of anti-fuse cells with a deep-submicron thin/thick gate oxide process, and the identification of sensitive circuits using a pulsed laser are analyzed and discussed in Sect. 3. For space applications, the aluminum shielding effect and space error rate are predicted and discussed in Sect. 4.

## 2 Experimental setup

### 2.1 Devices under test (DUT) details

The 1-T anti-fuse PROM has a fast read speed and high storage density (8 Mbits and 16 Mbits). Its memory unit is shown in Fig. 1. A non-volatile memory cell is achieved with the thick and thin oxide anti-fuse technique. The cell was fabricated as a single transistor with a thin/thick oxide gate [10]. The thin oxide region (4.5 nm) is penetrated under the action of high voltage, leading to a conductive channel, while the thick part (7.5 nm) can withstand high voltage with its high resistance. The breakdown position is fixed on the edge of the thick and thin oxide film, which is called the program area. The DUTs were decapped before exposure in order to make swift heavy ions reach the sensitive regions.

Each DUT adopted a 130-nm silicon epitaxial process with 16 layers including passivation and metal on top of the die. Compared with 8-Mbit PROMs, the storage of a single bit in a 16-Mbit PROM is achieved by two anti-fuse memory units in order to enhance its programming reliability. A guard ring structure can provide spatial and electrical isolation in CMOS circuits in order to prevent a single event Latch-Up (SEL). We fabricated p + guard rings connected to the ground and enclosed the n+ sources in order to reduce the minority carriers in an NMOS. In a PMOS, n+ guard rings connected to high voltage were used to prevent the influence of minority carriers in the transistor. An EDAC verification code generated by a Hamming code and TMR in an internal latch employed a triple modular voter circuit. EDAC and TMR are two main SEU-hardened methods that are further analyzed in Sect. 3.

The DUTs were utilized in dynamic mode at room temperature, and the frequency was controlled at 20 MHz (cycle time: 50 ns) with a 1-A current limitation. The cycle time can affect the number of captured errors created by particle-induced transient pulses in peripheral CMOS circuits and then can influence the effect of our error

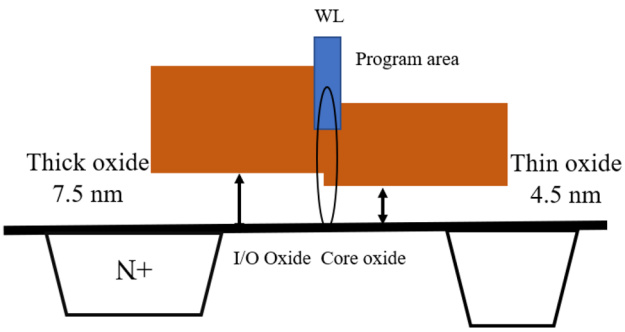


**Fig. 1** (Color online) Diagram of thin/thick gate oxide anti-fuse memory unit

correction methods (EDAC and redundancy). The DUT was employed using a serial addressing mode to read statistics, and its memories were continuously scanned by an FPGA-based tester. In the test process, the internal data in the DUT were a 00-FF circular sequence code. Once an error was detected, the error information including its address was recorded. Any error data and abnormal currents were investigated and presented on the screen.

### 2.2 Heavy-ion facility and parameters

Heavy-ion testing was carried out at the Heavy Ion Research Facility in Lanzhou (HIRFL) at the Institute of Modern Physics, Chinese Academy of Sciences, and at the HI-13 Tandem Accelerator at the China Institute of Atomic Energy. The flux of incident ions can be controlled at $10^4$ ions $cm^{-2}$ $s^{-1}$. Most of the irradiation tests were performed in air with heavy ions passing through a vacuum/air transition foil. Both Al foils and air were used as energy degraders to adjust the beam energy. The swift heavy-ion parameters in the experiments are listed in Table 1 [9, 11–13]. Five kinds of heavy ions were used for DUT irradiation. Both the LET and range values were calculated by using SRIM 2013 (in Table 1). Although the HI-13 beams had inferior energy, the thicknesses of all upstream multilayers could still be penetrated.

### 2.3 Pulsed-laser testing system

A picosecond pulsed laser was employed to irradiate the DUT and gather the SEU signals in a timely manner. The test system (Fig. 2) was composed of an optical module, a high-energy pulse laser (with 1064-nm center wavelength and 25-ps pulse width), an optical polarization, and an attenuation module. Laser pulse polarization and attenuation were achieved by combining filters that attenuated the beam to fixed amounts with polarizer/half-waveplate continuous variation. An energy monitoring and controlling system with operating software was used to control the energy changes from 1 nJ to 30 nJ. A camera was needed to image the surface of the DUT and focused laser spot, making it possible to identify which sensitive node was being tested by the pulsed laser [14]. Additionally, a three-dimensional mobile platform provided the DUT positional parameters directly in order to retain the accuracy and stability during the experiment.

In the test, a topside irradiation mode with a 5 μm spot size was selected. Owing to the large feature size and low metal coverage rate in the DUT, incident photons from the topside easily reached the SEE sensitive nodes unhindered by metal interconnects or packaging [14]. Given the very small sizes of the sensitive nodes in the DUT, a stage with a step size of $< 1$ μm should be used. The pulsed-laser parameters illustrated above can effectively characterize the SEE both spatially and temporally.

## 3 Experimental results and analysis

This section presents the heavy-ion and pulsed-laser irradiation results. Owing to the thin/thick gate oxide anti-fuse process in the memory cell and the guard ring structures in the CMOS circuits, no SEL phenomena occurred in the DUT during the entire process. $p^+$ and $n^+$ guard rings were used to prevent the influence of minority carriers by keeping the wells within their appropriate potentials. It can be concluded that the DUTs possessed a strong capacity to resist SEL. Other testing results are presented as follows. First, the SEU cross sections with dynamic bit errors and address errors distinguished in the heavy-ion vertical incidence irradiation under different LET values were illustrated. Second, the effect of irradiation hardness techniques and the hard error influence was characterized and analyzed. Then, laser mapping results revealed the sensitive area, which was verified by additional $^{181}$Ta irradiation.

### 3.1 Heavy-ion SEU test

DUTs with 8-Mbit and 16-Mbit configurations were irradiated by five swift heavy ions, and the SEU data were collected. SEUs in the DUTs mainly contained dynamic bit errors and address errors, as shown in Table 2. For the advanced thin/thick gate oxide anti-fuse process in the DUT memory block, each unit exhibited a high anti-irradiation performance. However, a few dynamic bit errors in the readout during irradiation were observed. This may have resulted from dynamic upsets in the output buffer,

**Table 1** Experimental heavy-ion types and energies

| Accelerator | Ion species | Initial energy (MeV) | *LET* (MeV $cm^2$ $mg^{-1}$) | Range in silicon (μm) |
|---|---|---|---|---|
| HI-13 | $^{28}$Si | 135.0 | 9.3 | 50.7 |
| | $^{35}$Cl | 150.0 | 13.4 | 42.8 |
| HIRFL | $^{86}$Kr | 2150.0 | 19.6 | 343.2 |
| | $^{209}$Bi | 1985.5 | 91.1 | 101.4 |
| | $^{181}$Ta | 2262.5 | 80.5 | 99.3 |

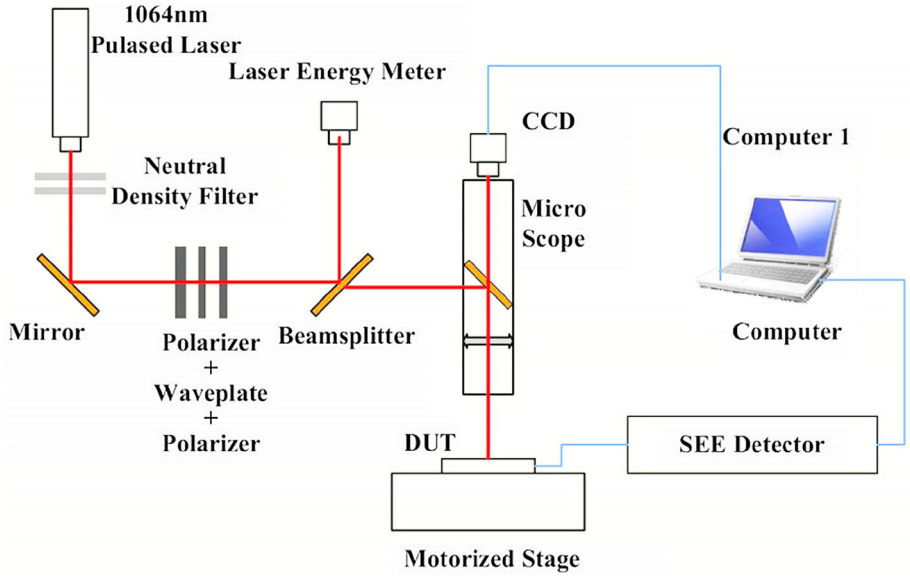


**Fig. 2** (Color online) SEE laser testing system

**Table 2** Distinguishing between dynamic bit errors and address errors

| Error type | Error address |
|---|---|
| NO Error | – |
| Dynamic Bit Error 07c0e3 | prom: 67e6 sram: 6766 **Dynamic Bit Error** |
| NO Error | – |
| NO Error | – |
| NO Error | – |
| Address Error 002d08 | prom: 0010 sram: 1110 **Address Error** |
| Address Error 002d09 | prom: 0000 sram: 1312 **Address Error** |
| Address Error 002d0a | prom: 0000 sram: 1514 **Address Error** |
| Address Error 002d0b | prom: 0000 sram: 1716 **Address Error** |
| Address Error 002d0c | prom: 0100 sram: 1918 **Address Error** |
| ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ Several Clock Cycles | |
| NO Error | – |

thus making a single-bit error appear. The internal address counter in the DUT stores the information of the current address and any increments or resets. If a counter is upset, a subsequent reading will proceed from the new (upset) address [2]. The address encoded in the DUT identifies the current location. Apparently, most upsets in the counter may be owing to a single bit, but long-lasting multiple-bit upsets were also seen.

Based on the recorded upset data, a Weibull function (as given below) was used to fit the heavy-ion-induced SEU data.

$$\sigma = \begin{cases} \sigma_{\text{sat}} \left\{ 1 - \exp\left[ -\left( \dfrac{LET - LET_{\text{th}}}{w} \right)^{s} \right] \right\} & LET \geq LET_{\text{th}} \\ 0 & LET \leq LET_{\text{th}} \end{cases}, \quad (1)$$

where $\sigma$ (cm$^2$ bit$^{-1}$) is the SEU cross section in terms, $\sigma_{\text{sat}}$ (cm$^2$ bit$^{-1}$) is the saturation upset cross section, $LET_{\text{th}}$ is the minimum LET to observe an error in the stored data, $s$ is a dimensionless exponent, and $w$ is a width parameter. The total gathered errors are shown in Fig. 3.

For 8-Mbit PROMs, the LET threshold of the SEU is about 9.2 MeV cm$^2$ mg$^{-1}$, with the saturation cross section at $1.0 \times 10^{-5}$ cm$^2$ device$^{-1}$. The 16-Mbit PROM has a similar LET threshold (9.6 MeV cm$^2$ mg$^{-1}$) but a higher saturation cross section at $2.7 \times 10^{-5}$ cm$^2$ device$^{-1}$. The thresholds of two DUTs are almost identical, while the 16-Mbit PROM has a larger interaction area for charge deposition and collection, causing the probability for the interactions between heavy ions and the sensitive volumes in 16-Mbit PROM improved. This leads to a negligible increase in the SEU saturation cross section of the 16-Mbit PROM. However, when the saturated cross section values are normalized per bit, the two DUTs are roughly the same: $1.3 \times 10^{-12}$ cm$^2$ bit$^{-1}$ (8 Mbit) and $1.7 \times 10^{-12}$ cm$^2$ bit$^{-1}$ (16 Mbit).

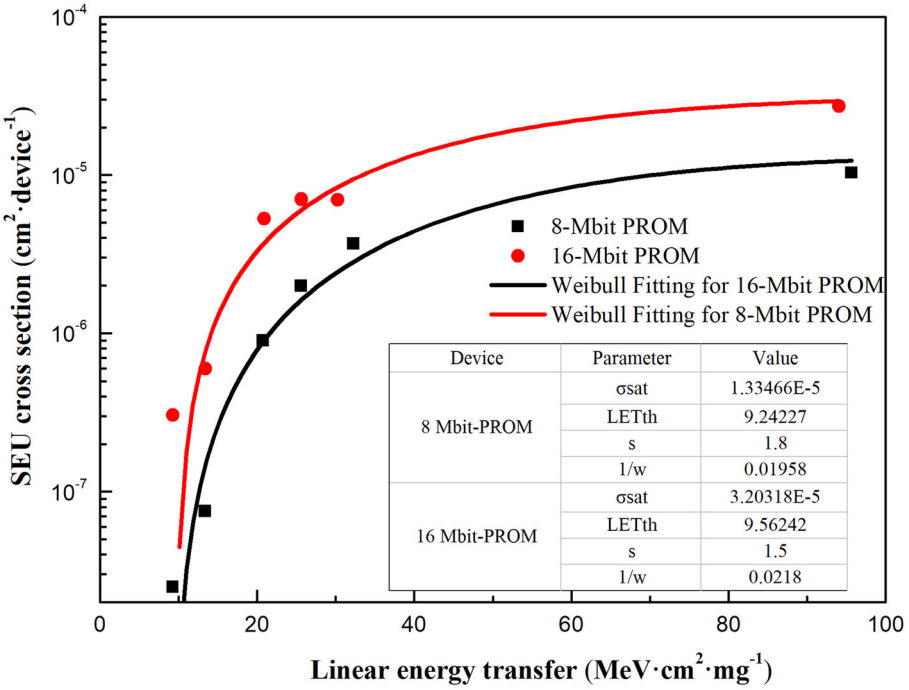


**Fig. 3** SEU cross section of total errors in 8-Mbit and 16-Mbit PROMs versus LET

Upsets in address counters and I/O pairs result from a single bit, although a few multiple-bit upsets were observed. All of the address errors were measured and fitted by a Weibull function, as shown in Fig. 4. In the figure, the LET thresholds of the 8- and 16-Mbit PROMs are approximately 21.1 MeV $cm^2$ $mg^{-1}$ and 18.1 MeV $cm^2$ $mg^{-1}$ with a saturation cross section at $9.7 \times 10^{-6}$ $cm^2$ $device^{-1}$ ($1.2 \times 10^{-12}$ $cm^2$ $bit^{-1}$) and $1.3 \times 10^{-5}$ $cm^2$ $device^{-1}$ ($8.1 \times 10^{-13}$ $cm^2$ $bit^{-1}$), respectively.

The LET thresholds of the address data are higher than those of the stored data, but they play a primary role in the SEU rates with LET values between 22.4 and 37.6 MeV $cm^2$ $mg^{-1}$. For several LET values, the rates of the address data can exceed 90%. A superior threshold may

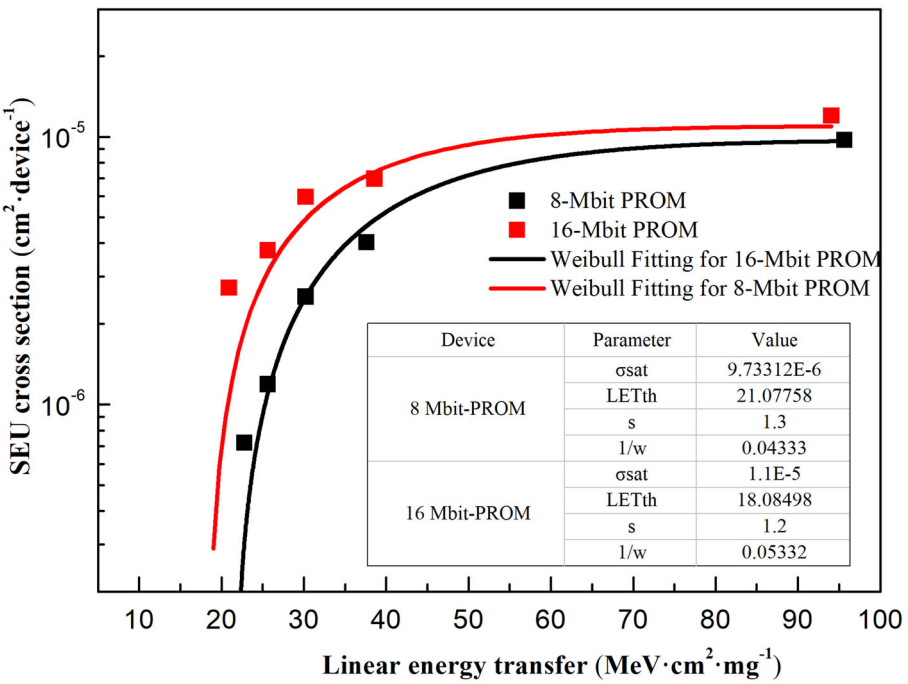


**Fig. 4** SEU cross section of 8-Mbit and 16-Mbit PROM address errors versus LET

be derived from high reinforcement in the I/O ports and the TMR structure of the address counters. Above all, large I/O ports need to deposit more charge to trigger an upset, and a large critical charge is difficult to create in low LET irradiation conditions. On the other hand, all of the address counters with basic CMOS structures have TMR consolidation. An error signal pulse introduced by the external test environment must be loaded to significant parts such as the reset sites, and it eventually passes through the voter. These restrictive conditions increase the upset threshold.

PROMs with 8-Mbit and 16-Mbit configurations adopt the same radiation hardening structure and obtain similar irradiation testing results. This shows that the sensitive circuits of these two devices are the same, and their anti-irradiation performance is mainly determined by reinforcement in the sensitive circuits. Thus, their overall anti-irradiation ability is better than that of several foreign products investigated in [1, 2]. Here, EDAC and TMR, as two main reinforcement methods, decreased the saturation cross section of the error data in the 8-Mbit PROM and 16-Mbit PROM by approximately $10^{-12}$ cm$^2$ bit$^{-1}$, indicating a good capacity to resist SEU.

The EDAC verification code adopted by the DUTs is generated by a Hamming code with 32 plus 8 structures. In irradiation experiments, the EDAC function was used continuously. According to the data stored in the memory cells and the examined algorithms designed as EDAC codes, the testing system can determine whether errors appeared and make corrections immediately. The TMR mode in the internal latch (Fig. 5) employs three logic cells to store the same data and selects the correct output by a triple modular voter circuit.

Error signals caused by heavy ions and captured by a latch or register need to satisfy three basic conditions: existence paths from the struck node to a latch or register, a proper arriving time, and a necessary profile at the latch input. Under TMR reinforcement in the latch circuits, even if an error signal is captured by the latches, there is still no guarantee that it will be transmitted to the output and pass the TMR voter.

Compared to the statistics in the heavy-ion test in Ref. [2], the TMR structure in the latch circuit can reduce the upset rates to a great extent. However, the hardened effects of the TMR and EDAC techniques are affected by the cycle time. With the error accumulations in one period, dynamic bit errors may not be corrected by a one-error-correction Hamming code and are distinguished by a triple redundant voter in time, thereby providing the error information as the output.

Additional large-fluence swift heavy-ion irradiation was used to check the program redundancy technique that existed in the 16-Mbit PROMs, which were created to enhance the reliability and decrease the influence of hard errors in memory cells. After high LET $^{209}$Bi (91.1 MeV cm$^2$ mg$^{-1}$) irradiation for over a decade of cycles (each cycle was tested with nearly $10^8$ ions), several hard errors appeared only in the 8-Mbit PROM (as shown in Table 3), although the probability was extremely low and the rates were lower than $10^{-6}$. These persistent hard errors can be interpreted as irradiation damage created by swift heavy-ion irradiation in their program area, as shown in Fig. 6.

Because of the thin and sensitive program areas in anti-fuse transistors, a large fluence of swift heavy ions can form surface roughness, ion tracks, and irreparable damage and can cause several unprogrammed cells to eventually become programmed. The experimental results revealed that an irreparable program can be created by high LET $^{209}$Bi particles, resulting in the occurrence and detection of 0-to-1 upset errors. However, taking both the space LET spectrum and the DUTs' actual working states into consideration, this hard damage may not exist over a decade in geosynchronous orbit or medium earth orbit. This means that DUTs without programming-redundant design are still suitable for general space missions. However, for long-term space missions, this reliability-enhanced design seems to be a better choice.

### 3.2 Laser SEU test

Laser mapping images with sensitive areas marked by colored points are shown in Fig. 7. The scanning energy was continuously changed from 1 nJ to 30 nJ, and the experimental manipulation was repeated to radiate the DUT in the full exposure area [15, 16]. The energy values in Fig. 7a–c indicate the laser thresholds of the power source, I/O pairs, and internal circuits, respectively, by comparing them with the schematic view of the DUT in Fig. 7d. Each mapping image is repeated at least three times.

The internal power source module in the upper right corner of Fig. 7d is the most sensitive part because the circuit around the power source is extremely difficult to reinforce. The experimental results proved the significance of this issue. In addition, the I/O pairs connected to the data output in the peripheral circuits showed errors when the laser energy was 13 nJ or higher. This corresponded to the higher threshold in the large reinforced I/O pairs of the heavy-ion test. Then, a few error data items near the center of the DUT occurred; these increased in areas and at rates where the laser energy increased.

Errors that occurred in the middle area of the DUT are reading comparison circuits. These dynamic circuits are used to store and compare the data in continuous modes. When ions or a laser strikes, the transient pulses eventually appear and propagate in the comparison circuit. When laser energy increases, the data in the latch

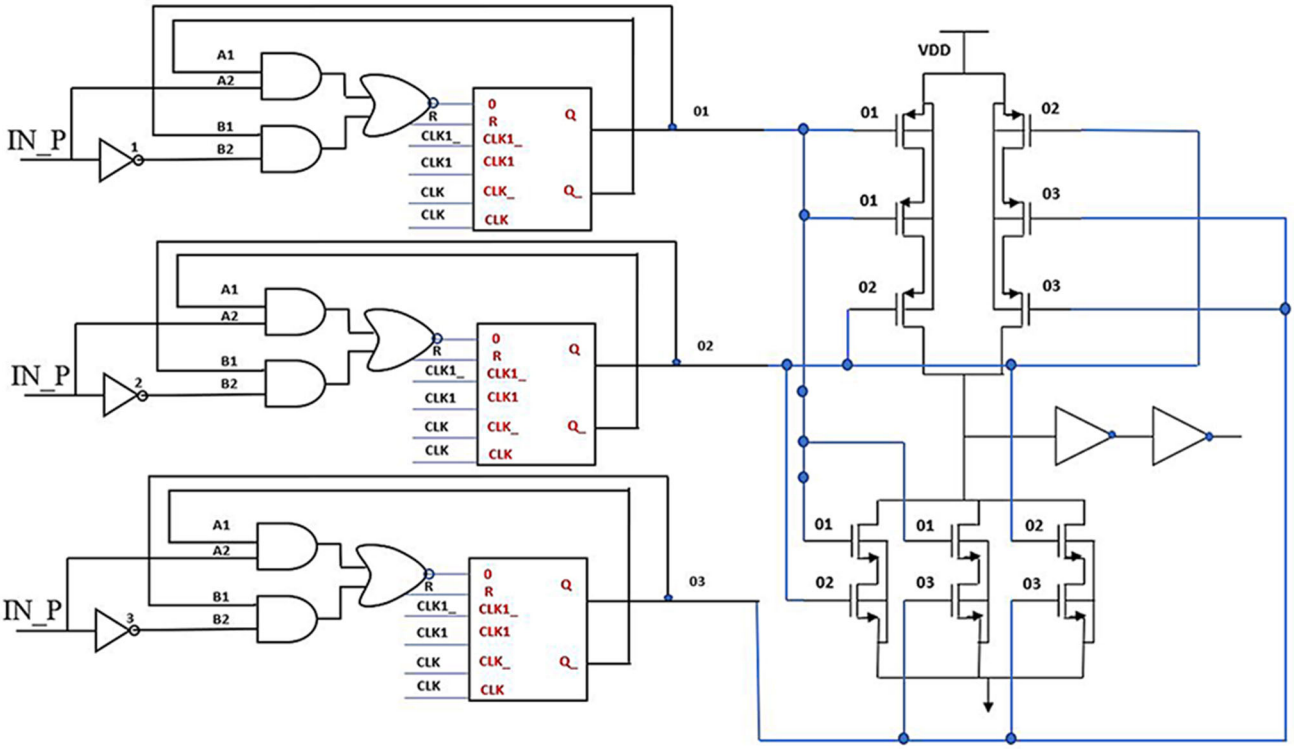


**Fig. 5** TMR structure in latch circuit

**Table 3** Extracted hard errors in 8-Mbit PROM

| Error type | Error address |
|---|---|
| Dynamic Bit Error: 0086b7 | prom: ef6e sram: 6f6e |
| No error | – |
| Dynamic Bit Error: 0086b7 | prom: ef6e sram: 6f6e |
| Dynamic Bit Error: 0086b7 | prom: ef6e sram: 6f6e |
| No error | – |

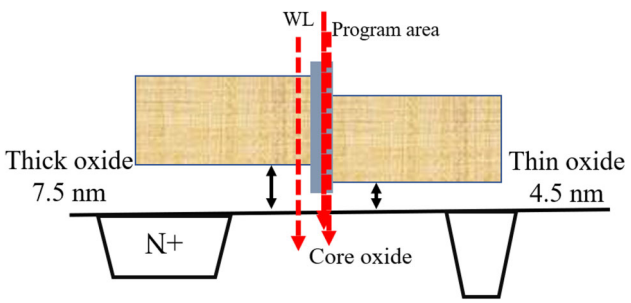


**Fig. 6** (Color online) Generation of persistent hard error in anti-fuse structure

circuits have a few errors. Nevertheless, the increased error rates and sensitive areas in the reinforcement latch circuits can be neglected.

The laser experiment verified the excellent radiation resistance of the DUT for the areas of stored data that were not very sensitive to photons, or where upsets may be detected and corrected by the EDAC code TMR voter in time. The address bits have a high SEU threshold, but when the laser energy is higher (> 8.5 nJ), error data cannot be corrected by the voter and EDAC in time owing to the surging of long-lasting and successive upsets.

The power source, I/O pairs, and peripheral circuit without hardness designs are SEU-sensitive areas revealed by laser irradiation. Using only a large-size hardness technique in the I/O pairs cannot totally prevent SEUs. Nevertheless, I/O blocks in the PROM will not be operated until the FPGA demands to be configured in an actual space environment. This takes effect under the intermittent operation working condition only when the stored information required to be transmitted rather than under the continuous working mode in the entire SEE ground test, thus sharply declining the SEU risk.

In addition, without further reinforcement in the I/O pairs, the saturated cross section of this PROM was fairly small already, which revealed its excellent antiradiation performance to satisfy space requirements.

Accelerated $^{181}$Ta ions with an energy of 12.5 MeV u$^{-1}$ were used to reexamine the pulsed-laser testing results by adding 2-mm Al foils above the internal power source on the right part of the DUT and all I/O pairs. The calculated

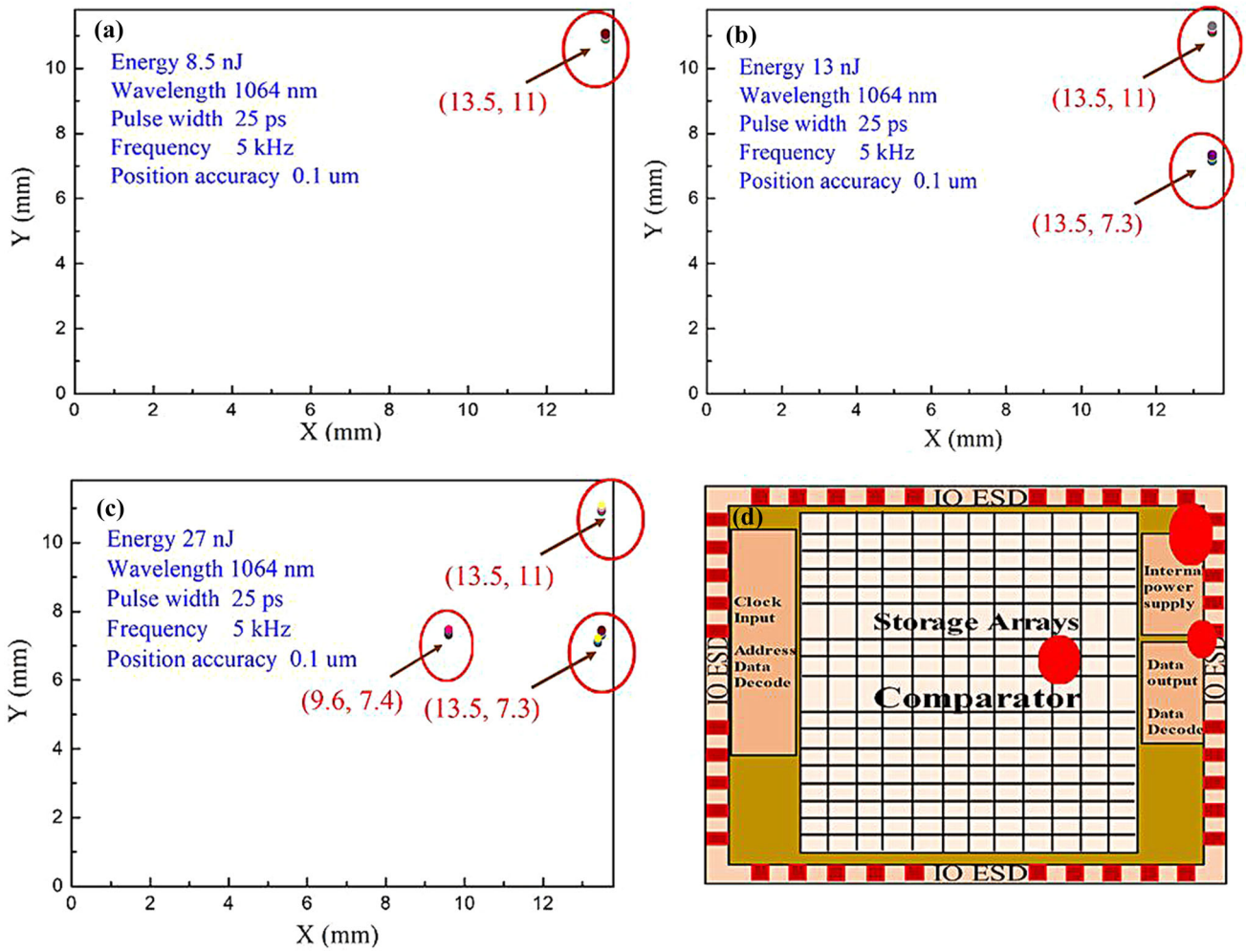


**Fig. 7** (Color online) Mapping results by picosecond pulsed laser with energy of **a** 8.5 nJ, **b** 13 nJ, **c** 27 nJ, and **d** 30 nJ (schematic view)

saturation cross section was $4.1 \times 10^{-6}$ cm$^2$ device$^{-1}$, which declined significantly when compared with its initial value ($2.7 \times 10^{-5}$ cm$^2$ device$^{-1}$). This verified that in the pulsed-laser test, the I/O pairs and internal power source contributed the majority of the upset rates.

## 4 Prediction of error rate in space applications

SEUs induced by heavy ions in space were calculated by CRÈME-96 and CRÈME-MC based on the rectangular parallelepiped (RPP) model extracted by the DUT structure [17–19]. Geosynchronous orbit, as one of the most serious environments to be influenced by heavy ions, was chosen to evaluate the upset rates of the DUT behind different Al-shielding thicknesses.

### 4.1 RPP model extraction

Simulation tools based on the Monte Carlo method were used. The effective calculation area was divided equally per bit and can be calculated by the following formula:

$$S_{\text{bit}} = \frac{S_{\text{total}}}{N}, \tag{2}$$

where $N$ is the total number of bits in the PROM. $S_{\text{total}}$ is the actual area of the DUT, and $S_{\text{bit}}$ is an equivalent single-bit area. Then, the sensitive area per bit per square centimeter ($\sigma_{\text{bit}}$) can be calculated based on the experimental results summarized above. For a 16-Mbit PROM, $\sigma_{\text{bit}}$ is $1.7 \times 10^{-12}$ cm$^2$.

Experimental heavy ions were used to irradiate the model of the PROM. Beams were set at normal incidence with a zenith angle of 0° to directly radiate the DUT model built in Fig. 8. The particle fluence was controlled at $4.0 \times 10^{10}$ ions cm$^{-2}$. Based on the device parameters and Eq. (2), the depth of the sensitive volume was set at 1 μm.

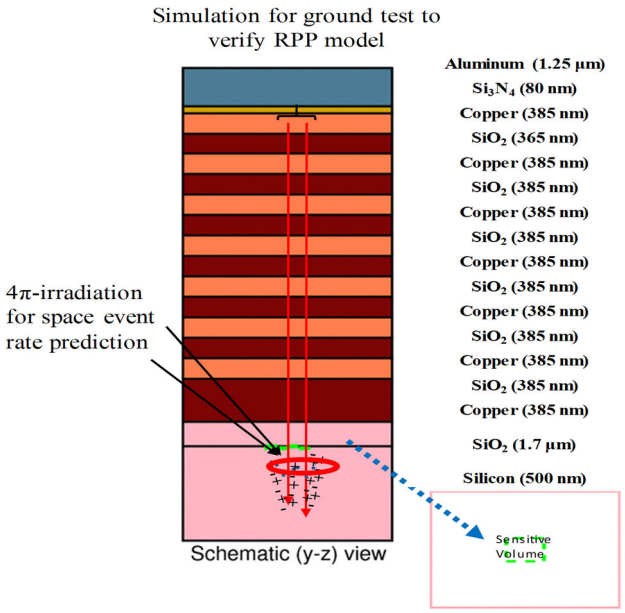


**Fig. 8** (Color online) Extracted RPP model based on ground heavy-ion test

The relation between the energy deposition in the entire sensitive volume and the cross section in space can be calculated by using the Crème-MC simulator [17–19].

The collected charge ($Q_c$) can be determined based on the results of the RPP selection and their ascertained energy deposition. For Si devices, $Q_c$ associated with an individual particle event can be calculated by a linear combination of the energy deposited in each volume ($E_i$). This can be written as [17]

$$Q_c = \frac{1\,\text{pC}}{22.5\,\text{MeV}} \sum_i \alpha_i E_i. \tag{3}$$

The depth ($H_{sv}$) of the volume is related to the critical charge ($Q_{cri}$). Since the energy to produce an electron hole pair in silicon is a constant equivalent to 3.6 eV, $Q_{cri}$ can be defined by [17]

$$Q_{cri} = 10.35 \times LET_{th} \times H_{sv}, \tag{4}$$

where $LET_{th}$ in Eq. (4) indicates the LET threshold values and $H_{sv}$ is in micrometers. By combining Eq. (3) and Eq. (4), $E_i$ can be determined [17]. It is obvious that the cross section of $^{28}$Si and $^{35}$Cl is slightly below $10^{-13}$ cm$^2$ bit$^{-1}$, which is close to the LET threshold in the heavy-ion test (around $10^{-13}$ cm$^2$ bit$^{-1}$). In addition, the cross section obtained by the simulation of $^{209}$Bi is approximately $1.9 \times 10^{-12}$ cm$^2$ bit$^{-1}$, which matches the experimental saturation cross section at $1.7 \times 10^{-12}$ cm$^2$ bit$^{-1}$. Thus, the established RPP model for space prediction fits well with the experimental results.

### 4.2 Calculation of error rates

The prediction of heavy-ion SEU rates (R) in space is accomplished based on the measured cross sections in the heavy-ion test and the ion flux in a given orbit obtained by Crème-96 [20, 21]. It is calculated by

$$R = \int_0^\infty \Phi_{\text{eff}}(LET)\sigma(LET)\text{d}LET, \tag{5}$$

where $\sigma(LET)$ is the effective cross section, i.e., it can be averaged on all solid angles (as shown in Fig. 8). The sensitive volume was irradiated by heavy ions in space from 4π solid angles. Here, $\Phi_{\text{eff}}$ is a differential ion-flux spectrum for a given shielding thickness in geosynchronous orbit in a solar maximum condition [20].

Figure 9 proves that with a shielding thickness over 3 mm, Al may provide promising results in reducing SEU rates. Based on the constructed RPP model in CRÈME-MC and the calculated $Q_{cri}$, the SEU rates caused by heavy ions in space were calculated and are shown in Fig. 10. Shielding by 10-mm Al produced a superior protection effect with a low event rate of $6.26 \times 10^{-13}$ upset bit$^{-1}$ day$^{-1}$. The calculated event rate is matched to continuous working conditions such as a ground test. This may be a few orders larger than its actual intermittent operation mode in space.

## 5 Discussion

Our experimental results in heavy-ion and pulsed-laser tests revealed the radiation-hardened performance of 8-Mbit and 16-Mbit PROMs. DUTs fabricated by the thin/thick gate oxide anti-fuse process with additional EDAC-

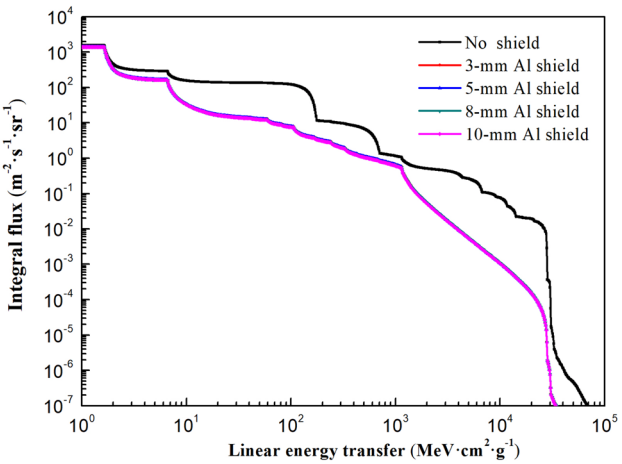


**Fig. 9** Heavy-ion energy after penetrating different shielding thicknesses of Al

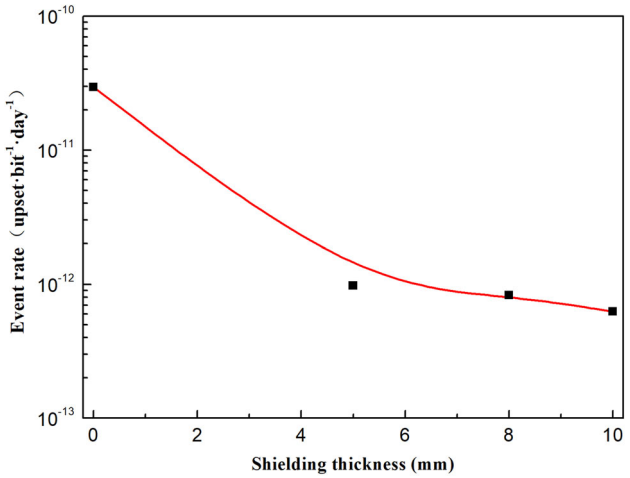


**Fig. 10** Event rate per bit per day in geosynchronous orbit versus shielding thickness of Al

and TMR-hardened design have excellent application prospects, significantly decreasing the SEU risk. In peripheral logic circuits, swift heavy ions incident to a particular sensitive node with charge deposition may generate a transient pulse. Then, the transient pulse may create upset errors, but this is mainly determined by the particles' striking positions and the arrival time of the transient pulse in circuits. The striking positions of the particles affect the pulse width and amplitude in CMOS circuits. In addition, the arrival time of a transient pulse is essential because the pulse signal may be captured by a latch or register circuits only within the rising edge of the clock. [21, 22]. Otherwise, a transient pulse may be blocked during the following clock period and eliminated by a scribing operation, or removed by special hardness techniques [22, 23]. Moreover, taking the TMR structure into consideration, even if an upset error exists in one latch, it still cannot influence the output voter results.

Additional $^{209}$Bi (1985.5 MeV) and $^{181}$Ta (2262.5 MeV) were chosen to check the programming reliability and the effectiveness of the laser test, respectively. Further, high-fluence $^{209}$Bi irradiation verified the formation and proportion of the hard errors. Irradiation damage created by swift heavy ions with high LET values can destroy anti-fuse memory units, cause irreparable damage, and finally program the unprogrammed cells.

However, the 16-Mbit PROM completely eliminated hard errors by storing a single bit in two anti-fuse memory units. This enhanced the reliability of the DUT to a great extent, especially for long-term orbiting satellites. The saturation cross section declined significantly in $^{181}$Ta irradiation when the internal power source and I/O pairs were maintained under the protection of aluminum foils. The results of $^{181}$Ta irradiation matched well with the laser test, which indicated that superior anti-irradiation performance can be achieved by hardening the power source and I/O pairs, although the upset rate for the DUT in space is extremely low.

## 6 Conclusion

The 130-nm CMOS-based thin/thick gate oxide anti-fuse PROM reinforced by EDAC and TMR techniques had an extremely low saturation cross section in heavy-ion radiation tests. Dynamic bit errors mainly caused by the dynamic upsets in the output buffer have a low LET threshold for the CMOS process, while address errors have high thresholds but long-lasting influence. The 16-Mbit PROM passed a programming reliability test with zero hard errors appearing during the high-fluence $^{209}$Bi irradiation. A laser test revealed that in the vicinity of the internal power source module and I/O ports are sensitive areas, although the large-size techniques in the I/O blocks improved their SEU thresholds. Based on an extracted RPP model, a low SEU rate in geosynchronous orbit was estimated, indicating promising space applications because of the structure and radiation hardening techniques even without additional reinforcement.

## References

1. S.M. Guertin, G.M. Swift, D. Nguyen, Single-event upset test results for the Xilinx XQ1701L PROM, in *Radiation Effects Data Workshop (REDW), 1999 IEEE* (1999), pp. 35–40. https://doi.org/10.1109/redw.1999.816054
2. J. George, G. Swift, S. Guertin et al., Heavy ion SEE testing of Xilinx One-time programmable configuration PROMs, in *Radiation Effects Data Workshop (REDW), 2004 IEEE* (2004), pp. 72–78. https://doi.org/10.1109/redw.2004.1352908
3. C.P. Han, L. Zhang, Y.P. Zou et al., Design and implementation of high reliable spaceborne reconfiguration system, in *International Conference on Electronics Information and Emergency Communication (ICEIEC), 2016 IEEE* (2016), pp. 273–277. https://doi.org/10.1109/iceiec.2016.7589737
4. S. Chiang, R. Wang, J. Chen, et al., Oxide-Nitride-Oxide antifuse reliability, in *International Reliability Physics Symposium 28th Annual Proceedings(IRPS), 1990 IEEE* (1990) pp. 186–192. https://doi.org/10.1109/relphy.1990.66084
5. O. Kim, C.J. Oh, K.S. Kim, CMOS trimming circuit based on polysilicon fusing. Electron. Lett. **34**, 355–356 (1998). https://doi.org/10.1049/el:19980320
6. E. Hamdy, J. McCollum, S.O. Chen et al., Dielectric based antifuse for logic and memory ICs, in *IEDM Technical Digest (IEDM), 1988 IEEE* (1988), pp. 786–789. https://doi.org/10.1109/iedm.1988.32929
7. X. Fan, Dissertation, University of Electronic Science and Technology of China, 2011 **(in Chinese)**
8. L. Zou, Y.L. Deng, G.X. Pei, M. Du, Research on SEU characteristics of PROM bit-cells. Comput. Meas. Control **21**, 2544–2546 (2013). https://doi.org/10.16526/j.cnki.11-4762/tp.2013.09.064. **(in Chinese)**

9. C. Geng, J. Liu, K. Xi et al., Monte Carlo evaluation of spatial multiple-bit upset sensitivity to oblique incidence. Chin. Phys. B **22**, 059501 (2013). https://doi.org/10.1088/1674-1056/22/5/059501
10. C. Geng, X.Y. Li, Y. Lin et al., Investigation single event effects characterization on configuration PROMs of FPGA induced by heavy ions. Nucl. Phys. Rev. **33**, 359–363 (2016). https://doi.org/10.11804/NuclPhysRev.33.03.358. **(in Chinese)**
11. J.L. Barth, C.S. Dyer, E.G. Stassinopoulos et al., Space, atmospheric, and terrestrial radiation environments. IEEE Trans. Nucl. Sci. **50**, 466–481 (2003). https://doi.org/10.1109/TNS.2003.813131
12. J. Liu, J.L. Duan, M.D. Hou et al., SEU ground and flight data in static random access memories. Nucl. Instrum. Methods Phys. Res., Sect. B **245**, 342–345 (2006). https://doi.org/10.1016/j.nimb.2005.11.125
13. Z.G. Zhang, J. Liu, M.D. Hou et al., Angular dependence of multiple-bit upset response in static random access memories under heavy ion irradiation. Chin. Phys. B **8**, 086102 (2013). https://doi.org/10.1088/1674-1056/22/8/086102
14. S.P. Buchner, F. Miller, V. Pouget et al., Pulsed-laser testing for single-event effects investigations. IEEE Trans. Nucl. Sci. **60**, 1852–1875 (2013). https://doi.org/10.1109/TNS.2013.2255312
15. Y.G. Jiang, G.Q. Feng, Z. Xiang et al., Pulsed laser method for SEE testing in FPGAs. Atom. Energy Sci. Technol. **46**, 582–586 (2012). https://doi.org/10.13700/j.bh.1001-5965.2013.0514. **(in Chinese)**
16. G.Q. Feng, Y.G. Jiang, Z. Xiang et al., Comparison of multi-bit upset in FPGA induced by pulsed laser and heavy ions. Atom. Energy Sci. Technol. **48**, 732–736 (2014). https://doi.org/10.7538/yzk.2014.48.S0.0732. **(in Chinese)**
17. R.A. Weller, M.H. Mendenhall, R.A. Reed et al., Monte Carlo simulation of single event effects. IEEE Trans. Nucl. Sci. **57**, 1726–1740 (2010). https://doi.org/10.1109/TNS.2010.2044807
18. A.J. Tylka, J.H. Adams, P.R. Boberg et al., CREME96: a revision of the cosmic ray effects on micro-electronics code. IEEE Trans. Nucl. Sci. **44**, 2150–2160 (1997). https://doi.org/10.1109/TNS.2012.2218831
19. M.H. Mendenhall, R.A. Weller, A probability-conserving cross-section biasing mechanism for variance reduction in Monte Carlo particle transport calculations. Nucl. Instrum. Methods A **667**, 38–43 (2012). https://doi.org/10.1016/j.nima.2011.11.084
20. E.L. Petersen, The SEU figure of merit and proton upset rate calculations. IEEE Trans. Nucl. Sci. **45**, 2550–2562 (1998). https://doi.org/10.1109/23.736497
21. J. Barak, R.A. Reed, K.A. LaBel, On the figure of merit model for SEU rate calculations. IEEE Trans. Nucl. Sci. **46**, 1504–1510 (1999). https://doi.org/10.1109/23.819114
22. P.E. Dodd, L.W. Massengill, Basic mechanisms and modeling of single-event upset in digital microelectronics. IEEE Trans. Nucl. Sci. **50**, 583–601 (2003). https://doi.org/10.1109/TNS.2003.813129
23. P. Francis, J.P. Colinge, G. Berger, Temporal analysis of SEU in SOI/GAA SRAMs. IEEE Trans. Nucl. Sci. **42**, 2127–2137 (1995). https://doi.org/10.1109/23.489263