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Heavy ion-induced MCUs in 28 nm SRAM-based FPGAs: upset proportions, classifications, and pattern shapes

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Abstract

For modern scaling devices, multiple cell upsets (MCUs) have become a major threat to high-reliability field-programmable gate array (FPGA)-based systems. Thus, both performing the worst-case irradiation tests to provide the actual MCU response of devices and proposing an effective MCU distinction method are urgently needed. In this study, high- and medium-energy heavy-ion irradiations for the configuration random-access memory of 28 nm FPGAs are performed. An MCU extraction method supported by theoretical predictions is proposed to study the MCU sizes, shapes, and frequencies in detail. Based on the extraction method, the different percentages, and orientations of the large MCUs in both the azimuth and zenith directions determine the worse irradiation response of the FPGAs. The extracted largest 9-bit MCUs indicate that high-energy heavy ions can induce more severe failures than medium-energy ones. The results show that both the use of high-energy heavy ions during MCU evaluations and effective protection for the application of high-density 28 nm FPGAs in space are extremely necessary.

Keywords FPGAs · Heavy ions · Multiple cell upsets · Extraction · Worse irradiation

1 Introduction

Static random-access memory (SRAM)-based field programmable gate arrays (FPGAs) are sensitive to radiation-induced single event upsets (SEUs) [1–3]. Single-bit upsets (SBUs), as a well-known effect in FPGAs, occur when single particles (such as heavy ions) deposit energy that exceeds the critical charge in single memory cells. However, in modern advanced process technologies, owing to the smaller area and decreased critical charge of transistors, single particles can affect more than one memory cell simultaneously in the physical layout to generate clustered errors, that is, multiple cell upsets (MCUs) [4]. MCUs have become a catastrophic factor that threatens the safety of FPGAs applied in aerospace missions [5, 6]. Particularly, as the feature size of transistors continuously shrinks to the nanoscale, the proportion of MCUs in FPGAs increases dramatically [7, 8]. When MCUs occur in critical configuration RAMs (CRAMs) that control the entire functions of FPGAs, an abnormal state of the on-orbit systems may occur. Therefore, it is crucial to study the impact of MCU on CRAMs to guarantee the safety of critical electronic components in aerospace missions.

Although fault injections can simulate MCU information, irradiation tests are closer to the actual space environment to study the influences of MCUs on circuits because of the actual ion-induced charge generation process [9, 10]. Heavy ions of various energies are typically utilized in irradiation tests. Therefore, the required energy range must be

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specified. The medium-energy range is defined as 1–10 MeV per nucleon [11]. Beams that reach 10–100 MeV/n and 5–150 GeV/n are considered to be high-energy and ultra-high-energy beams, respectively [12]. For ground-based accelerator evaluations, medium-energy heavy-ion irradiation under vertical incidence is typically utilized. However, high-energy heavy ions existing in the space environment [13] have recently promoted the MCU investigations. The results in [14] showed that compared to medium-energy heavy ions, ultra-high-energy heavy ions with the same ionization ability can induce larger-scale MCUs in 28 nm FPGAs, indicating that the energy of heavy ions significantly affects the size of MCUs, but the ionization ability was relatively small (3.7 MeV/(mg/cm^2)). Because high-energy heavy ions have considerably higher ionization ability than ultra-high-energy heavy ions, they would generate larger proportions and sizes of MCUs that significantly threaten the safety of FPGAs. Additionally, based on medium-energy heavy ions, the tilted irradiation tests in [15] demonstrated more serious MCU effects on nanoscale FPGAs. When considering tilted high-energy heavy ions, considerably larger MCUs may appear in nanoscale FPGAs, compared with medium-energy heavy ions with a higher ionization ability. Unfortunately, no study has been conducted on irradiation tests with high-energy heavy ions to demonstrate the worse MCU effects of the high ionization ability on 28 nm FPGAs. Although [16] performed more serious irradiation tests in different directions with medium-energy heavy ions for Kintex-7 FPGAs, detailed MCU patterns and sizes were not provided. Hence, systematic studies including worse MCU characterizations and effective MCU discriminations are necessary to determine the more serious MCU influences and support the process of radiation-hardened designs.

In contrast to the standard modular structures of SRAMs, the complex layout arrangement of CRAMs with different sensitive node distances may induce diverse MCU features, leading to an accurate distinction between MCUs in CRAMs much difficult [17]. Additionally, the complicated interleaved schemes used to mitigate MCUs make it unfeasible to discriminate between MCUs [18]. Although the distinction between the SBU and MCU data can be achieved by controlling the flux of the ion beams and performing microbeam scanning [19, 20], the time and cost consumed are non-negligible. Additionally, there exists an inexpensive method named "statistical analysis," which classifies MCUs by XORing flipped pairs, but it is not appropriate for the modular separated FPGA architecture [21, 22]. Besides, [17] presented a statistical MCU extraction from FPGAs according to the abnormous relationships between upset addresses, but it lacked theoretical support. In [23], although the authors extracted MCUs with the help of a Monte Carlo simulation and theoretical prediction, there was no further explanation of the relationships between upsets satisfied when MCUs were extracted. Therefore, there is an urgent need to propose a convincing and effective MCU extraction method for representative FPGA-based systems to determine the impact of MCUs.

In this study, systematic heavy-ion irradiations on 28 nm SRAM-based FPGAs were performed to determine the worse MCU response of devices, and an improved MCU extraction method was proposed to study the MCU features. With detailed MCU information, we identified the worse impacts of high-energy heavy ions than medium-energy ones and different MCU features under various irradiation conditions. This paper is organized as follows. In Sect. 2, we introduce the irradiated devices, test system, and experimental information. The detailed MCU extraction process, results, and discussion are presented in Sect. 3. Finally, we present our conclusions.

2 Experimental setup

2.1 Devices under test

High-performance Xilinx XC7K325T FPGAs were chosen as the devices under test (DUTs), which have been widely used in cost-sensitive applications to achieve high-end connectivity, bandwidth, and signal processing capability [24]. A 28 nm bulk silicon process with a high-k metal gate was utilized in the DUT. All programmable routings or switches in the DUTs are controlled by CRAMs, which can achieve complex functions to satisfy the requirements of different space missions after rational configurations.

The CRAMs are formally arranged into "frames" (rows) and "bits" (columns) for Xilinx families, and the specific functions can be realized by configuring the customized bitstreams generated by the Vivado software into the CRAM part. The DUT has 22,546 frames (including seven dummy frames) and 72,846,048 bits (i.e., 101 32-bit words for each frame). All frame data can be read back and compared with the golden bitstream, and the error data, as well as the logical locations (frame# and bit#), are extracted after the comparisons.

2.2 Test system

A test system was developed to capture the irradiation vectors of the DUT. The test system consisted mainly of a motherboard and daughterboard. The DUT on the daughterboard was irradiated during the tests. The main control FPGA soldered on the motherboard was responsible for reading the contents of the DUT, transmitting commands, and identifying functional failures. Both the motherboard and daughterboard need a 12 V DC power supply. The high-speed interface was utilized to connect the two boards, and

the configuration time was less than 0.5 ms. Additionally, we designed software on the host computer to control the test system. After the beam is turned off, the motherboard executes bitstream comparisons and uploads the results to the main control FPGA. The detailed information on the upsets and types of hard errors were captured and saved as log files for further analysis.

2.3 Irradiation parameters

Irradiation tests were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL) at the Institute of Modern Physics, Chinese Academy of Sciences. High-energy ^{78}Kr ions and medium-energy ^{129}Xe ions were used to irradiate the DUT. The ^{129}Xe ions were accelerated using a sector separator cyclotron. The ^{78}Kr ions were from the cooling storage ring (CSR), and this was the first available high-energy single-event experiment of the CSR heavy-ion accelerator. To meet the ion range requirement, the substrate of the DUT was thinned to approximately 50 μm.

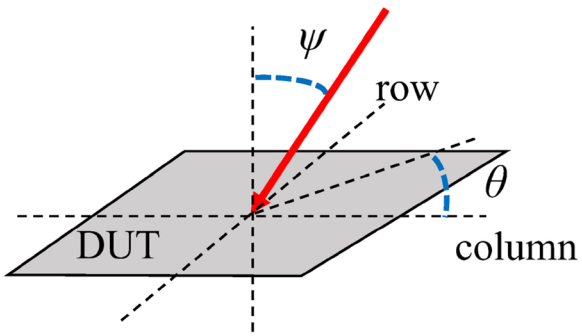


Fig. 1 Ion beam with azimuth angle θ and zenith angle ψ incident on the DUT surface

It should be noted that the tests were performed under the nominal temperature (20 ℃). The standard core voltage of the DUT was 1.0 V. Moreover, several aluminum foils were used to achieve multiple linear energy transfer (LET) values. The DUT was fixed on a 5-dimensional platform to change its position and rotate the tilts (θ, ψ), as shown in Fig. 1.

Additionally, many testing trials were performed at a low fluence to reduce the occurrence of MCUs induced by several heavy ions, and the detailed explanations are presented in the next section. The experimental conditions and parameters are listed in Table 1. In both the ^{78}Kr and ^{129}Xe experiments, the number of upsets in each run was controlled at less than 400. Any trials with upsets exceeding 400 were discarded from the dataset. In our testing scheme, static modes were used to radiate the DUT. The static modes start with the configuration of our DUT with a bitstream and then with the beam on. During the radiation tests, the circuits inside the DUT do not work because the static modes do not rely on clock driving. Heavy ions only affect the configuration functionality of the circuits, that is, the CRAM cells. After reaching the preset heavy-ion fluence, the beam was turned off, and the radiated and golden bitstreams were compared to identify the upsets. To date, only a single testing trial has been completed. Before the next static trial, the configuration must be restarted to restore the functionality of the DUT. By repeating this operation, multiple trial results were obtained. Static modes have the benefit of preventing undesired occurrence of functional errors and mitigating the rates of burst errors during the reconfiguration process [25], which improves the efficiency of our MCU extractions. The heavy-ion testing platform of HIRFL can achieve accurate flux as well as control the preset fluence.

Table 1 Detailed experimental information

Heavy ion	Energy (MeV) in active regions	LET(MeV/(mg/cm^2)) in active regions	Range (μm) in silicon	Angle (θ, ψ)	Flux (ions/(cm^2 s))	Upsets	Number of trials
^{78}Kr	3348.0	13.3	699.4	(0°, 0°)	730	3662	15
				(0°, 30°)	715	5468	22
	1653.0	20.8	246.4	(0°, 0°)	640	4771	18
				(0°, 30°)	440	4232	22
	793.0	31.0	98.2	(0°, 0°)	310	3164	17
				(0°, 30°)	350	3628	14
^{129}Xe	771.0	66.5	58.4	(90°, 0°)	200	1721	7
				(90°, 30°)	150	1590	7
				(90°, 45°)	160	1211	5
				(0°, 30°)	100	1482	7
				(30°, 30°)	100	3392	15
				(45°, 30°)	80	898	4

3 Results and discussion

During data analysis, several consecutive upsets of almost 16 bits in the same frame were observed and were identified as being caused by micro-functional failures [17]. Because these abnormal upsets interfere with the real MCU results, before the MCU extraction, they were removed from the collected upset data.

3.1 FMCUs

"False MCUs (FMCUs)", typically defined as MCUs induced by several particles rather than single ones, significantly affect the determination of correct MCU results. Therefore, before irradiation tests, it is necessary to propose a test principle that prevents the occurrence of FMCUs as much as possible.

According to [26], the probability of FMCUs can be

$$P_k(n,p)(\text{collision}) \approx 1 - \exp\left(-\frac{p(p-1)(2k-1)}{2n}\right). \quad (1)$$

In this equation, p is the number of upsets in each radiation test, k is the collision range, which was set to 32 (the length of a word in the Kintex-7 FPGA), and n is the number of bits in one specific memory. It can be observed that the probability of the FMCUs depends only on the number of upsets. Equation (1) shows that when there are a few upsets, the probability of the FMCUs can be sufficiently low. This is the reason why we separated our tests into multiple rounds as illustrated in Sect. 2.3. A more specific approach to obtain as few upsets as possible is to control the fluence of the heavy ions in each round of the radiation test. In the analysis of the upsets, the minimum and maximum numbers of upsets were 86 and 272, respectively. Based on Eq. (1), the minimum and maximum probabilities of the FMCUs in our radiation designs were approximately 0.3% and 3.0%, respectively, which proved the statistical property of this calculation.

3.2 MCU extraction

MCUs can be extracted by determining the differences in the positional relationships between the actual upset data and theoretical predictions. Therefore, the first important task was to create a predictive model. In this model, only SBUs exist, referred to as only-SBU systems [22], where the relationships between single upsets show a specific frequency distribution. However, the actual radiation violates the above assumptions because heavy ions can affect more than one cell simultaneously to generate the MCUs. The charge-sharing effect is another essential factor in MCU generation. More specifically, because MCUs are generated by single particles, there must be a certain rule between the upsets because it is determined by the statistical spatial and temporal nature of the ion beams and the specific MCU sensitivities of devices. Hence, the relationships between the real upsets must exhibit different frequencies from the theoretical only-SBU predictions; that is, the relationships appearing more frequently than the predictive ones can be identified as being caused by the MCUs.

Before constructing the predictive model, we first assume that there is a rectangular space of length X and width Y, and this space contains N elements, where N is equal to $X \times Y$. The elements in this space can be included by a set named R, where $R = \{A_1, A_2, A_3, \ldots, A_N\}$, and A_i is the i_{th} arbitrary element in R. Each element A_i in this space has its unique coordinate representation, labelled as (x_i, y_i) formally like a position in the X–Y plane. Hence, the coordinates of all elements in this space can be defined from the bottom left (1, 1) to the top right corner (X, Y).

In fact, there are specific relationships between the elements in this space. To identify the relationships between them without repetition and loss, we should first organize them in increasing order, and the principle is given by.

$A_i = (x_i, y_i), A_j = (x_j, y_j)$ and

if

$x_i < x_j$

or

$x_i = x_j$ and $y_i < y_j$

then $A_i < A_j$.

Subtraction can be used to determine the unique relationships among these elements. Hence, we can formally obtain several offsets, such as $(\Delta x, \Delta y)$. We then define a set named the offset set (OS) that contains all these offsets. It is worth noting that the Δx of each offset in the OS must be equal to or greater than 0, and the contents of the OS can be determined by

$$\text{OS} = \{(A_j - A_i) | A_i < A_j, A_i, A_j \in R\}. \quad (2)$$

To illustrate the subtraction process more clearly, we used a 2×3 array named S as an example. The coordinates of all the six elements and their subtracted offsets are listed in Table 2.

In the example illustrated above, X and Y are selected as 2 and 3, respectively. We then return to the Kintex-7 FPGA. As illustrated in Sect. 2.1, the CRAM bits are arranged in rows and columns in the Xilinx FPGAs. Therefore, in the N-bit CRAM space mentioned above, X and Y were 22,539 and 3232, respectively. Using Eq. (2), we can infer that the

Table 2 Results of the calculated offsets in a 2×3 array

S	(1, 1)	(1, 2)	(1, 3)	(2, 1)	(2, 2)	(2, 3)
(1, 1)		(0, 1)	(0, 2)	(1, 0)	(1, 1)	(1, 2)
(1, 2)			(0, 1)	(1, –1)	(1, 0)	(1, 1)
(1, 3)				(1, –2)	(1, –1)	(1, 0)
(2, 1)					(0, 1)	(0, 2)
(2, 2)						(0, 1)
(2, 3)						

ranges of x and y of the offset (x, y) are from 0 to 22,538 and -3231 to 3231, respectively, and they are both integers. The offsets (x, y) in the N-bit CRAM space are arbitrary combinations of all x and y within the above ranges; however, these offsets must meet the increasing order rules exactly at $x=0$. Thereby, there is a total of $N(N\text{-}1)/2$ offsets with repetition. For an arbitrary offset (x, y), the probability that it appears in the OS is determined by

$$p(x,y) = \frac{2}{N(N-1)}(Y - |y|)(X - x). \tag{3}$$

After each radiation test, N_u upsets ($N_u << N$) were observed. A set named U_n containing all the N_u upsets with increasing order is then created to calculate the new OS, and the next significant step is to determine the predictive frequency distributions. For these N_u upsets in an individual radiation trial, the number of offsets in the new OS is given by (4) to obtain N_{OS}.

$$N_{OS} = 1/2 \cdot N_u \cdot \left(N_u - 1\right) \tag{4}$$

In our predictive model, because we assume that these upsets are irrelevant to each other, the probability of an arbitrary offset (x, y) appearing m times in the total N_{OS} trials can be calculated using the classical binomial probability distribution

$$p_{x,y}^{N_{OS}}(m) = \binom{N_{OS}}{m} \cdot p(x,y)^m \cdot (1 - p(x,y))^{(N_{OS}-m)}. \tag{5}$$

Then, under this prediction, the number of offsets that appear m times in N_{OS} trials is simply the sum of all the conditions; that is, the probability of each offset (x, y) multiplied by its appearing times $N_{x,y}$ in the new OS.

$$N(m) = \sum_{(x,y)} N_{x,y} p_{x,y}^{N_{OS}}(m) \tag{6}$$

To ensure that the extracted MCUs have more than 95% confidence, we set 0.05 as the maximum value of Eq. (6) to determine the cut-down value, labelled as m.

We illustrate the above extraction process using an example. In the case of the Kintex-7 FPGA, based on Eq. (2) and Eq. (3), we can first determine the probabilities of all offsets {(0, 1), (0, 2), …, (0, 3231), (1, −3231), (1, −3230), …, (1, 3231), (2, –3231),…, (22,538, 3231)}. After a single radiation test, we observed 214 upsets, and the N_{OS} was 22,791. According to Eq. (5), we can determine the probabilities of all the actual obtained offsets (those offsets are absolutely the subset of the above offsets) that are in the new OS appearing m times. We then sum the above probabilities of all offsets multiplied by their appearing times in an individual test round to determine the number of offsets appearing m times. By letting the left-hand term in Eq. (6) be equal to 0.05, we obtain a cut-down value. In this case, the cut-down value m was 2.9. Thus far, we have completed the single process of obtaining one cut-down value. Then, a question arises: How do we identify the offsets that are caused by MCUs? The answer is that offsets that emerge more frequently than 2.9 times are extracted as true offsets that are induced by MCUs, because they violate the irrelevance between upsets, that is, only-SBU theoretical prediction. By repeating the above process, we obtain many cut-down values, which rely on the number of rounds of the static tests performed. However, if we carry out too many rounds of tests, the calculation and comparison processes are bound to be huge. To address this problem, two rules are defined below to make MCU extraction more convenient and accurate.

A. *Cut down rule*

This rule helps extract the MCUs more conveniently. Because of the specific physical layout arrangement and the MCU sensitivities of devices, after the cut-down values of all the testing rounds are confirmed, these values and the occurrence numbers of the same offsets obtained from multiple rounds can be added separately to create a histogram containing all the possible offsets. Taking two rounds of radiation tests as an example, their cut-down values are calculated to be 2.9 and 3.1, and offset (1, 0) occurs 30 and 39 times, respectively. We can then add them separately. Finally, the cut-down value is 6.0, and the offset (1, 0) occurs 69 times. Based on this rule, the offset results of the ^{78}Kr and ^{129}Xe irradiations are shown in Fig. 2. Offsets that occurred above the cut down (dashed red and blue lines in Fig. 2) were identi-

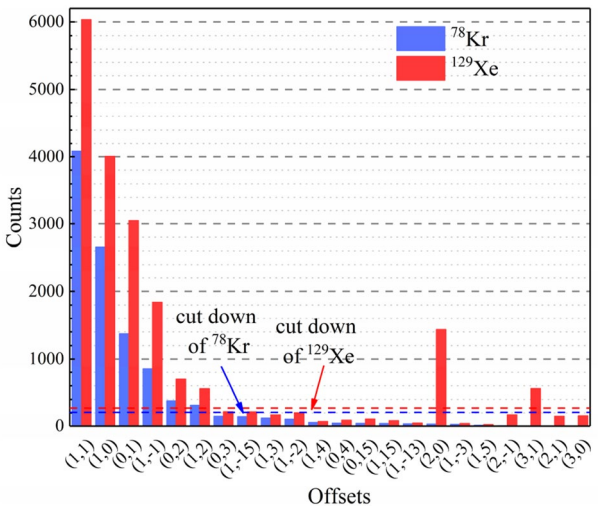


Fig. 2 (Color online) Results of offsets caused by ^{78}Kr and ^{129}Xe ions

Table 3 Statistical offset results for the occurrence numbers of logical upset offsets that do not exceed the cut-down value

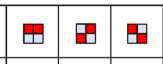
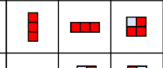
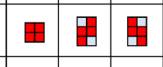
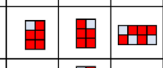
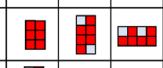
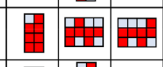
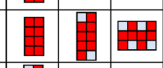
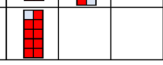
Shape	Max number of occurrences in each run	Offset values
	2	(0, 1), (1, 0), (1, −1), (1, −2)
	4	(0, 1), (1, −1), (1, 0), (1, 1), (2, −1), (2, 0), (3, 0), (3, 1)
	2	(0, 1), (0, 2), (1, −1), (1, 0), (1, 1), (1, 2), (1, 3)
	3	(0, 1), (1, −1), (1, 0), (1, 1), (1, 2), (2, −1), (2, 0), (2, 1), (3, 1), (3, 2)
	2	(0, 1), (0, 2), (0, 3), (1, −2), (1, −1), (1, 0), (1, 1), (1, 2), (1, 3), (1, 4)
	2	(0, 1), (0, 2), (0, 3), (1, −3), (1, −2), (1, −1), (1, 0), (1, 1), (1, 2), (1, 3)
	2	(0, 1), (0, 2), (0, 3), (0, 4), (1, −3), (1, −2), (1, −1), (1, 0), (1, 1), (1, 2), (1, 3)

fied to discriminate the MCUs, and the remaining offsets were discarded.

B. *Repetition rule*

Here, we define another principle called the repetition rule. This rule is available for offsets that do not exceed the cut-down value. For example, during the analysis, some exclusive MCUs presented in Table 3 appeared at least 2 times in an individual round. Because the probability of the same-shape MCUs appearing more than two times can be calculated to be very low, the offsets marked in red were reconsidered and added to the true offset group. This rule helped recover anomalous offsets that were not in the OS, as confirmed by the cut down rule.

Table 4 Logical sizes and shapes of different MCUs

2-bit MCU	
3-bit MCU	
4-bit MCU	
5-bit MCU	
6-bit MCU	
7-bit MCU	
8-bit MCU	
9-bit MCU	

MCU extraction begins with the construction of 2-bit MCUs; then, the larger MCUs need to be further identified based on the 2-bit MCU results by determining if the offsets between them are included in the confirmed OS. This procedure is iteratively performed until the offsets of the maximum MCUs go against the OS.

3.3 Results analysis

Figure 3 shows the detailed SBU and MCU results of the ^{78}Kr and ^{129}Xe irradiation tests. For the ^{78}Kr ions, the cross-sections of the SBUs and MCUs were almost the same. However, the MCUs dominated the ^{129}Xe ion-induced upsets, which demonstrated a high-energy deposition ability and a strong charge sharing effect of the ^{129}Xe ions. Moreover, for both tests, significant increases in the cross-sections of the angular irradiations were observed, indicating that the different ion trajectories can affect the MCU characteristics of the 28 nm SRAM-based FPGAs.

Based on Fig. 2 and Table 3, the extracted logical sizes and shapes of the MCUs are presented in Table 4. We obtained diverse (up to 9-bit) MCU patterns based on the selection of the worst irradiation parameters; these MCU data can support an effective radiation hardening process under a harsh space environment. It is important to note that, because of the statistical distribution nature presented in this paper, this method can be applied to arbitrary memory-based devices. If other types of FPGAs are irradiated, the MCU results can be easily obtained by changing X and Y in Eq. (3). For the same generation of Xilinx FPGAs, owing to the same process technologies, the MCU information presented in Table 4 can be directly used to distinguish the MCU-induced cross-sections and failures.

The percentages of MCUs of different sizes are presented in Fig. 4a (for ^{78} Kr ions) and Fig. 4b (for ^{129}Xe ions). It is clear that for the high LET ^{129}Xe ions, approximately 60% MCUs were the major problem for aerospace

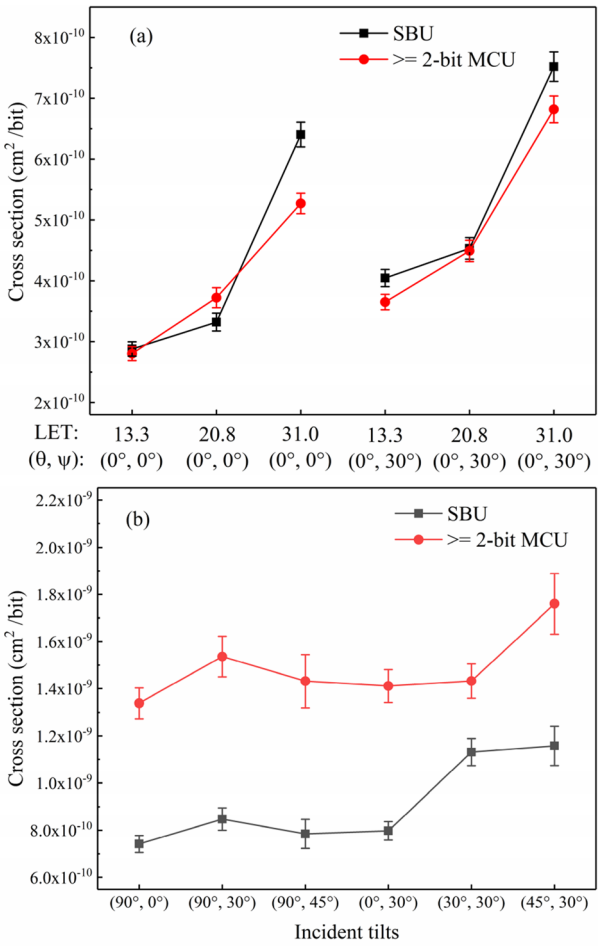


Fig. 3 (Color online) Detailed SBU and MCU results of **a** ^{78}Kr ion and **b** ^{129}Xe ion irradiation

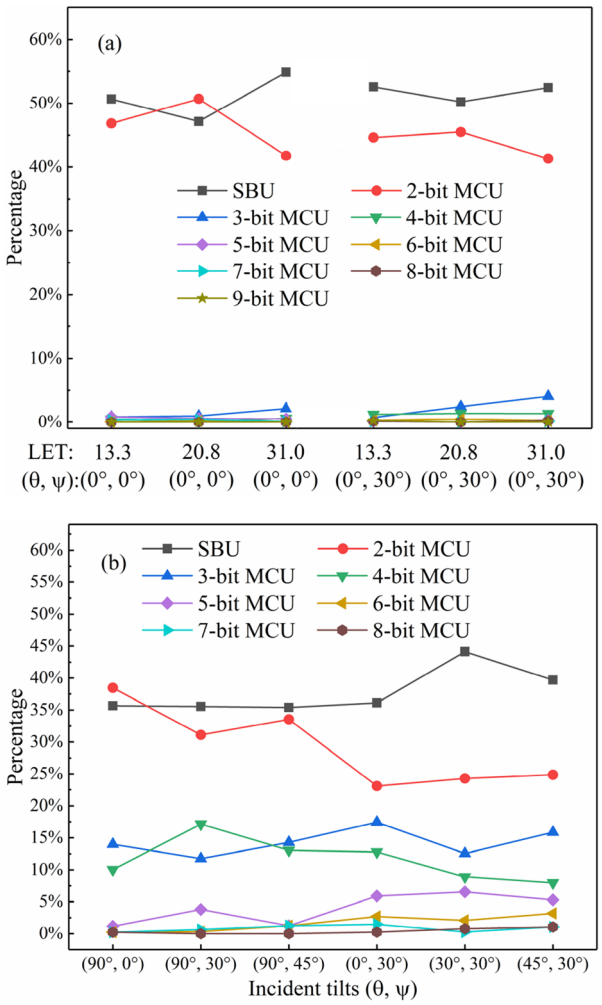


Fig. 4 (Color online) Percentages and sizes of MCUs induced by **a** ^{78}Kr ions and **b** ^{129}Xe ions

electronic systems. In Figs. 4a, b, an apparent percentage dependence of the large (more than 3-bit) MCUs on the LET and tilts was observed, and the good consistency indicated that the MCU distinction method is suitable for high-density FPGAs. Under the same LET, all large offsets (i.e., large MCUs) were generated under tilted incidence, which also proved the effectiveness of the MCU extraction method.

Additionally, for the ^{129}Xe ion irradiation, 7-bit MCUs were observed in the (90°, 30°) directions; however, under the (0°, 30°) incidence, the offset (1, 4) helped identify the largest 8-bit MCUs. For θ or ψ varying from 0° to 45°, the percentages of the largest MCUs increased by 5–6 times, demonstrating that there are indeed different layout distances in the different directional irradiations. Moreover, large (more than 4-bit) MCUs appeared more frequently when ψ was equal to 30°, which identified worse tilted irradiation effects. The MCU results verified the impacts of the different sensitive region arrangements on the extracted MCU orientations, and the discrepancies of the cross-sections in different incident directions must be considered to obtain the worse and more accurate MCU responses.

Although the SBUs and 2-bit MCUs occupied almost the entire ^{78}Kr upset dataset, when the LET was 13.3 MeV/(mg/cm^2) and the tilt was (0°, 30°), 9-bit MCUs were observed twice in an individual irradiation round. Compared with the maximum 8-bit MCUs found in the ^{129}Xe tests with the same (0°, 30°) incidence, the ^{78}Kr ion-induced larger MCUs revealed that although the high-energy heavy ions have a much smaller LET, the generated charges can still exceed the critical charge of the 28 nm FPGAs. Therefore, the ^{78}Kr ions have more severe effects than the ^{129}Xe ions, even with a considerably higher LET.

In fact, heavy-ion energy has a significant effect on MCUs. During the interaction of heavy ions with devices, a region formally like a cylinder, called the ionization track, is created along the path of heavy-ion incidence to deposit energy in the memory cells. There are two important

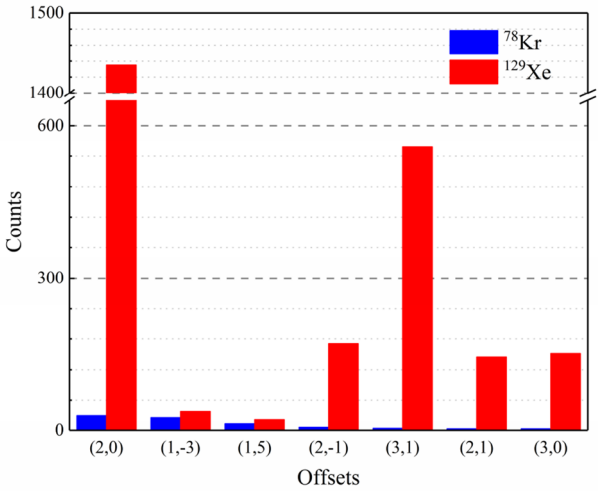


Fig. 5 (Color online) Count comparison of offsets between ^{78}Kr and ^{129}Xe ions, we zoomed in on the right part of Fig. 2

parameters in this region. One is the radius, which identifies the range that the heavy ions can affect, and the other is the density of electron–hole pairs inside the ionization track, which determines the collected charge. Any cells within this track will be upset once their collected charge is equal to or greater than the critical charge. As reported in [27], heavy ions with higher energies have wider ionization tracks; this is because they can transfer more energy to the target atoms by the direct ionization process. These secondary atoms have higher kinetic energy that affects the subsequent atoms, finally generating a wider ionization track. In our testing scheme, because the ^{78}Kr ions at the LET of 13.3 MeV/(mg/cm^2) had considerably higher energy than the ^{129}Xe ions, their wider ionization track can affect more cells. However, it should be noted that compared to the ^{129}Xe ions, the density of the electron–hole pairs inside the ionization track of the ^{78}Kr ions is lower. This is because the ^{78}Kr ions have a smaller LET (LET corresponds to the density of the electron–hole pairs). Therefore, the ^{78}Kr ions have a smaller probability of inducing cells to be upset exactly at the edge of the ionization track, which exceeds the critical charge of the 28 nm technology. However, in modern scaling devices, because the critical charge of cells is sufficiently low, these cells are more prone to be upset to generate large MCUs, which is the reason why we observed the largest 9-bit MCUs. Therefore, to avoid underestimating the MCU sensitivity, high-energy heavy ions are necessary for the evaluation of advanced devices.

We further compared the offset counts between the ^{78}Kr and ^{129}Xe ions in Fig. 2 and 5 to better understand the more serious influences of high-energy heavy ions. As shown in Fig. 2, the number of offsets (1, 1), (1, 0), (0, 1), (1, –1), (0, 2), and (1, 2) exceeded the separate cut-down values for

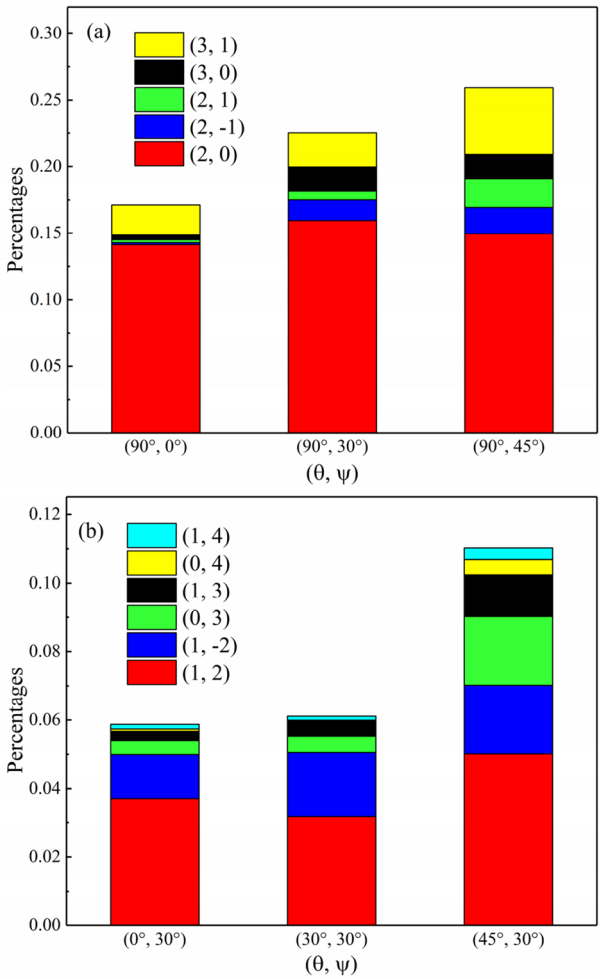


Fig. 6 (Color online) Percentages of large offsets at incidences of **a** $\theta = 90°$ and **b** $\psi = 30°$ in ^{129}Xe radiation tests

both the ^{78}Kr and ^{129}Xe heavy ions. Although the number of offsets of the ^{78}Kr irradiation was less than that of the ^{129}Xe ions, except for (2, 0), (2, −1), (2, 1), (3, 0), and (3, 1); the worse effects of the ^{78}Kr ions were determined by finding a comparable number of offsets to the ^{129}Xe ions.

In Fig. 5, the offsets (2, 0), (2, −1), (2, 1), (3, 0), and (3, 1) of the ^{129}Xe ions appeared more frequently than those of the ^{78}Kr ions. To determine the causes of this phenomenon, Fig. 6a illustrates the percentages of the large lateral offsets of the ^{129}Xe radiation tests at various tilts. It can be observed that the offset (2, 0) percentages were almost the same (approximately 15%) for all the conditions, indicating that the ^{129}Xe ions can simultaneously affect cells with a logically lateral distance of 3. Additionally, as ψ increased, the remaining offsets appeared more frequently, proving that large lateral offsets were indeed induced by $\theta = 90°$. Because we only irradiated our DUT with high-energy heavy ions in the $\theta = 0°$ direction, these large lateral offsets rarely occurred.

When radiating the DUT in various θ directions, a similar conclusion can be made from Fig. 6b; that is, the increased azimuth angles can induce larger offset percentages in the longitudinal orientation. When comparing the offset distances between (90°, 30°) and (0°, 30°) in Fig. 6, the largest offset (1, 4) revealed the worst MCU sensitivities when θ was equal to 0°, which is in good agreement with the largest 8-bit MCUs found in the ^{129}Xe radiation tests at (0°, 30°). The offsets in the longitude were larger than those in the lateral direction, demonstrating that the word direction was more sensitive than that between words.

As mentioned above, because irradiations under $\theta = 0°$ can cause the largest longitudinal offsets, the numbers of offsets (1, 2), (1, −2), (0, 3), (1, 3), (0, 4), and (1, 4) of the ^{78}Kr data were almost the same as that of the ^{129}Xe ions. It can be inferred that high-energy heavy ions in the rotated θ directions generate larger MCUs (more than 9-bit) by creating larger lateral offsets.

For modern scaling devices, the energy, LET, tilts, and irradiation directions are becoming serious issues in irradiation evaluations. Under tilted incidence, it is predicted that, as the ionization ability of high-energy heavy ions increases, the sizes and proportions of the MCUs will dramatically increase, which will seriously affect the function of FPGA-based on-orbit systems, which must be considered. Additionally, based on the worse 9-bit MCUs observed in the high-energy tests, high-energy heavy ions are recommended to fully characterize the MCUs during ground-based accelerator radiation tests. With the help of the general MCU distinction methods, more serious MCU impacts were accurately determined according to the worse irradiation evaluation. Moreover, as illustrated in Fig. 6, the selection of various directional evaluation schemes affects both the OS content and MCU features owing to the different ion energy transfer trajectories. Therefore, diverse MCUs in different directions should also be considered by hardening designers.

4 Conclusion

In this study, systematic medium-energy ^{129}Xe and high-energy ^{78}Kr ion tests under different irradiation directions were performed to evaluate the negative effects of MCU. Additionally, the MCU extraction and classification of the 28 nm SRAM-based FPGAs were successfully proposed, and the detailed MCU shapes, sizes, and frequencies were presented.

Based on the statistical MCU identification methods, offsets that did not match the predictive model were extracted to construct the MCUs. Some offsets that appeared to be less than the cut-down value were further determined by checking whether the MCUs appeared more than 2 times. A restriction of less than 0.05 in Eq. (6) enables the MCU extraction method to achieve more than 95% confidence. The detailed SBU, MCU results, and extracted large offsets revealed and demonstrated the worse sensitivity differences (offset orientations) in different irradiation tilts and directions, and further identified the 9-bit MCUs caused by the negative impacts of high-energy heavy ions on the 28 nm FPGAs. Therefore, the use of high-energy heavy ions to evaluate scaling devices for the worse MCU sensitivities was necessary.

Worse radiation evaluations and detailed MCU extractions are indispensable for preapplied digital circuits in harsh space environments. The worse MCU data and detailed analysis presented in this paper can be used to perform targeted hardened strategies to mitigate destructive MCUs and further control soft error rates.

Author contributions All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by Shuai Gao, Xin-Yu Li and Ze He. The first draft of the manuscript was written by Shuai Gao and Chang Cai, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

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