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Offset-free DC-coupled analog frontend circuit for high-dynamic-range signals

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Abstract The analog frontend (AFE) coupling circuit is a crucial processing element for data acquisition systems based on analog-to-digital converters (ADCs). Currently, high-speed and high-resolution ADCs are predominantly designed with differential input stages. Conventional high-speed ADC drivers are mainly AC-coupled by employing transformers (Baluns) or fully differential amplifiers (FDAs) with blocking capacitors. However, the results of this study indicate that a certain degree of DC offset error exists and manifests itself as the baseline error in the presence of power dividers connecting several DC-coupled channels that implement high-dynamic-range (HDR) signal conditioning. The study involves a theoretical analysis and explanation of the baseline offset error. The offset error can potentially lead to unexpected out-of-range issues for sampling devices, including high-speed ADCs and switched capacitor array ASICs. High-performance FDAs are adopted, and an offset-free DC-coupled AFE circuit is proposed to address the aforementioned issue using two-stage amplification and a resistive attenuator. The proposed methodology is verified via circuit simulations and hardware design. Thus, the baseline offset problem can be accurately solved using the proposed circuit by minimizing the neglectable error. The proposed circuit facilitates improvements in the high-precision measurement of HDR signals in many nuclear physics experiments and some applications in the DC-coupling scheme with FDAs involving resistive power dividers.

Keywords Offset-free · DC-coupled · Two-stage amplification · Resistive attenuator · High-dynamic-range

1 Introduction

Recently, high-speed digitizers or data acquisition systems have been widely used to record individual signals in nuclear and particle physics experiments. The analog frontend (AFE) circuit is a crucial processing element for data acquisition systems and is based on either high-speed analog-to-digital converters (ADCs) or switched capacitor arrays (SCA). High-speed and high-resolution sampling devices (ADCs and SCAs) are predominantly designed with differential input stages owing to their excellent noise rejection [1]. Conventional coupling circuits are mainly AC-coupled, employing transformers (Baluns) [2–4] or fully differential amplifiers (FDAs) with blocking capacitors [5–7].

Previous studies in the field of AFE design for high-speed data acquisition mainly focused on AC-coupling [2, 4–6, 8–12], whereas some designs used the DC-coupled circuit with FDAs to achieve wide-band AFE [13, 14]. However, there is a paucity of studies on the potential baseline error that results from the nonzero common-mode voltage in the presence of resistive power dividers connecting adjacent channels. In the high-precision measurement of high-dynamic-range (HDR) signals in some nuclear and particle physics experiments, conventional AFE adopts different sets of power dividers and attenuators to cover a wide dynamic range [15, 16]. Therefore, the

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offset issue can negatively affect measurement accuracy in the connection scheme.

Therefore, this study highlights the offset issue that results from the resistive power divider connecting several DC-coupled channels via FDAs. Additionally, this study proposes a new methodology to address the offset issue using the processing circuit.

2 Background theory

The "split-range scheme" referred in the study corresponds to a conventional technique to receive HDR signals. For example, in the two-split scheme, the HDR signal is initially split to two parallel paths by a power divider and then attenuated to different ranges by individual attenuating factors A_1 and A_2, as shown in Fig. 1. Operational amplifiers correspond to typical ADC drivers to implement essential signal conditioning.

a. Resistive power dividers The aim of the study is to achieve DC-coupled AFE, and thus resistive devices are satisfactory. To split the wide range of the input signal, a resistive power divider that serves as a splitter in Fig. 1 is employed to replicate signals. In the design, the reflection coefficients correspond to critical parameters to characterize the isolation of the resistive power dividers.

b. Resistive attenuators In the split-range scheme, a simple "π" attenuator, as shown in Fig. 2, can function in different input-range selections using appropriate resistors. The corresponding values of R_A and R_B are calculated based on Eq. (1), where A denotes the attenuating factor.

$$R_A = Z \cdot \frac{A^2 - 1}{2A} \qquad R_B = Z \cdot \frac{A + 1}{A - 1} \tag{1}$$

c. Single-ended-to-differential (SE-DE) conversion Most real-world signals are single-ended, and a typical schematic is presented to illustrate SE-DE conversion based on an FDA in Fig. 3 [17]. To ensure balanced feedback factors and impedance matching, the accurate value of each corresponding resistor is calculated based on [18]. The study emphasizes the nonzero common-mode voltage V_{OCM} in differential signal design and processing via an FDA.

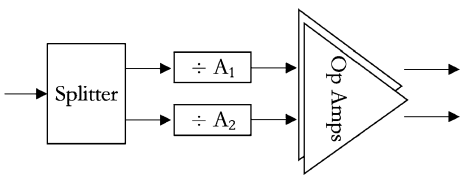

Fig. 1 Typical split-range scheme to cover HDR signals in AFE design

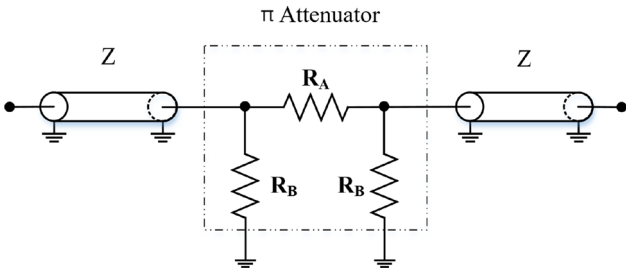

Fig. 2 Balanced "π" attenuator termination to the transmission line with characteristic impedance Z

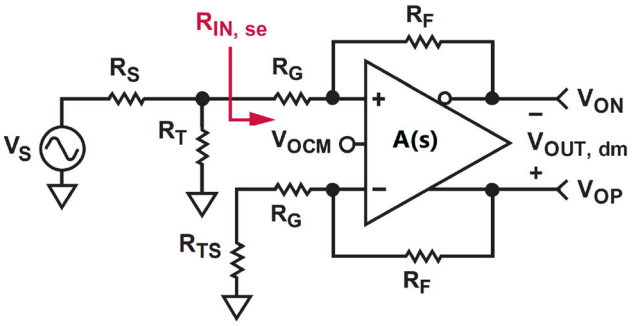

Fig. 3 Schematic for SE-DE conversion using an FDA in analog signal conditioning

3 Model and analysis

Based on the background theory described above, this section analyzes the generation of the baseline error in the split-range scheme via DC-coupled one-stage amplification using an FDA. Figure 4 provides an overview of the connection scheme of the signal generator, power divider, and two signal acquisition channels (CHA and CHB). All the discrete components in the signal path are resistive to satisfy the DC-coupling requirement.

a. DC Offset voltage resulting from V_{OCM} When there is zero input, the differential output voltages V_{ON} and V_{OP}, as shown in Fig. 4, correspond to V_{OCM}. After imposing the input signal, the resulting output signal is equivalently treated as a differential-mode component superimposed by V_{OCM}. In principle, the DC component V_{OCM} at the differential output terminals is always fed back to the input ports (A node and B node denoted in Fig. 4) based on voltage division rule, and thus the offset voltage V_{off} is expressed in Eq. (2).

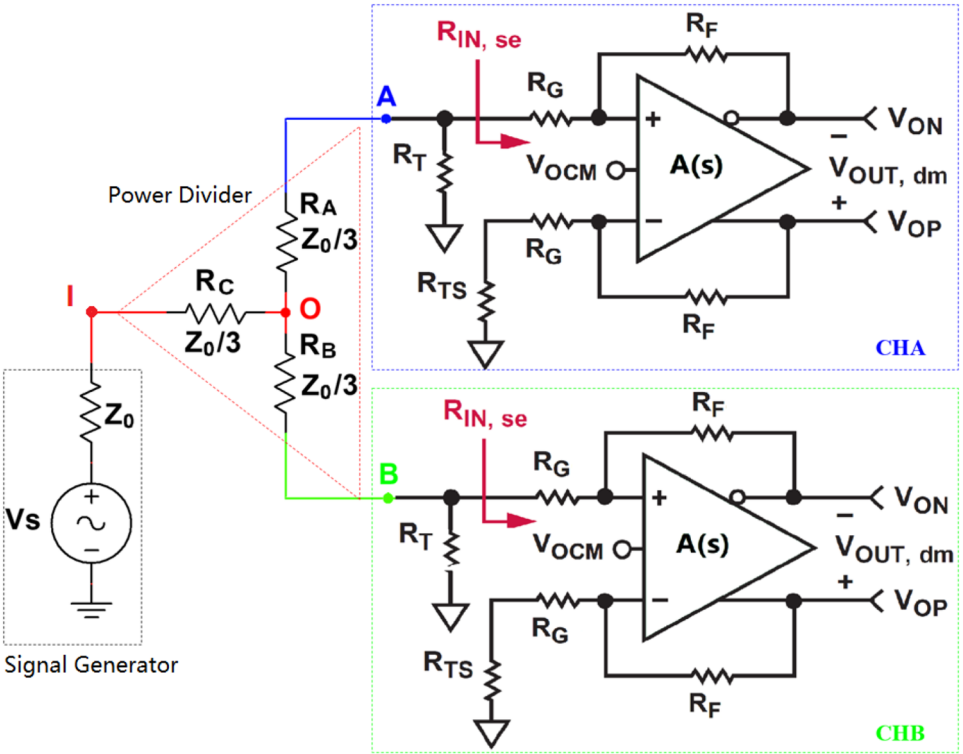

Fig. 4 Illustration of baseline error for adjacent channels in DC-coupled circuits using FDAs in split-range scheme

$$V_{\text{off}} = \frac{R_{\text{TS}}}{R_{\text{TS}} + R_{\text{G}} + R_{\text{F}}} V_{\text{OCM}} \tag{2}$$

The study emphasizes the self-consistency of the circuit in Fig. 3 and does not lead to any additional error resulting from V_{OCM} in the normal case.

b. Baseline error generation due to resistive power divider The power divider in Fig. 4 corresponds to a 1-to-2 splitter and the reflection coefficient $S_{ij} = 1/2$. Hence, we can express the level of the baseline error ΔV_{off} as in (3).

$$\Delta V_{\text{off}} = \frac{1}{2} V_{\text{off}} = \frac{1}{2} \frac{R_{\text{TS}}}{R_{\text{TS}} + R_{\text{G}} + R_{\text{F}}} V_{\text{OCM}} \tag{3}$$

To provide a quick description of the magnitude of the baseline error, the study considered the typical FDA LMH5401 from Texas Instruments as an example to illustrate the degree of error level at the input terminal based on Eq. (3) via calculating the corresponding parameters in Tab.2 from [19]. We selected a parameter $\eta = \Delta V_{\text{off}}/V_{\text{OCM}}$ to represent the level of the offset error, as shown in Table 1. The table shows the value of η to be as high as 10%. This indicates that for a typical 1.25-V common-mode voltage, the value of ΔV_{off} at the input terminal can correspond to 125 mV. As shown in Table 1, the generated baseline error should not be ignored in high-precision measurements.

Table 1 Examples of $\eta = \Delta V_{\text{off}}/V_{\text{OCM}}$ for LMH5401

A_V(V/V)	$R_{\text{G}}(\Omega)$	$R_{\text{F}}(\Omega)$	$R_{\text{TS}}(\Omega)$	η(%)
2	90.9	200	30.1	4.7
4	22.6	152	43.9	10.0
8	12.1	250	48.3	7.8
10	9.76	300	47.8	6.7

c. Discussion Figure 4 presents the case when the external signal is connected to the positive input terminal. The offset voltage does not change even if the signal is connected to the negative input terminal given that V_{OCM} is common to the two differential output terminals. Therefore, the two connection schemes lead to the same voltage although the reverse polarity offset error is observed at the output port in the presence of a resistive power divider. Despite the self-consistency of the circuit, a certain constant output voltage manifests itself as an undesirable baseline error in the split-range scheme.

Unfortunately, the offset error potentially leads to an unexpected out-of-range issue for sampling devices including high-speed ADCs and SCA ASICs. This can constitute a significant issue for any applications with DC-

coupled FDAs serving as the input driver and involving resistive power dividers.

Traditionally, offset error is assessed within the scope of one single channel due to the intrinsic character of amplifier devices. However, there is paucity of studies on the offset error due to the resistive power divider in the split-range scheme.

4 Methodology and verifications

4.1 Proposed methodology

The analysis in the previous section indicated that the baseline error was primarily caused by the nonzero V_{OCM} in the split-range scheme. A direct method to address the issue involves blocking the DC voltage with a series of capacitors although the technique is not satisfactory for the DC-coupling requirement. Given the background, the current study proposed a processing circuit based on two-stage amplification and resistive attenuator to minimize the offset voltage V_{off} (and the baseline error ΔV_{off}) such that it is neglectable. This corresponds to the meaning of the term "offset-free" in the study.

At the first amplification stage, the common-mode voltage V_{OCM} is set to zero, i.e., connected to the ground. The zero V_{OCM} value does cause offset voltage in principle, and SE-DE conversion is implemented at this stage. The second stage shifts differential signals to the optimal input range of the ADC or SCA ASIC. Hence, at this stage, the V_{OCM} should be normally set to nonzero. The DC path connecting the input terminal remains unblocked, and this still creates a minimized version of the offset voltage. Nevertheless, the resistive attenuator presented in Fig. 1 with a suitable A further attenuates the offset voltage such that it is neglectable; and the following section demonstrates this point.

4.2 Verification by simulations

To verify the proposed methodology, four types of simulation circuits with different structure characters were constructed in the NI Multisim environment. The structure characters and simulation objectives of the four types of circuits (referred to (a-1), (a-2) and (b-1), (b-2) circuits) are listed in Table 2. Specifically, the (a-1) circuit was used to identify the baseline offset error in the split-range scheme while (b-2) circuit was created to verify the proposed circuit. Additionally, (a-2) and (b-1) circuits were constructed to demonstrate the single effect of an additional amplification stage and attenuator, respectively. For the purpose of simplicity, the attenuating factors A_1 and A_2, as shown in Fig. 1, were both set to 4.

The simulations highlight the comparison of results from the virtual oscilloscope XSC1 in Fig. 5 between one independent separated signal channel and another channel in the split-range scheme via a resistive power divider. For the purposes of brevity, the former is hereafter termed as single scheme, while the latter is termed as split scheme. The simulation schematic for (b-2) circuit (the proposed circuit in the study) in single and split schemes is shown in Fig. 5, and (a-1), (a-2), and (b-1) simulation schematics are determined by modifying this circuit.

a. Zero-input condition First, a zero input was applied to identify the baseline offset error and compare the levels of the error among the four types of circuits. The simulation results are shown in Fig. 6A. In each of the four sub-figures, the blue and red plots denote the results of the single and split schemes, respectively. The difference between the red plot and blue plot in the first three sub-figures indicates that output signals were superimposed by offset errors in the split scheme. However, a clear trend of decreases in the offset error level was observed from (a-1) to (b-2) circuit. The baseline error of the proposed (b-2) circuit was minimized as significantly small. In the zero-input condition, the output signal actually corresponded to the baseline, and the baseline should theoretically be at the zero level. To quantitatively describe the decreasing trend for the four types of circuits, the baseline errors are summarized and presented in the second column of Table 3. The results confirmed that the baseline error was minimized from 486.7 mV to a sufficiently low value of 0.6 mV. Additionally, the baseline value from (a-1) to (a-2) was observed as minimized to 1/16, thereby verifying the significant effects of the resistive attenuator.

b. Nonzero-input condition Second, a sinusoidal signal was applied to conduct simulations on nonzero-input condition. The amplitude of the sinusoidal signal in the

Table 2 Type codes and objectives of the four types of simulation circuits with different structure characters

Type code	Structure characters	Objectives
(a-1)	One stage, without attenuator	Identifying the baseline offset error
(a-2)	One stage, with attenuator	Verifying the function of attenuator
(b-1)	Two stages, without attenuator	Verifying the function of two-stage amplification
(b-2)	Two stages, with attenuator	Verifying the proposed circuit

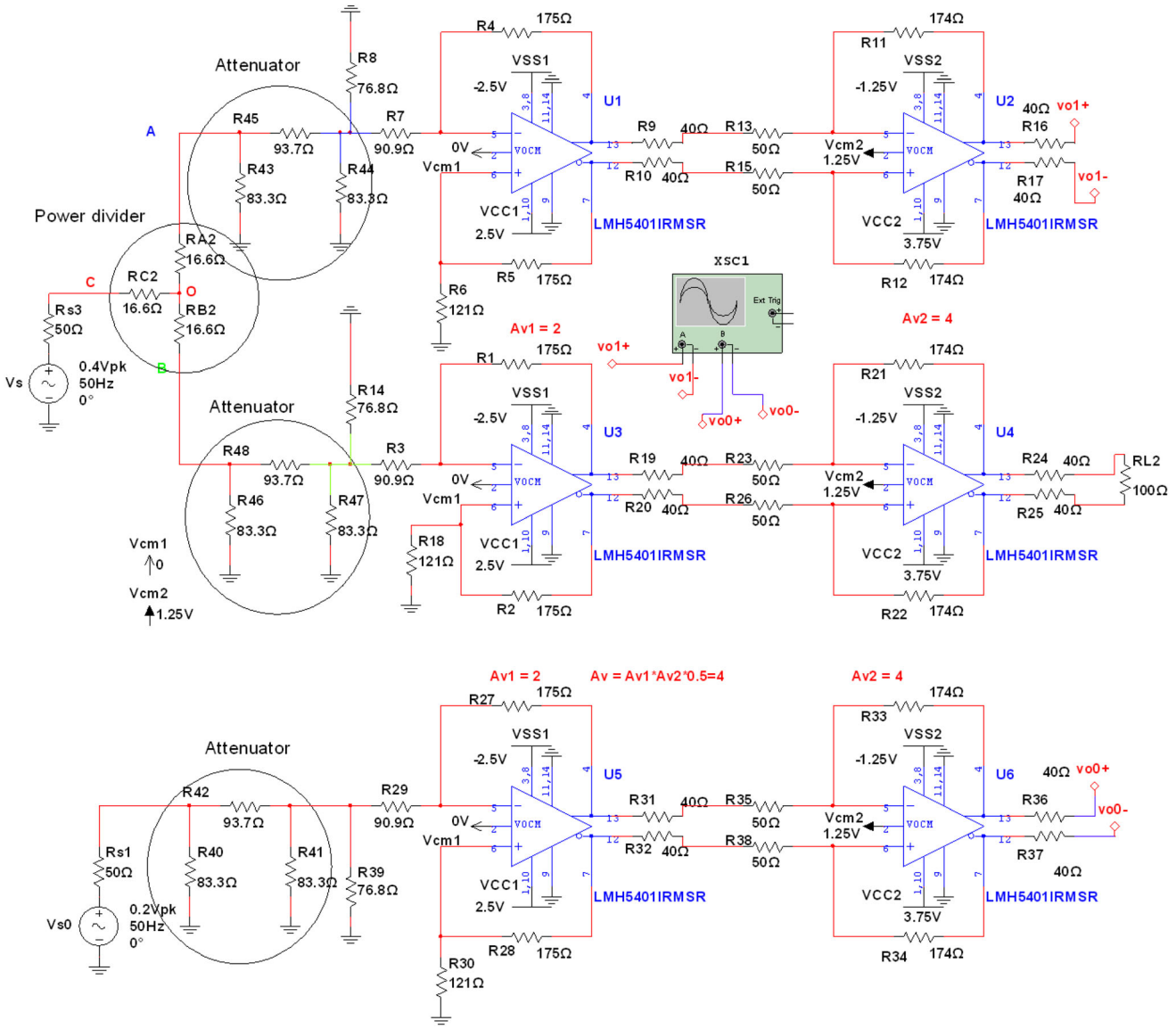

Fig. 5 Simulation schematic in NI Multisim environment for the proposed (b-2) circuit: (vo1+ − vo1-) denotes the output of the split scheme in the presence of power divider, while (vo0+ − vo0-) denotes the single scheme in the normal case as a comparison. The (a-1), (a-2), and (b-1) simulation schematics are determined by modifying this circuit

respective circuit was configured to achieve a theoretical peak-to-peak value corresponding to 200 mV for the differential signal observed at the output ports. The simulation results are organized and shown in Fig. 6B. Evidently, the baseline errors in the four types of circuits were significantly reduced. On the nonzero-input condition, the baseline errors calculated from the simulation results are statistically summarized in the third column of Table 3. Furthermore, a comparison of the "Baseline error1" with "Baseline error2" in Table 3 revealed that the baseline error exhibited a fixed pattern based on circuit parameters including relevant resistors and connecting schemes.

4.3 Verification by hardware design

Based on the proposed (b-2) circuit, this study designed a PXI 3U board in the Cadence environment. The hardware-design block diagram of the proposed AFE circuit is shown in Fig. 7. With respect to the FDAs, LMH5401 devices were employed as the ADC driver to implement two-stage amplification and signal conditioning.

A photograph of the PXI 3U board with four channels is presented in Fig. 8. (The baseline shift, trigger generation and distribution, and PXI configuration modules were also designed on the board. However, the parts are not within

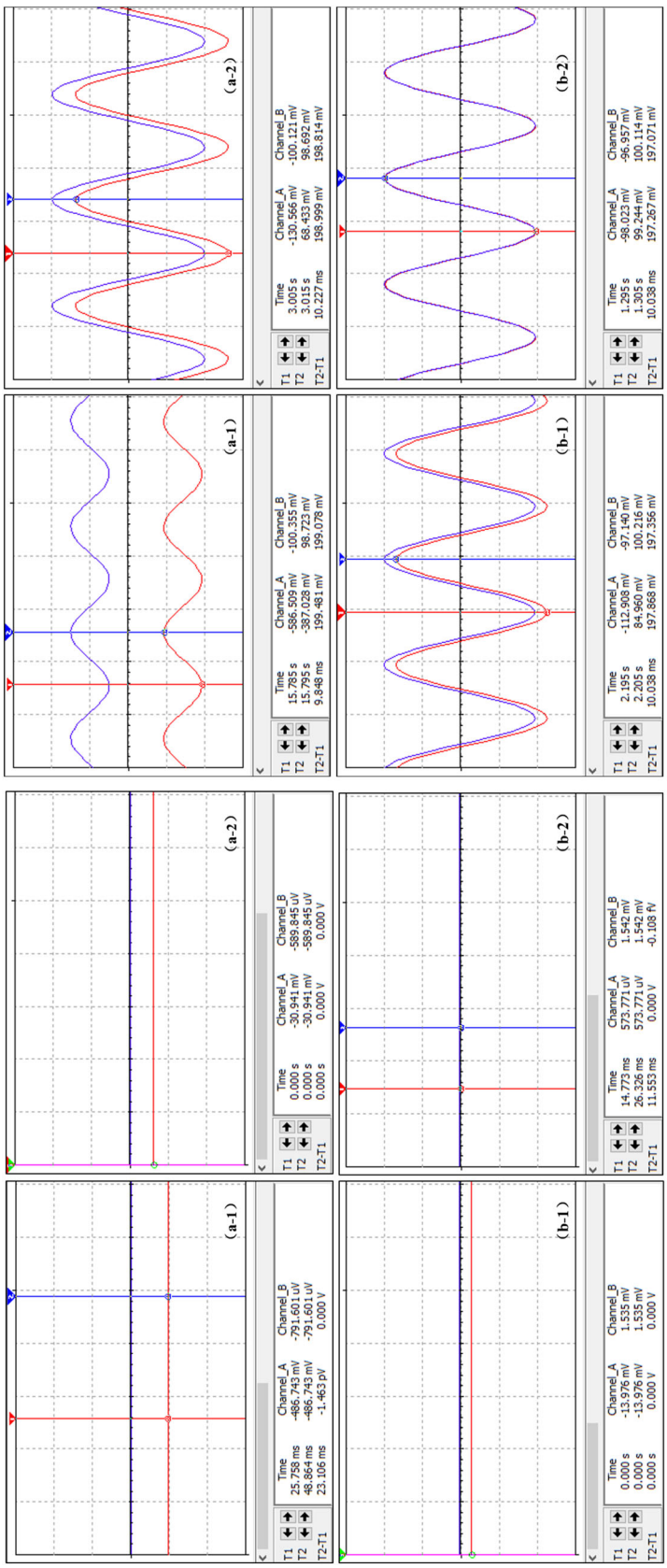

Fig. 6 Simulation results for the four types of circuits on the zero-input condition (**a**) and nonzero-input condition (**b**). Blue and red plots denote single and split schemes, respectively

Table 3 Statistic characters of baseline error for Fig. 6 results

Case	Baseline error1 (mV)	Baseline error2 (mV)
(a-1)	486.7	486.8
(a-2)	30.9	31.0
(b-1)	14.0	14.0
(b-2)	0.6	0.6

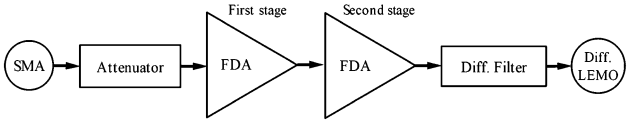

Fig. 7 Block diagram for the hardware design of the proposed processing circuit

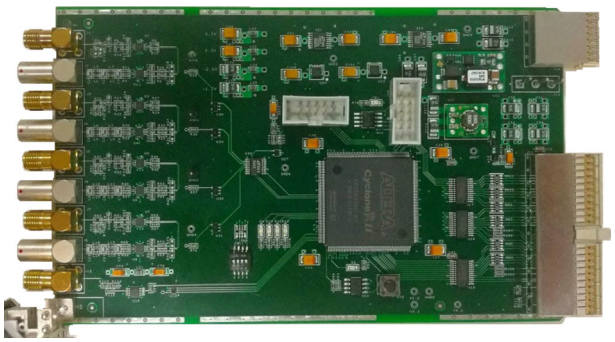

Fig. 8 Photograph of the PXI3U board for verifying the proposed processing circuit

the scope of the study.) The most direct way to implement the test of the board was to measure at the input terminal in no-input state given that the baseline errors were caused by the nonzero DC offset voltage at the input terminal in the split-range scheme. After putting the board in a slot of the PXI 1042 chassis, we used a multimeter (Fluke 87V) to measure terminal voltage and obtained a zero value. Additionally, a LeCroy oscilloscope (HDO6054) was also used to measure the DC voltage and observe the effective baseline submerged in the background noise. The results indicated the absence of detectable offset voltage observed at the input ports using either a Fluke 87V multimeter or a LeCroy oscilloscope, which consequently led to the absence of significant baseline errors in the presence of a resistive power divider in the split-range scheme.

5 Discussion and conclusion

5.1 Discussion

The current methodology was proposed from the hardware-design perspective. Theoretically, the non-block DC path indicated that the baseline error cannot be completely eliminated by the proposed AFE circuit. To clearly disclose the essential cause of the baseline error, the simulation circuits herein did not consider non-idealities that can affect specific values of the results. Although the simulation setup appeared to be highly ideal and the hardware verification did not appear to be adequately accurate, improvements in the proposed circuit were evident. In a certain sense, the problem was actually solved from the engineering application perspective via minimization of the error to the point of it being negligible. Additionally, the offline correction procedure can also be applied to solve the problem after essential calibrations are performed because the baseline error exhibits a fixed pattern for a given circuit structure in a specific connection scheme. The significant merit of offline correction corresponded to the absence of increased complexity in hardware design although it suffered from the drawback of requiring tedious work. Furthermore, the calibration is not self-adaptable and should be conducted again in the case of changes for the circuit characters. Additionally, the baseline offset error correction can also be implemented online with a potentiometer that is connected to the un-driven side. As shown in the TIDA-00826 design guide, with respect to the DC-coupled input, the potentiometer is employed to apply an appropriate DC correction, nulling the possible DC offset and matching the DC voltage of the input signal [20]. A comparison of the two correction schemes indicated that the proposed methodology constituted a more direct solution albeit the increased complexity in hardware design.

However, it is beyond the scope of this study to examine a specific solution to the DC offset problem for high-performance oscilloscopes.

5.2 Conclusion

This study indicates that the conventional self-consistent ADC driver using a DC-coupled FDA can cause an additional baseline error and consequently lead to unexpected out-of-range issues for sampling devices. The offset error is a major concern for HDR signals or any applications in the DC-coupling scheme involving resistive power dividers. After exploring the mechanism of the baseline error using the model and analysis, an offset-free DC-coupled AFE circuit based on two-stage amplification and a resistive attenuator was proposed to minimize the unwanted voltage. Essential simulations were implemented in an NI Multisim environment, and the proposed methodology was verified. Furthermore, a PXI 3U board was designed to verify the effects of the proposed circuit.

Although this study successfully addressed the baseline error from an engineering perspective, it presents a limitation in that an appropriate attenuating factor "*A*" should

be guaranteed. Despite its limitations, the study is certainly expected to significantly contribute to the high-precision measurement of HDR signals in many nuclear physics experiments and some applications in the DC-coupling scheme with FDAs involving resistive power dividers. Additionally, future studies should investigate a method to impose a voltage reference to implement the baseline shift function without introducing additional potential offset error. Furthermore, the proposed circuit was verified to be highly applicable in cases when the resistive divider corresponds to 1-to-2 splitting. Future studies should also focus on ensuring the applicability of the proposed methodology for general 1-to-N power dividers.

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