A Prototype of beam position and phase measurement electronics for the LINAC in ADS

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Abstract This article presents a prototype of beam position and phase measurement (BPPM) electronics designed for the LINAC in China Accelerator Driven Sub-critical system (ADS). The signals received from the Beam Position Monitor (BPM) detectors are narrow pulses with a repetition frequency of 162.5 MHz and a dynamic range more than 40 dB. Based on the high-speed high-resolution Analog-to-Digital conversion technique, the input RF signals are directly converted to In-phase and Quadrature-phase (*IQ*) streams through under-sampling, which simplifies both the analog and digital processing circuits. All signal processing is integrated in one single FPGA, in which real-time beam position, phase and current can be obtained. A series of simulations and tests have been conducted to evaluate the performance. Initial test results indicate that this prototype achieves a phase resolution better than 0.1 degree and a position resolution better than 20 μm over a 40 dB dynamic range with the bandwidth of 780 kHz, which is well beyond the application requirements.

Key words Beam position and phase measurement, RF signal IQ under sampling, Analog-to-digital conversion, ADS

1 Introduction

The ADS is capable of transmuting radioactive nuclear wastes and meanwhile producing energy in a clean and safe way, and it is now a very important research domain in China[1]. As a key part of ADS, a high intensity proton LINAC is required to produce high power proton beams. To guarantee a high beam quality, the measurement of beam position, phase and current is indispensable.

The beam position and current can be calculated from the signal amplitudes of the four BPM detectors as in Eqs.(1), (2) and (3)[2].

$$Y=K_Y(V_A-V_B)/(V_A+V_B)-Y_{offset} \quad (1)$$

$$X=K_X(V_C-V_D)/(V_C+V_D)-X_{offset} \quad (2)$$

$$I=K_I(V_A+V_B+V_C+V_D)+I_{offset} \quad (3)$$

where X and Y are the positions in X and Y axis; $\boldsymbol{I}$ is the beam current; V_A, V_B, V_C and V_D are amplitudes of the four induction signals; K_X, K_Y and K_I are position and current coefficients.

The induction signals from the BPM detectors are periodic narrow pulses with the repetition frequency of 162.5 MHz. Considering that the signal energy is located on the frequency of 162.5 MHz and its integral multiples, the relative amplitudes of the narrow pulses can be obtained from the signal amplitudes on 325 MHz, because they are proportional to each other.

Most of beam measurement systems in China and abroad are single-function, for example, either only phase or only position measurement[3–11]. In the LINAC of ADS, both high-resolution beam position and phase measurements are demanded within one single system. And the position and phase resolutions are required to be better than 0.2 mm and ±0.5 degree in the input amplitude range of –38 – –4 dBm. In the

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phase measurement, a MO signal (162.5 MHz sine wave) is used as a reference.

This paper presents a prototype Beam Position and Phase Measurement Electronics for the LINAC of ADS.

2 Measurement principle

The mainstream methods of position and phase measurements are based on *IQ* analysis. With orthogonal ***I*** and ***Q*** information, beam phase and amplitude can be calculated [3], as in Eqs.(4) and (5):

$$Phase = \arctan(I/Q) \quad (4)$$

$$Amplitude = (I^2+Q^2)^{1/2} \quad (5)$$

Traditional IQ analysis methods are based on analog demodulation, such as the RF phase monitor system in the BEPCII LINAC[5,6]; this method requires complex analog manipulation, and the performance is easily deteriorated by noise, non-linearity and mismatches of the analog circuits[7]. With the development of the *A*/*D* conversion and digital signal processing techniques, the Intermediate-Frequency (IF) *IQ* sampling technique was developed, in which the RF signal is firstly down converted to an IF signal by analog manipulation, and then digitized with a sampling clock at a frequency four times of the IF signal frequency (f_s=4f_{IF}), to directly obtain the ***I*** and ***Q*** streams; thus the Digital Signal Processing (DSP) algorithm is quite simple and the complexity of analog circuits is also reduced[8–10]. There also exists another method named digital *IQ* demodulation, in which the input RF signal is directly digitized after amplification and filtering, with all signal processing conducted in digital domain. It is remarkable for its simplest analog circuits, however, with rather complicated DSP algorithms[4,11].

This BPPM electronics is designed based on the method of RF signal *IQ* under sampling (RFIQUS), in which the RF signal is directly converted to a digital IF signal after simple analog manipulation. By adjusting the sampling clock frequency, we can obtain 4 samples within one IF period, i.e. ***I*** and ***Q*** points. This method simplifies both the analog circuits and the DSP algorithms; thus a better system simplicity can be achieved[12].

In the RFIQUS method, the sampling clock frequency should be carefully selected, as in Eq.(6).

$$f_s=4Nf_{in}/(4NK\pm1) \quad (6)$$

where *N* and *K* are integers.

In this BPPM electronics, the measurement is conducted with the second harmonics of the induction signals (325 MHz); meanwhile, the MO signal (162.5 MHz) also needs to be measured as the phase reference, which means the electronics is responsible for processing signals with two different frequencies. As for the 325 MHz signal, f_s is set to be 100 MHz (*K*=3 and *N*=1). Fig.1 illustrates the basic *IQ* under sampling procedure in frequency domain. As shown in Fig.1(a), through under sampling, the 325 MHz RF signal is equivalently down converted to a 25 MHz digital IF signal, whose frequency is just in the center of the Nyquist zone. We performed simulations to verify the validity of the method based on the Matlab platform. As shown in Fig.2(a), there exit just 4 samples (***I***, ***Q***, –***I***, –***Q***) in one period of the IF signal. As for the 162.5 MHz MO signal (as shown in Fig.2(b)), by discarding half of samples, a 12.5 MHz IF signal can also be obtained with 4 samples within one period, and now the equivalent sampling rate is decreased from 100 MHz to 50 MHz. The sampling procedure for the MO signal in frequency domain is shown in Fig.1(b).

The above analysis and simulations indicate that the 325 MHz RF signal and 162.5 MHz MO signal can be converted to ***I*** and ***Q*** streams simultaneously with the same sampling clock, and then the position and phase can be further calculated.

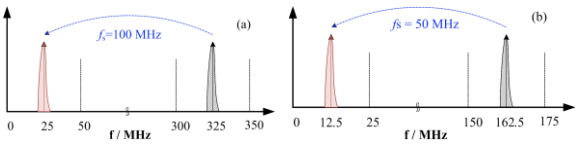

Fig.1 Under sampling procedure in frequency domain. (a) 325 MHz RF signal, (b) 162.5 MHz MO signal

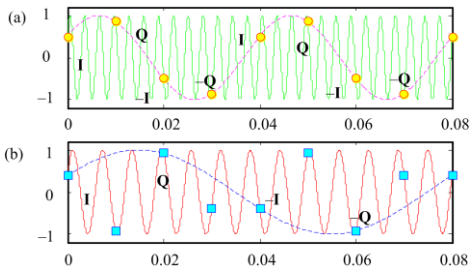

Fig.2 Simulation of the under-sampling process in time domain; the solid lines refer to the input RF signals; the dashed lines are the digital IF signals.

3 System architecture

This BPPM electronics consists of two hardware modules: the Analog Front End (AFE) and the Digital Processing Board (DPB), which are packaged within two PXI-6U modules, as shown in Fig.3. The RF and MO signals are firstly filtered and amplified in the analog signal manipulation circuits, and then under sampled in the *A*/*D* conversion parts to ***I*** and ***Q*** streams, which are transferred to the DPB. All the digital signal processing is integrated in one single FPGA in the DPB. The calculated results are transferred through the PXI bus to a Single Board Computer (SBC) located in Slot0 of the chassis, for further data analysis and display.

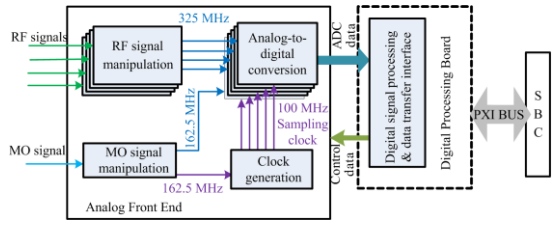

Fig.3 Block diagram of the BPPM electronics.

3.1 Analog manipulation circuits

As mentioned above, the input signals from the BPM detectors are narrow pulses with a repetition frequency of 162.5 MHz. As shown in Fig.4(a), the first Band Pass Filter (BPF) is used to extract the 325 MHz RF signal (the second harmonic component of the pulses), and the other 2 BPFs are used to suppress out-of-band noise and spurious frequency components. To guarantee a good system performance over a large dynamic range, the 325 MHz RF signal are amplified by the Auto Gain Control (AGC) circuit to fit the full-scale range of the *A*/*D* Converter (ADC). The AGC consists of cascaded gain blocks and RF attenuators, which achieves a variable gain more than 40 dB. As for the MO signal, the manipulation circuits are quite similar, except for a smaller input dynamic range, as shown in Fig.4(b). Moreover, the MO signal is split to two paths, one as the reference for the system clock and the other used for phase calculation.

Simulations have been conducted to estimate the performance of the manipulation circuits for 325 MHz RF signal in Agilent Advanced Design System software. As shown in Fig.5, the gain dynamic range is more than 40 dB, and the rejection outside the frequency range of 300–350 MHz is good enough for the anti-aliasing filtering requirement in this application[13].

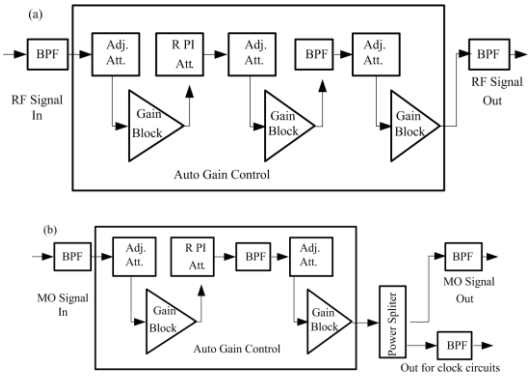

Fig.4 Analog manipulation circuits. (a) 325 MHz RF signal, (b) MO signal.

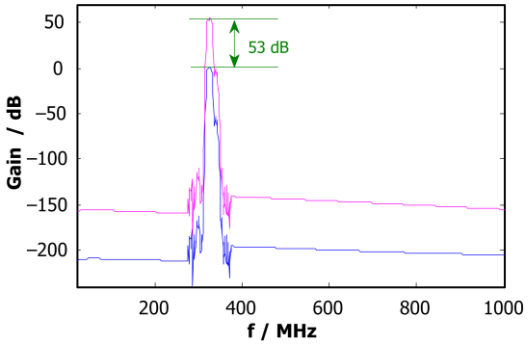

Fig.5 Simulation results of the analog manipulation circuits for the 325 MHz RF signal.

3.2 Analog-to-digital conversion circuits

As the kernel part of the RFIQUS method, the ADC chip AD9467 with 16-bit resolution and 200 Msps maximum sampling rate is employed. With an input signal frequency up to 300 MHz, its Effective Number of Bit (ENOB) and Spurious Free Dynamic Range (SFDR) parameter are better than 11.9 bit and 91 dBc separately, rendering it suitable for under-sampling application[14]. Moreover, the AD9467 output interface is 8 bit wide with the Double Data Rate (DDR) technique and the Low Voltage Differential Signal (LVDS) standard, which simplifies hardware design.

The analog front end circuit for the ADC is very important, especially in high-speed high-resolution situation. The circuit is used to convert the single-ended signal to differential signals and match the impedance. As shown in Fig.6(a), a balun

transformer TC1-1T+ with center tap on secondary balanced side[15] is used, which has excellent amplitude and phase balance[16]. To further reduce the unbalance caused by parasitic effect, two TC1-1T+s are used in a cascade mode[17]. In addition, the secondary-side termination is employed for a smoother frequency response[18].

To select suitable values of the resistors and capacitors in Fig.6(a), a series of simulations have been performed based on S-parameter models. Fig.6(b) shows the S11 simulation results for the 325 MHz RF signal (the S11 parameter is equivalent to the signal reflection ratio of the front-end circuit). By trying different values of resistors and capacitors, an optimal S11 of -62.0 dB is achieved. With the same method, an optimal S11 of -66.5 dB is obtained for the MO signal.

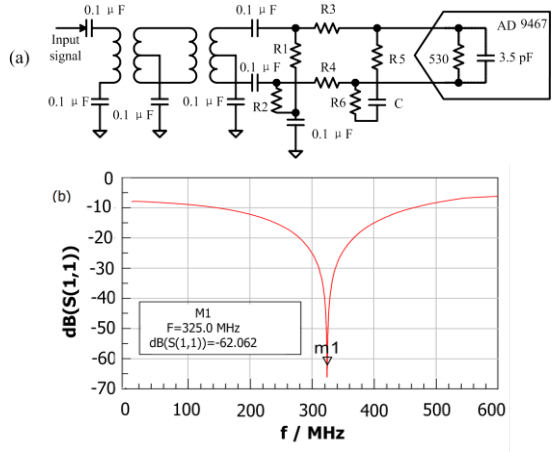

Fig.6 ADC front-end circuit design and simulation. (a) Block diagram of the ADC front-end circuit, (b) S11 parameter simulation results for the 325 MHz RF signal.

3.3 Clock generation circuits

In high-speed high-resolution *A*/*D* conversion, a high quality clock circuit is indispensable. The sampling clock jitter will directly affect Signal-to-Noise Ratio (SNR), as in (7) [19].

$$SNR = -20\log(2\pi f_{in} t_{jitter}) \quad (7)$$

Sampling clocks for A/D conversion can be generated with modern digitally controlled phase locked loop (PLL) circuits. In this system, a cascaded PLL structure is employed for excellent jitter cleaning.

As shown in Fig.7(a), the 162.5 MHz reference clock derived from the MO signal is fed into PLL1 to generate a 100 MHz output signal. The PLL1 provides initial jitter cleanup with a narrow-loop bandwidth and a low close-in phase noise VCXO. PLL2 translates the output signal of the PLL1 with a low far-end phase noise VCO. With the combination of the two PLL stages, the jitter of the final output signal will be quite low with phase noise suppression in both close-in and far-end regions [20]. A clock generator chip AD9523-1 with excellent jitter performance is employed, which integrates all the circuits in Fig.7(a), except for the VCXO in PLL1. And S620-LF of KVG co. is selected as the low noise external VCXO.

To estimate the performance of this clock generation circuits, simulations were performed in the ADIsimCLK Ver1.4 software. As shown in Fig.7(b), the broad band jitter of the output clock is 274 fs. As for the input frequencies of 325 MHz and 162.5 MHz, the corresponding ENOBs are 10.5 bit and 11.5 bit respectively, well beyond the application requirement.

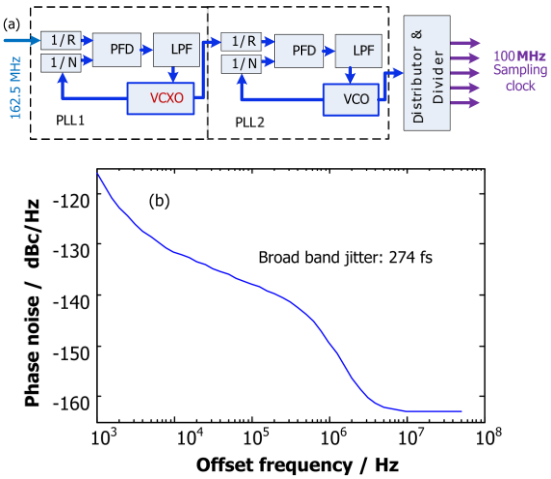

Fig.7 Clock generation circuits design and simulation. (a) Block diagram of the clock generation circuits, (b) Phase noise simulation results of the clock generation circuits.

3.4 Digital signal processing & data transfer interface

The block diagram of the DPB is shown in Fig.8(a). The main FPGA in the DPB receives the high speed ADC data from the AFE, and calculates the position and phase results, which are stored in an on-board DDR SDRAM. The PXI interface is implemented in the CPLD for communication with the SBC in Slot0. To enhance the flexibility of the system design, on-line modification of the FPGA logic is achieved, for which a 128-Mb FLASH chip is used to store the configuration data.

The XC5VLX155T device from Xilinx Virtex 5 family is employed as the main FPGA, where all the digital processing is implemented, as shown in Fig.8(b). The input DDR LVDS data (8 bit, 200 Msps) from the AFE is rearranged to 16-bit 100-Msps data streams through IDDR and IBUFDS primitives in XILINX FPGA. And then the ***I*** and ***Q*** arrays are extracted to calculate the amplitude and phase according to the algorithms based on Eqs.(4) and (5). Finally the *X* and *Y* positions and the beam current are obtained with the amplitudes of the four 325 MHz RF signals based on Eqs.(1), (2) and (3). Then the results of beam phase, position and current are transferred to the PXI interface in the CPLD. The FPGA is also responsible for decoding the commands from the PXI bus to control the AFE.

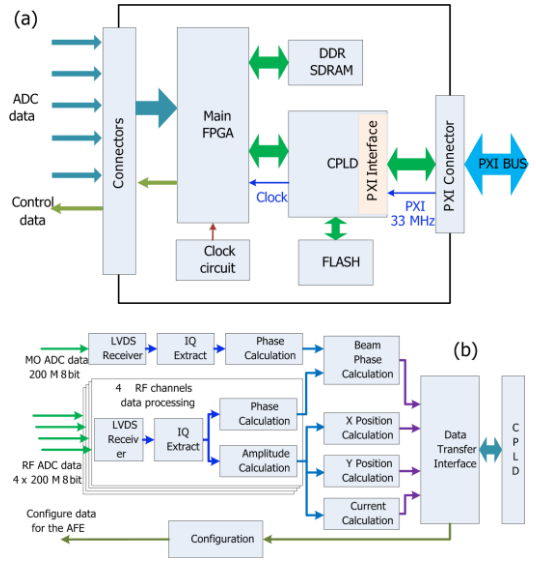

Fig.8 Digital processing board design. (a) Block diagram of the digital processing board, (b) Data processing logic in the FPGA.

4 Initial Test Results

A series of tests have been conducted to evaluate the system performance. The test platform is shown in Fig.9. A high-quality signal generator R&S SMA 100A is used to generate a 325 MHz RF signal and a 162.5 MHz synchronous clock as the MO signal. The 325 MHz signal is then split to the four RF channels in the AFE. The ADC data from the AFE is transferred to the DPB through high-speed high-density flat cables. The SBC in Slot0 of the PXI chassis is responsible for the data readout and the system control, as well as offline data analysis.

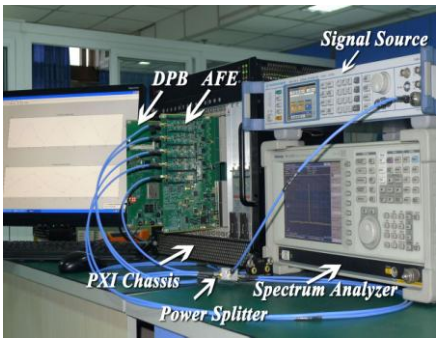

Fig.9 System under test.

4.1 Tests of analog manipulation circuits

The quality of the analog manipulation circuits in the AFE directly affects the position and phase measurement resolution. We conducted tests with a real-time spectrum analyzer Tektronix RSA3303B. By comparing the amplitudes of the AFE input and output signals, the actual gain of the circuits can be calculated. A series of gain test results can be obtained by tuning the attenuation of the RF channels. Test results indicate a gain dynamic range of 47 dB is achieved, beyond the 40 dB requirement.

Test results of the band pass filtering performance are shown in Fig.10; as for the 325 MHz RF signal and 162.5 MHz MO signal, the out-of-band suppression is better than 85 dB and 100 dB.

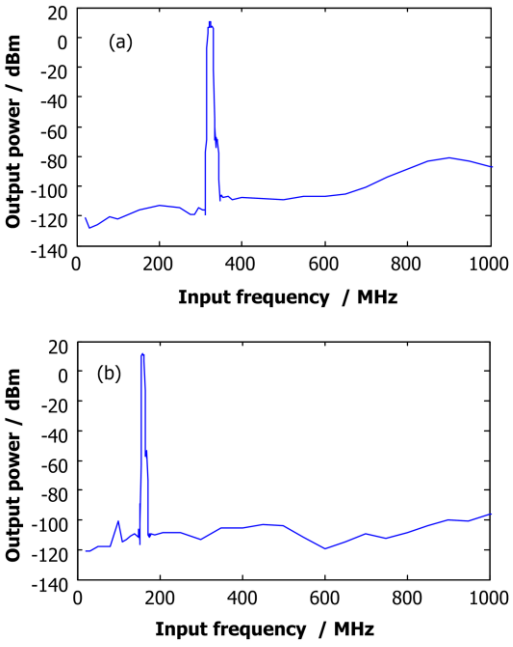

Fig.10 Band pass filtering performance. (a) 325 MHz RF signal. (b) 162.5 MHz MO signal.

4.2 Waveforms of the digitized IF signals

The waveform of the digitized IF signals in Fig.11 accords well with the simulation results in Fig.3. It indicates that *I* and *Q* arrays can be obtained from the original 325 MHz RF signal and 162.5 MHz MO signal simultaneously.

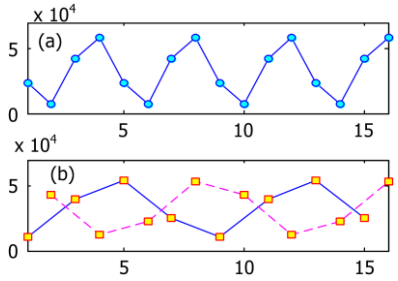

Fig.11 Digitized waveforms of the 325 MHz RF signal and 162.5 MHz MO signal. (a) RF signal under-sampled waveform, (b) MO signal under-sampled waveform.

4.3 Test results of position and phase measurement

Figure 12(a) shows the histogram of phase measurement results with a –10 dBm input amplitude, which corresponds to a phase resolution of 0.08 degree. As shown in Fig.12(b), in the input amplitude range of –44 dBm to –4 dBm, the phase resolution is better than 0.2 degree with the bandwidth of 25 MHz, and better than 0.1 degree with the bandwidth reduced to 780 kHz, well beyond the ±0.5 degree requirement.

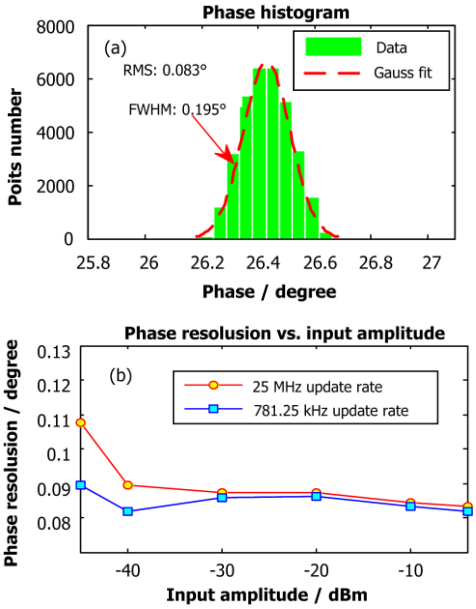

Fig.12 Test results of Phase measurement. (a) Histogram of phase measurement results (input amplitude: –10 dBm, bandwidth: 780 kHz), (b) Phase resolution with different input signal amplitudes.

Figure 13(a) is the position histogram, and a resolution of 0.398 um is achieved with a –10 dBm input amplitude. Fig.13(b) shows the position resolution in the amplitude range of –44 dBm to –4 dBm. A position resolution better than 20 um is achieved over this 40 dB dynamic range, which is better than the requirement of 0.2 mm. When the input amplitude exceeds –40 dBm, the resolution is better than 5 μm.

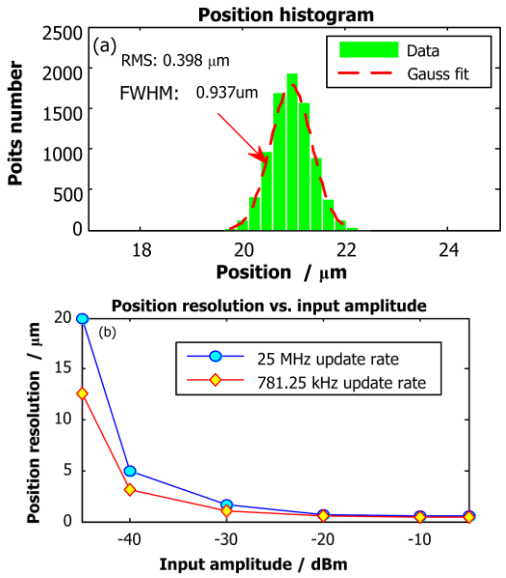

Fig.13 Test results of position measurement. (a) Histogram of position measurement results (input amplitude: –10 dBm, bandwidth: 780 kHz), (b) Position resolution with different input signal amplitudes.

5 Conclusion

A prototype of beam position and phase measurement electronics for the LINAC in ADS is presented. We designed two modules—the AFE and DPB based on the PXI 6U standard, and conducted initial tests to evaluate the performance. The electronics has achieved a phase resolution better than 0.1 degree and a position resolution better than 20 μm over the input amplitude range of 40 dB with bandwidth of 780 kHz.

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