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Design and simulation of Gaussian shaping amplifier made only with CMOS FET for FEE of particle detector

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Abstract The objective of this paper is to design and simulate a shaping amplifier circuit for silicon strip, Si(Li), CdZnTe and CsI detectors, etc., which can be further integrated the whole system and adopted to develop CMOS - based application, specific integrated circuit for Front End Electronics(FEE) of read-out system of nuclear physics, particle physics and astrophysics research, etc. It's why we used only CMOS transistor to develop the entire system. A Pseudo-Gaussian shaping amplifier made by fourth-order integration stage and a differentiation stage give a result same as a true CR-RC^4 filter, we perform shaping time in the range, 465 ns to 2.76 μs with a low output resistance and the linearity almost good.

Key words Shaping Amplifier, CMOS transistor, Gaussian, CR-RC^n filter, Simulation

1 Introduction

In nuclear instrumentation, a shaping amplifier is a CR -RC^n filter consisting of a differentiation stage followed by an n order integration stage. A band-pass biquadratic structure is preferred to implement the shaping amplifier, because of its low sensitivity to component variations. A two-stage amplifier has been designed at IMP for the filter, followed by a source output stage[1, 2].

The design is a single channel shaping amplifier, intended to read out the signals from charge sensitive preamplifier for silicon strip, Si(Li), CdZnTe and CsI detectors, etc. Gaussian shaping amplifier accepts a step-like input pulse and produces an output shaped like a Gaussian function. The purposes are to filter much of noise from the signals of interest and to provide a quickly restored baseline to allow high counting rates[3]; it is why the shaping time specification should be well selected. The shaping time is defined as the time-equivalent of the standard deviation of the Gaussian output pulse. A simpler measurement to make in the laboratory is the full width of the pulse at half of its maximum value (FWHM). This value is greater than the shaping time by a factor of 2.35[4]. The design consists of 4 poles integration and signal gain is available for different shaping times with the range 465 ns to 2.76 μs.

The filter parameters have been selected by simulation using Proteus[5] to optimize the energy resolution. The circuit configuration of the shaping amplifier proposed in this paper can be adopted to develop CMOS-based application specific integrated circuit (ASIC) for front end electronics (FEE) of read-out system of nuclear physics, particle physics and astrophysics research, etc. providing measurements of energy of particle.

2 Circuit design

2.1 Shaping amplifier principle

A shaping amplifier is AC-coupled to preamplifier[6], which is a two-stage amplifier with a source follower output stage, as illustrated in Fig.1. The DC level from the input network is isolated by the capacitor C1. Also

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the C1 and the input resistor of the amplifier provide the differentiation function of shaping amplifier. The output of this circuit looks like the result of true RC/CR filter. After connecting four shaping amplifiers, a Pseudo-Gaussian shaping amplifier is constructed with one differentiation stage and four integration stages, and has almost the same function as a true CR-RC^4 shaping amplifier. The shaping time can be selected from 465 ns to 2.76 μs supported by the simulation result.

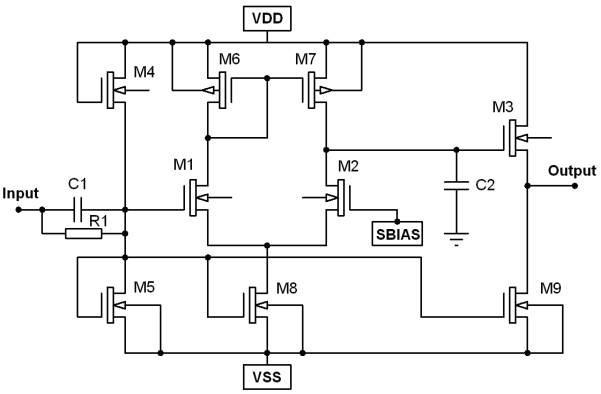


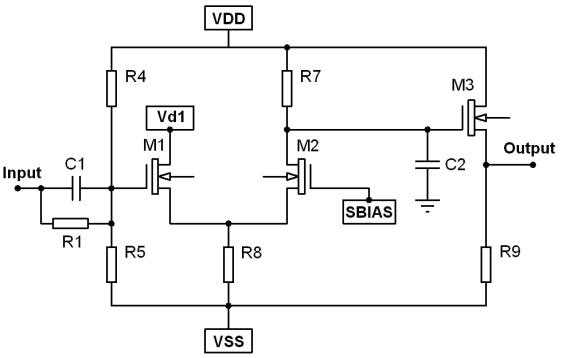
Fig.1 Schematic drawing of shaping amplifier.

2.2 The core shaping amplifier

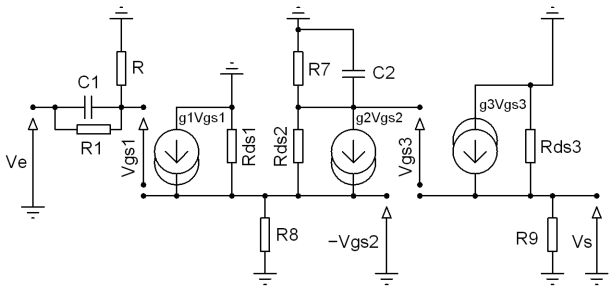
Composed of a two-stage amplifier followed by an integration stage, this shaping amplifier mainly comprises the capacitor C2, the transistor M7 implemented as resistor, and the transistors M2 and M1(Fig.1), and the last stage is a source follower unity gain buffer with output stage for low output resistance. The first stage amplifier minimizes the power dissipation by allowing the transistor input to be biased through the transistor CMOS M6 implemented as diode[6]. The input transistor bias is set by transistor CMOS M4 and M5 implemented as an external resistor which also delivers to the transistors (transistors M8 and M9) current mirror[7].

2.3 Shaping transfer function

The shaping amplifier in Fig.2(A) is the same as the one in Fig.1, we just replaced the transistors (M4, M5, M7, M8, and M9) implemented as a resistor [8] and the transistor M6 implemented as a diode ($V_{d1}=V_{DD}-V_{dsat6}$). To develop the transfer function, we transformed the circuit in Fig.2 to an equivalent circuit related to the frequencies adopted (Fig.2B).



(A)



(B)

Fig.2 Shaping amplifier circuit (A) and its equivalent circuit related to the frequencies adopted (B).

From Fig.2(B), R is the equivalent resistance of R4 and R5 looked in parallel, the transfer function is given by Eq.(1) :

$$H(S)=H_0\left(\frac{1+\tau_d s}{1+\tau_D s}\right)\left(\frac{1}{1+\tau_i s}\right)^n \tag{1}$$

$$s=jw,\quad n=1,\quad \tau_d=R_1C_1,\ \tau_D=[R_1R/(R_1+R)]C_1$$

$$\tau_i=\frac{\left(\left(1+g_1R_{ds1}\right)+R_{ds1}\left(\frac{1}{R_8}+\frac{1+g_2R_{ds2}}{R_{ds2}}\right)\right)}{\left(\left(1+g_1R_{ds1}\right)+R_{ds1}\left(\frac{1}{R_8}+\frac{1+g_2R_{ds2}}{R_7+R_{ds2}}\right)\right)}\left(\frac{R_7R_{ds2}}{R_7+R_{ds2}}\right)C_2$$

where H_0 is a constant depending of the parameters from different stage and from the input and output resistances; τ_i is the shaping time (the time constant of the integrators); τ_D is the time constant of the differentiator; and n is order of the integration stage (also called shaper order).

2.4 Main design parameters

The main design parameters are given in Table 1.

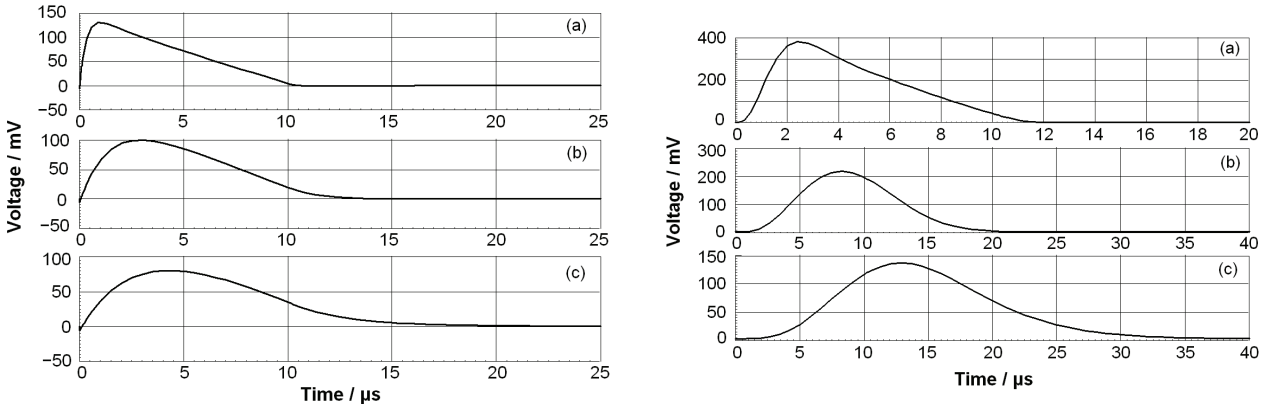
Table 1 The design parameters of the shaping amplifier

Parameters	Values
Power supplies	$V_{DD}=+2$ V, $V_{SS}=-2$V
Input transistor M1 parameter	$K=2\times10^{-1}$ A/V^2, $V_T=1$
Transistor M2 parameter	$K=2\times10^{-5}$ A/V^2, $V_T=1$
Bias voltage of transistor M2	SBIAS = +2 V
Input amplitude range	10 mV_{p-p} to 2 V_{p-p}
Output resistance	25 Ω

3 Shaping amplifier performance

3.1 Simulation results and discussion

The measurement was made for several values (Fig. 3A). The shaping time of signals observed in the output of a single shaping amplifier, have a range from 939 ns to 4.26 μs related respectively to integration capacitor value from 10 pF to 100 pF. The output impedance of shaping amplifier was measured at 25 Ω with 10 kHz 100 mV input signals. It was also observed that the shaping time increased with the integration capacitor value, while the amplitude decreased with increasing capacitor values.



(A) (B)

Fig. 3 Shaping output CR-RC (A) and CR-RC^4 (B). (a) $C_2=10$ pF, (b) $C_2=50$ pF, (c) $C_2=100$ pF

When we constructed a CR-RC^4 filter, other integration stages with the same specification as one in Fig. 3(A) was connected directly without the AC couple. The shaping time was improved; therefore the range now is 652 ns to 3.12 μs, as illustrated in Fig.3(B).

3.2 Linearity measurements

Non-linearity of the circuit was measured (Fig. 4). One sees that the linearity is good up to 500 mV, where the non-linearity begins to increase , but it remains below 2% for $V_{in,\,max}=1000$ mV.

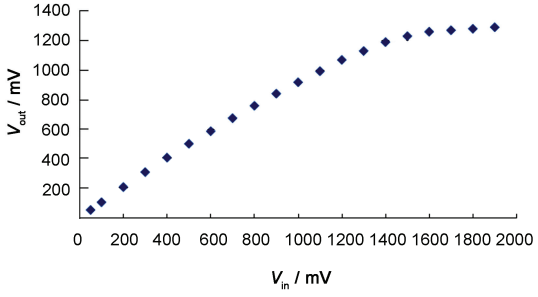


Fig.4 Measured non-linearity of the shaping amplifier (CR-RC^4 filter)

3.3 Achievement

The circuit configuration of the shaping amplifier can be adopted to develop CMOS-based application-specific integrated circuit, by replacing the integration capacitor with the transistor CMOS implemented as capacitor[9]. The replacement of the capacitor in Fig. 1 by transistor CMOS called capacitor CMOS, gives a new shaping amplifier circuit (Fig.5). The simulation from this circuit according to the same specification used for the real capacitor of integration, gives a slight change of shaping time, from 465 ns to 2.76 μs (Fig. 6). Also the measured linearity of CR-RC^4 filter is below 2% for the input amplitude range, 50 mV to 1000 mV.

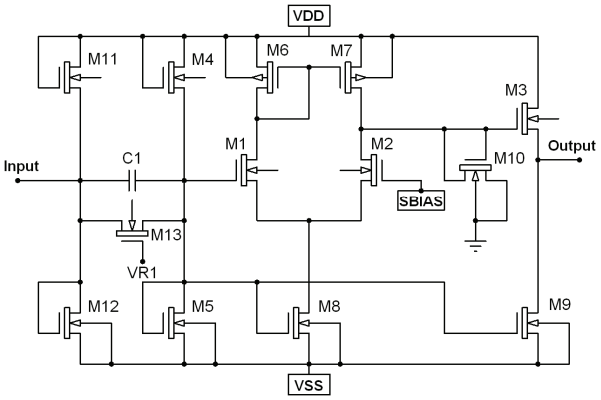


Fig.5 Schematic drawing of shaping amplifier with CMOS implemented as integration capacitor.

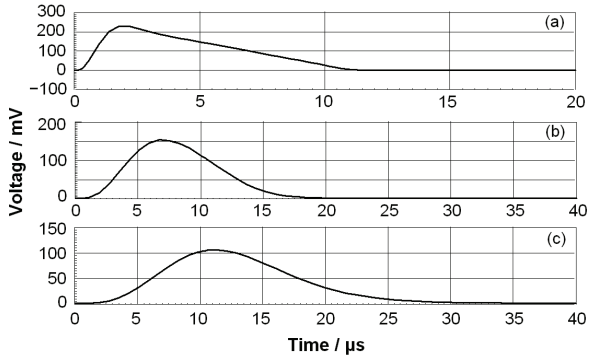


Fig.6 Shaping output CR-RC^4 with CMOS implemented as integration capacitor, (a) $C_2=10$pF, (b) $C_2=50$pF, (c) $C_2=100$pF.

From the results in Fig.3(B) and Fig.6, we can appreciate the difference of the amplitude and the shaping time. These differences come probably from parameters of the CMOS transistors [10], such as the equivalent resistance, which is not easy to control when we implement transistor CMOS as a capacitor [9]. It will be a challenge for us to control these parameters in the next step researches.

To summarize, the good show of Gaussian shaping amplifier after simulation can be obtained when the integration capacitor value is increased toward to100pF, but a big capacitor is not too good for ASIC realization. Fig.7 shows the output shaping amplifier of $n=1$ to $n=4$ order integration stage.

4 Conclusions

After designing the new shaping amplifier with CMOS FET implemented as integration capacitor, computer simulation was carried out by PSPICE simulator using BSIMV3.3 parameters of the Proteus, and the nearly same results were obtained when the simple capacitor

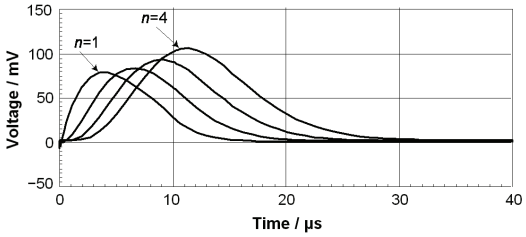


Fig.7 Output of shaping amplifier when $n=1$, $n=2$, $n=3$ and $n=4$ for $C_2=100$pF

is used as integrated capacitor and CMOS FET is implemented as integration capacitor. The advantage of this design is to develop CMOS-based application specific integrated circuit for an entire shaping amplifier. The shaping time for this purpose gives the range 465ns to 2.76 μs with 25 Ω as output resistance and good linearity. In the near future, we expect to improve these results by controlling the parameters of CMOS equivalent circuit, when it uses such as resistor, capacitor or diode, etc.

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