Analysis of output voltage on a planar insulating core transformer

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Abstract Output voltage is an important performance characteristic of planar insulating core transformer (PICT). In PICT magnetic cores are insulated from their neighboring magnetic cores by solid insulating materials. Solid insulating materials can increase leakage flux. This results in a low generated voltage in secondary coils, especially on the upper stages. Connecting flux compensation capacitors to secondary coils can compensate the flux loss. Design equations to calculate the flux compensation capacitors value and relevant simulation by CST and Protel software were presented. Simulation results of an actual PICT showed that output voltage increased by 19% after being connected to flux compensation capacitors and the voltage on every stage was equally distributed. Results of simulation were consistent with the following experimental test, which revealed that flux compensation capacitors were effective.

Key words Planar insulating core transformer (PICT), Output voltage, Flux compensation capacitors, CST, Protel

1 Introduction

Planar insulating core transformer (PICT) was developed over ten years ago[1,2], along with the developments of high frequency solid-state switching devices and planar technology As shown schematically in Fig.1, the secondary coils and voltage-doubler rectifiers of PICT are arranged on the printed circuit board (PCB) to reduce impedances and parasitic capacitances[3]. The structure of PCB also facilitates efficient utilization of the magnetic core. As a novel form of ICT[4-6], a PICT based on high frequency solid state switching devices offers higher operation efficiency, less energy consumption and smaller size than conventional ICTs. A PICT uses a multi-stage cascade circuit, with magnetic coupling between the insulated transformer cores, to transfer low voltage AC power to an assembly of high voltage. Magnetic cores are segmented by solid insulating materials[7]. Permeability of the solid insulation is almost that of air. This increases leakage flux and result in a reduction of generated voltage per turn in secondary coils, especially on the upper stages. The turn ratio is often increased with each higher stage to keep stage-to-stage voltage the same. It’s useful for conventional ICT, but not suitable for PICT with arrangement of identical PCB.

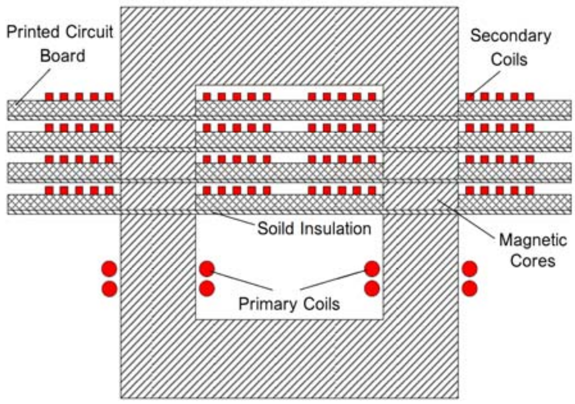

Fig.1 Diagram of PICT (voltage-doubler rectifiers and filter capacitors fixed on PCB are not shown).

In this paper a new method is proposed to increase output voltage of a PICT, which is simulated with the equations and the calculation results are verified by experiments.

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Received date: 2011-07-14

2 Theoretical analyses

The segmentation of the PICT magnetic cores introduces gaps in the magnetic circuit with permeability essentially that of air. This greatly increases the reluctance of the magnetic circuit, produces magneto motive force (MMF) drops and rises magnetizing current. Higher magnetizing current produces more leakage flux since leakage inductance is practically constant[8]. As a result, a lower voltage induced in the secondary coils, especially on the upper stages. Connecting flux compensation capacitors C_0 (Fig.2) to every secondary coils circuit can produce a current of the correct phase to provide a MMF. If the MMF produced by every flux compensation capacitor is proportional to the MMF loss by each gap, magnetizing current would be the same as that without solid insulation materials and the main flux throughout the magnetic circuit would remain constant.

Electromotive Force (EMF) E_{20} induced in the secondary coilson every stage can be given as

$$E_{20} = n_{20}\frac{\mathrm{d}\phi}{\mathrm{d}t} = n_{20}(2\pi f)\phi \tag{1}$$

where n_{20} is the secondary coils turns on every stage, ϕ is the magnetic flux flowing through the magnetic core and f is the frequency of excitation.

EMF E_{20} will produce a compensation current i_2' in the secondary coils

$$i_2' = \frac{emf}{r} = \frac{n_{20}(2\pi f)\phi}{\dfrac{1}{(2\pi f)C_0}} = n_{20}(2\pi f)^2 C_0\phi \tag{2}$$

where r is the resistance of the compensation capacitor C_0.

The current i_2' flows through the secondary coils on every stage and will produce a MMF F_{20} as given as

$$F_{20} = n_{20}i_2' = n_{20}^2(2\pi f)^2 C_0\phi \tag{3}$$

For an insulated gap having a cross-sectional area s and a thickness l_0, the reluctance R is given by

$$R = \frac{l_0}{\mu_0 s} \tag{4}$$

where μ_0 is the permeability of free space. The ϕ flowing through reluctance R results in a MMF drop F_{20}' as follows

$$F_{20}' = \phi R = \phi\frac{l_0}{\mu_0 s} \tag{5}$$

The value for the compensation capacitor C_0 is selected so that the secondary coils on every stage would generate exactly enough MMF F_{20} to compensate for the MMF drop F_{20}' in one layer of the insulated gap,

$$F_{20} = F_{20}' \tag{6}$$

Take Eq. (3) and Eq. (5) to Eq. (6), one has

$$C_0 = \frac{l_0}{n_{20}^2(2\pi f)^2\mu_0 s} \tag{7}$$

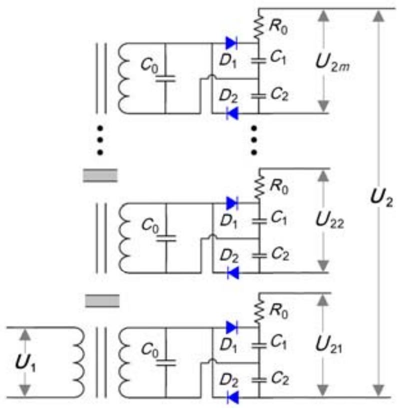

Fig.2 Circuit diagram of PICT.

From Eq.(7), the C_0 value is a function independent of the output voltage or current. For a fixed f in the primary coils of PICT, the analysis shows that connecting certain compensation capacitors to secondary coils on each stage can compensate the flux loss and increase output voltage.

3 Simulation and the circuit design

CST (Simulation) software provides accurate 3D electromagnetic electronic design automation solutions for the numerical solution of Maxwell's Equations. The magnetic field of a PICT with or without the solid insulation (l_0=0.8 mm) was simulated by low frequency domain solver of CST EM studio. The relevant parameters of the PICT are: n_1=5, n_{20}=64, s=100 cm^2, M=5, where n_1 is the primary coils turns and M is the number of stages. The mesh type of simulation is hexahedral while the mesh cells number is about 124 k. The CST simulation results are given in Table 1 for l_0=0.8 mm and the self inductance of primary coils is 107 μH, and for l_0=0 and the inductance of primary coils is 765 μH. From Table 1, it is obvious that the solid insulation materials cause coupling coefficient between the primary coils and the secondary coils on the m^{th} stage ($0<m\leqq 5$) k_m to taper off and lead to poor output voltage efficiency.

Table 1 CST simulation results of a PICT with (l_0=0.8 mm) and without solid insulation (l_0=0)

Parameters	l_0=0.8 mm					l_0=0				
	m =1	m =2	m =3	m =4	m =5	m =1	m =2	m =3	m =4	m =5
L_{2m}/mH	16.75	16.22	16.07	16.25	16.79	124.85	124.74	124.55	124.88	125.24
M_{12m}/mH	1.29	1.23	1.18	1.16	1.15	9.73	9.68	9.65	9.62	9.60
k_m	0.964	0.932	0.904	0.878	0.855	0.996	0.991	0.988	0.984	0.981
M_{212m}/mH	–	15.81	15.22	14.85	14.69	–	124.06	123.54	123.18	122.95
k_{212m}	–	0.959	0.928	0.900	0.876	–	0.994	0.991	0.987	0.983
M_{222m}/mH	–	–	15.47	15.05	14.86	–	–	124.06	123.65	123.39
k_{222m}	–	–	0.958	0.927	0.901	–	–	0.995	0.991	0.987
M_{232m}/mH	–	–	–	15.48	15.24	–	–	–	123.97	123.67
k_{232m}	–	–	–	0.958	0.928	–	–	–	0.994	0.990
M_{242m}/mH	–	–	–	–	15.84	–	–	–	–	124.42
k_{242m}	–	–	–	–	0.959	–	–	–	–	0.995

L_{2m} is the self inductance of the secondary coils on m^{th} stage. M_{12m} and k_m are the mutual inductance and the coupling coefficient between the primary and secondary coils on m^{th} stage. M_{2n2m} and k_{2n2m} are the mutual inductance and the coupling coefficient of the secondary coils between n^{th} stage and m^{th} stage ($0<n<5$, $0<m\leqq 5$)

The circuit based on the CST simulation was calculated by Protel Transient/Fourier analysis. From Eq.(7), C_0 is about 21 pF at the operating frequency of 136 kHz. Fig.3 is the circuit of Protel Transient /Fourier analysis.

The Protel Transient/Fourier analysis in Fig.3 began at 0 and ended at 50 ms, with the maximum step of 50 ns and the peak value of input voltage U_1 at 200 V. The analysis results of U_{2m} are given in Fig.4. By connecting the flux compensation capacitors, U_{21}, U_{22}, U_{23}, U_{24} and U_{25} increased to 5.13, 5.20, 5.26, 5.26 and 5.26 kV from 4.74, 4.48, 4.31, 4.22 and 4.18 kV, respectively. Therefore the total output voltage increased from 21.93 kV to 26.10 kV. Also, connecting the compensation capacitors improved uniformity of U_{2m}, averaged at 5.22 kV ±1.1% from the original average value of 4.39±5.2%.

The PICT simulated by CST and Protel was tested with a high frequency switching power supply. Fig.5 shows the excitation signal. U_{2m} with or without flux compensation capacitors was measured by a resistance divider.

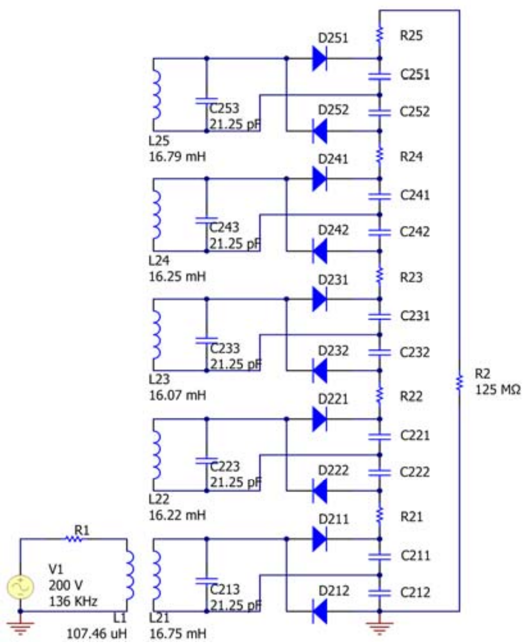

Fig.3 Circuit of Protel Transient/Fourier analysis.

The measured U_{2m} are shown in Fig.6. The voltages were 5.15, 5.10, 5.10, 5.05 and 5.23 kV after connecting the flux compensation capacitors. The measured data agreed well with the simulated data. The flux compensation technique minimizes stage-to-stage voltage differences yielding a higher efficiency design and allows all deck cards to be identical without compromising the voltage rating of the components on the upper stages.

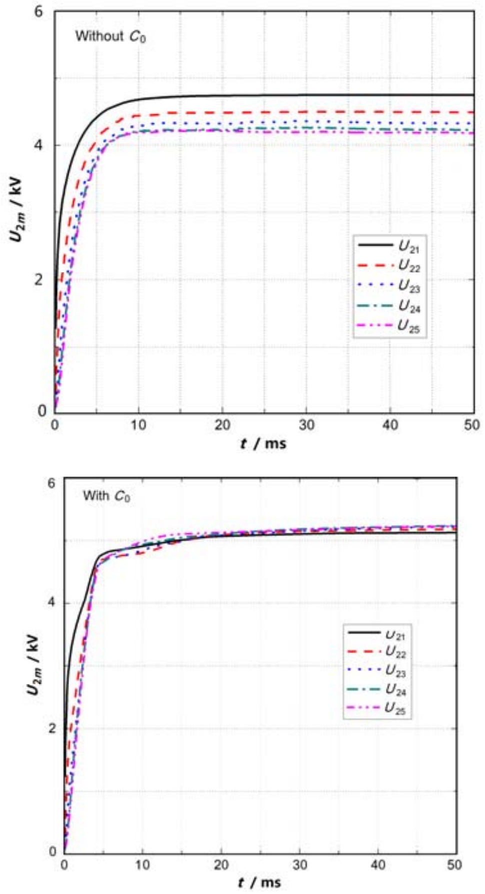

Fig.4 Results of Protel Transient/Fourier analysis with and without C_0.

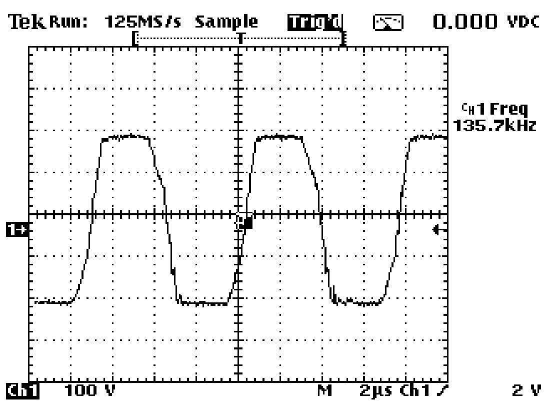

Fig.5 Excitation signal of ICT.

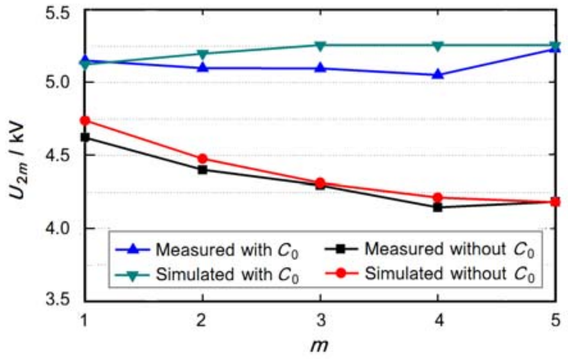

Fig.6 Experiment and simulation results of $u_{2\mathrm{m}}$.

4 Conclusion

Solid insulating materials can reduce the main flux of PICT and cause output voltage to taper off. Theoretical analyses indicated that connecting certain flux compensation capacitor to secondary windings on every stage could compensate the flux loss and increase output voltage effectively. Simulation results of an actual PICT illuminated that the output voltage increases from 21.93 kV to 26.10 kV after being connected to flux compensation capacitors. Voltages generated were equally distributed among stages without compromising the voltage rating of the components on the upper stages. Calculations of design equations and simulation were verified by corresponding experimental test. This indicates that flux compensation capacitors are effective. It's beneficial to optimize the design scheme for building an applicable PICT.

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