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Research into the sampling methods of digital beam position measurement*

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A fully digital beam position monitoring system (DBPM) has been designed for SSRF (Shanghai Synchrotron Radiation Facility). As analog-to-digital converter (ADC) is a crucial part in the DBPM system, the sampling methods should be studied to achieve optimum performance. Different sampling modes were used and compared through tests. Long term variation among four sampling channels, which would introduce errors in beam position measurement, is investigated. An interleaved distribution scheme was designed to address this issue. To evaluate the sampling methods, in-beam tests were conducted in SSRF. Test results indicate that with proper sampling methods, a turn-by-turn (TBT) position resolution better than 1 μm is achieved, and the slow-acquisition (SA) position resolution is improved from 4.28 μm to 0.17 μm.

Keywords: Beam position monitor, Analog-digital conversion, Digital phase-locked loop, Interleaved distribution scheme

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I. INTRODUCTION

Beam position monitors (BPMs) form an indispensable system of a synchrotron radiation source [1–6]. It measures the transverse centroid of the beam in the storage ring and the linac, the linac-to-booster transfer line, the full energy booster, and the booster-to-storage ring transfer line [7]. A digital BPM (DBPM) system was designed for Shanghai Synchrotron Radiation Facility (SSRF), a third generation light source and an important platform in various scientific research domains [1, 5, 6]. Figure 1 shows its block diagram. It receives signals from four capacitive pickup electrodes positioned around the beam pipe. The buttons generate fast pulses at the electron bunch repetition rate of $f_{\mathrm{RF}} = 499.654\,\mathrm{MHz}$ [1]. The input signals are first conditioned by the analogue radio frequency (RF) circuits in four sampling channels of the DBPM, with band-pass filters and amplification circuits. Using RF amplifiers and attenuators, a dynamic range of over 50 dB is achieved [6]. Then, the 499.654 MHz RF signals are digitized by four 14-bit ADCs with a sampling rate of 117.28 MHz, through which digital intermediate frequency (IF) signals of 30.5 MHz are generated. The digital IF signals are further processed by the algorithms integrated within a field-programmable gate array (FPGA) device.

As shown in Fig. 2, the IF signals are converted into I and Q arrays by digital down converters (DDCs) before the amplitudes of four input signals are calculated by the Cordic algorithm. Then, by employing the Δ/Σ principle [8], the beam position can be calculated using Eqs. (1) and (2)

$$X = K_x \frac{V_1 - V_2 + V_3 - V_4}{V_1 + V_2 + V_3 + V_4}, \tag{1}$$

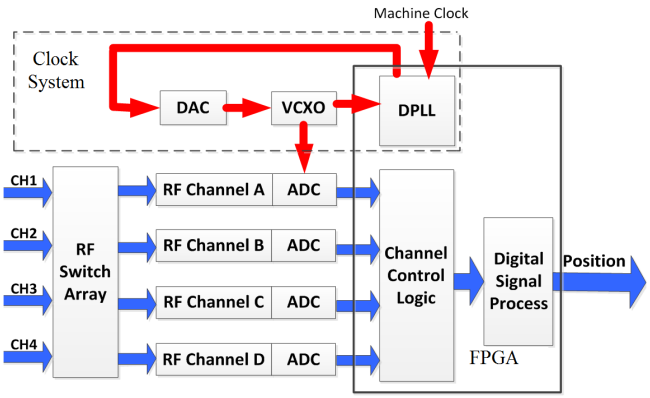

Fig. 1. (Color online) Block diagram of the DBPM designed for SSRF.

$$Y = K_y \frac{V_1 + V_2 - V_3 - V_4}{V_1 + V_2 + V_3 + V_4}, \tag{2}$$

where, $K_x = K_y = 10\,\mathrm{cm}$ are the effective length factors in X and Y directions, and V_{1-4} are amplitudes of signals in four RF channels.

Harmonic number of the SSRF storage ring is $H = 720$, so the turn rate is given by the machine clock frequency $(f_{\mathrm{mc}})499.654\,\mathrm{MHz}/H = 693.964\,\mathrm{kHz}$. Using a low-pass-filter (LPF), the slow-acquisition (SA) data are obtained from turn-by-turn (TBT) data. While the TBT data are used to analyze the beam position spectrum and study the position noise between tens of kHz to hundreds of kHz, the SA data is applied to beam monitoring, with a feedback loop to stabilize the beam orbit [7].

Performance of the ADCs affects measurement resolution of the overall BPM system, so great care must be taken with the sampling method. In this study, we explored the synchronization and the off-tune sampling modes, in the electronics design, which was evaluated through tests. A digital phase-locked loop (DPLL) algorithm was deployed on an FPGA device, enabling the system to implement and switch between different sampling methods used by the ADCs. To address

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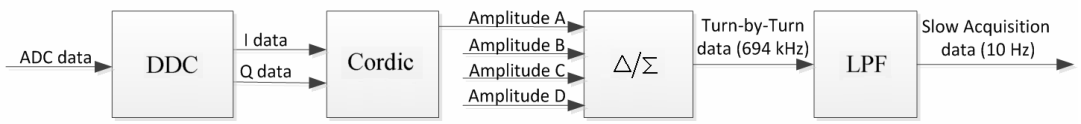

Fig. 2. Block diagram of the digital signal processing.

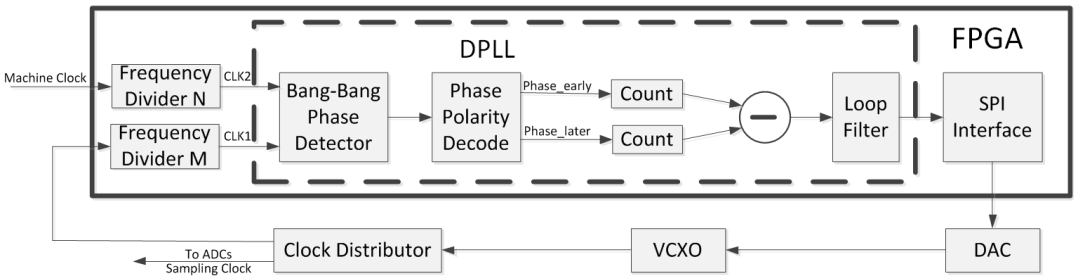

Fig. 3. Block diagram of the clock generation circuits.

the issue of long-term stability of the ADCs and the RF circuits, a switch array was designed to implement interleaved distribution of the input signals among four sampling channels. Results of on-site tests with different sampling methods were compared.

II. SAMPLING METHODS IN THE ADCS

The electron bunches produce RF signals in the BPM pickups with a frequency of $f_{\mathrm{RF}} = 499.654\,\mathrm{MHz}$, which are fed into the DBPM inputs. The signals are modulated by a macro pulse due to the turn frequency given by $f_{\mathrm{mc}} = 693.964\,\mathrm{kHz}(f_{\mathrm{RF}}/H)$. If the ADC sampling clock was not synchronized to the machine clock (f_{mc}), there would be a variation in the number of RF signals per TBT cycle [6]. This variation would cause undue fluctuations in the amplitude measurements, which could finally deteriorate the position resolution. Therefore, the synchronization sampling becomes mandatory for the TBT data, which means the sampling frequency (f_{s}) should be an integer multiple of f_{mc}, as shown in Eq. (3). In such case, the TBT data rate is exactly equivalent to f_{mc}

$$f_{\mathrm{in}}/f_{\mathrm{s}} = 720 f_{\mathrm{mc}}/(169 f_{\mathrm{mc}}) = 720/169. \tag{3}$$

Regarding the SA data, the requirement on the sampling frequency is quite different. As mentioned previously, the TBT data (694 kHz) is filtered by a digital LPF to obtain the SA data with a much lower rate of 10 Hz; therefore, if the sampling clock is not synchronized to the machine clock, the amplitude fluctuation can be filtered out. On the other hand, due to modulation of the macro pulse, sidebands with a frequency interval of f_{mc} exist in the frequency spectrum of the digital IF signal. In the ADCs, the circuit non-linearity causes harmonics of the digital IF signal to appear, which is accompanied by a similar distribution of sidebands. Some of the sidebands around the harmonics would overlap at the digital IF signal frequency ($44 f_{\mathrm{mc}}$), which would cause measurement errors with a very low frequency. This was observed in the SA measurement results of some BPM instrumentations, such as Libera Electron [9]. To address this issue, we should shift f_{s} in Eq. (3) by a certain small frequency difference Δf to relocate the sideband of the harmonics outside of the passband (5 Hz) of the LPF for the SA data [9]. A straightforward idea is to set f_{s} totally independent from f_{mc}, but the problem is that Δf can not be controlled precisely as f_{mc} shifts along with time. In this paper, we use an off-tune sampling mode, in which Δf is set to a certain value that can be modified easily by commands. To accommodate the above sampling modes and switch between them, a DPLL is specially designed based on an FPGA device.

III. SYNCHRONIZATION AND OFF-TUNE SAMPLING BASED ON DPLL

In conventional methods for clock synchronization, commercially available PLL chips are employed, which consist of a phase detector, a charge pumper, and a loop filter implemented in ICs. This is an easy way to design sampling clock generation circuits, however, rendering it impossible to switch between different sampling modes. To achieve good flexibility, we adopted a digital solution based on a modified DPLL in an FPGA device (XC4VFX100-11ff1152 from Xilinx virtex-4 family). The output codes from the DPLL are used to control an external digital-to-analog convertor (DAC) whose output is further fed to a voltage-controlled crystal oscillator (VCXO), as shown in Fig. 3. With different division factors (M and N in Fig. 3), the frequency relationship between the output clock (f_{s}) and the input reference clock (f_{mc}) can be determined.

As a kernel parts in DPLL, the digital phase detector is categorized into the linear type like Hogge phase detector and

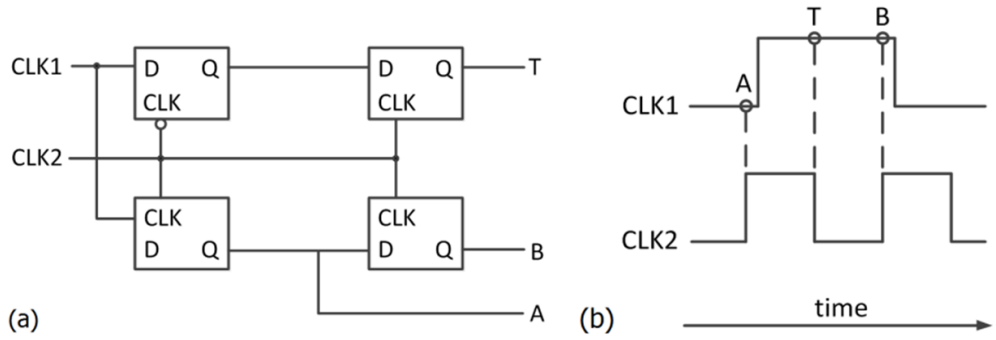

Fig. 4. Structure (a) and principle (b) of a Bang-Bang phase detector.

Fig. 5. (Color online) Simulation result of the Bang-Bang phase detector.

the nonlinear type like Alexander phase detector (i.e., Bang-Bang phase detector) [10, 11]. Alexander phase detector is chosen in the DBPM system, considering its superior performance and simplicity [12]. It outputs 3-bit data indicating which one of the two input signals leads the other. Its structure and principle are shown in Fig. 4, where A, T and B are three samples taken by three consecutive clock edges. If CLK2 leads CLK1, the first sample (A) is unequal to the last two (T and B).

We implemented this digital phase detector in the FPGA, and conducted simulations based on ISim (ISE 14.4). The results agree well with theoretical analysis (Fig. 5). Connecting this phase detector with the loop filter and other components in Fig. 3 implements a whole DPLL. With this scheme, there exists a relationship between the frequencies of two input clocks of the DPLL in the locked state, as shown in Eq. (4)

$$f_{\rm clk2} = 2f_{\rm clk1}. \tag{4}$$

Considering the relationship among the machine clock, the ADC sampling clock, CLK1 and CLK2 in Fig. 3, $f_{\rm s}$ can be expressed as Eq. (5). Then the relationship in Eq. (3) can be achieved with $M = 338$ and $N = 1$

$$f_{\rm s} = Mf_{\rm mc}/(2N). \tag{5}$$

Meanwhile, as mentioned above, to prevent the sidebands of harmonics from deteriorating the SA data, $f_{\rm s}$ should be shifted by a certain frequency difference Δf (i.e. the off-tune sampling mode). In this design, we implemented Δf by configuring a frequency divider with a factor K

$$K = f_{\rm mc}/\Delta f. \tag{6}$$

Thus, in the off-tune sampling mode, $f_{\rm s}$ can be expressed as

$$f_{\rm s} = 169f_{\rm mc} + \Delta f = 169f_{\rm mc} + f_{\rm mc}/K = (169K+1)f_{\rm mc}/K. \tag{7}$$

Comparing Eq. (5) with Eq. (7), the off-tune sampling can be implemented by the DPLL, and the relationships among N, M and K are described by Eq. (8)

$$N = K/2, \quad M = 169K + 1. \tag{8}$$

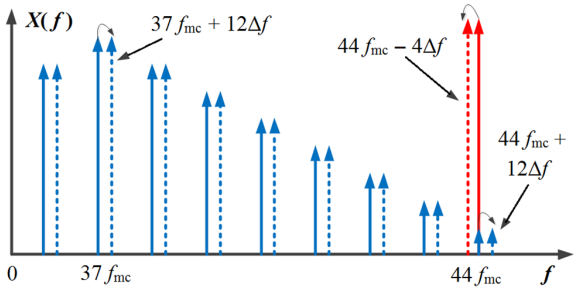

Fig. 6. (Color online) Sidebands of 3rd harmonic and IF baseband signal.

The next step is to determine the Δf value. The major influence comes from the sideband $(44f_{\rm mc})$ of the third harmonic $(37f_{\rm mc})$ overlapping on the digital IF signal [9]. As shown in Fig. 6, in the off-tune sampling mode, the sideband of the third harmonic and the digital IF signal are shifted by $12\Delta f$ and $-4\Delta f$, respectively, i.e. a total frequency interval

of $16\Delta f$ is achieved. To guarantee that the sideband can be effectively suppressed by the LPF (5 Hz pass band) for the SA data, the value of Δf should meet the requirement as follows

$$16\Delta f > 5\,\text{Hz}. \tag{9}$$

Meanwhile, considering the frequency tuning range of the VCXO (VFVX 120), the upper limitation of Δf is

$$\Delta f < 5.85\,\text{kHz}. \tag{10}$$

Combining Eqs. (9), (10) and (6), one obtains that the K value ranges from 118 to 2221

$$5\,\text{Hz}/16 < \Delta f_{\text{mc}}/K < 5.85\,\text{kHz} \rightarrow 118 < K < 2221. \tag{11}$$

In the design of DPLL, K is chosen as 256, and the corresponding values of N and M are 128 and 43 265. The final sampling frequency in the off-tune mode can be expressed as

$$\begin{aligned} f_{\text{s}} &= Mf_{\text{mc}}/(2N) \\ &= 43265f_{\text{mc}}/(2\times 128) \\ &= 169f_{\text{mc}} + f_{\text{mc}}/256. \end{aligned} \tag{12}$$

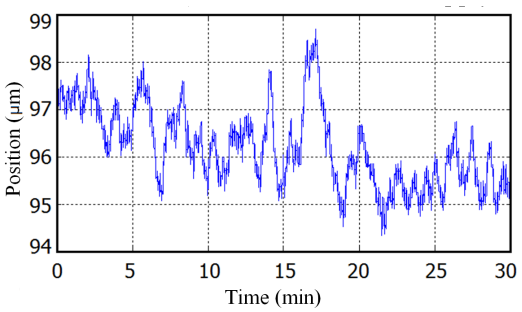

Fig. 7. (Color online) Y position waveform of the SA data.

IV. CONSIDERATION OF LONG-TERM STABILITY

In the DBPM, the SA data are mainly used to monitor long term variation of the beam position [7]. The beam position is calculated from the input signal amplitudes (A_1, A_2, A_3, A_4) multiplied by the gains of four sampling channels (G_1, G_2, G_3, G_4), as shown in Eqs. (13) and (14)

$$\begin{aligned} X &= K_x\frac{V_1 - V_2 + V_3 - V_4}{V_1 + V_2 + V_3 + V_4} \\ &= K_x\frac{G_1A_1 - G_2A_2 + G_3A_3 - G_4A_4}{G_1A_1 + G_2A_2 + G_3A_3 + G_4A_4}, \end{aligned} \tag{13}$$

$$\begin{aligned} Y &= K_y\frac{V_1 + V_2 - V_3 - V_4}{V_1 + V_2 + V_3 + V_4} \\ &= K_y\frac{G_1A_1 + G_2A_2 - G_3A3 - G_4A_4}{G_1A_1 + G_2A_2 + G_3A_3 + G_4A_4}, \end{aligned} \tag{14}$$

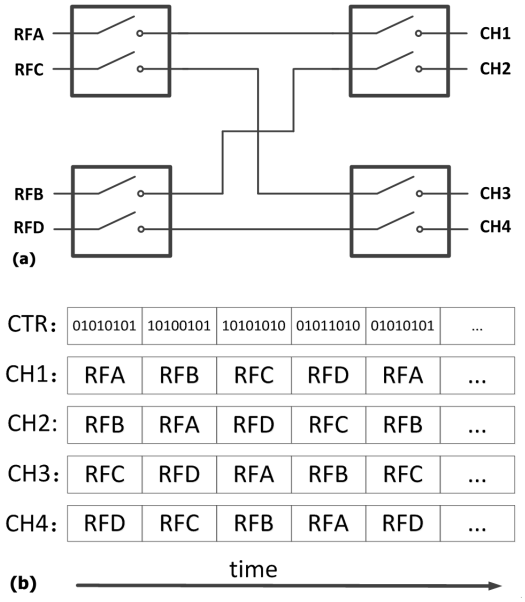

Fig. 8. Structure (a) and time diagram (b) of the switch array.

where $K_x = K_y = 10$ cm are the effective length factors in X and Y directions; G_{1-4} are the gain of the sampling channels; and A_{1-4} are amplitude of the input signals.

In the ideal situation, the four gain factors are equal and there are no measurement errors in beam position results; however, it is not the case in real applications. If the difference among the four gain factors keeps constant, the measurement error in SA data can easily be corrected by off-line calibration. However, we found that these gain factors change quite differently, which would inevitably deteriorate the resolution of the SA data in long term. As shown in Fig. 7, fluctuation of the SA data are obvious (the corresponding position resolution is 0.832 μm) in the laboratory tests where the input signals were generated by a signal sources (ROHDE & SCHWARZ SMA 100A). Therefore, we must apply new methods to address this issue.

The basic idea is to distribute the four input signals to the four sampling channels alternately according to a specified sequence. We designed an interleaved distribution scheme by using an RF switch array with the structure shown in Fig. 8(a) [13]. With different controlling signals, this switch array establishes corresponding signal paths between the four input ports and the four sampling channels. The control signals are generated by the FPGA, and are organized in a special sequence, with which the four input signals are evenly interleaved to four channels, as shown in Fig. 8(b). The switching frequency is designed as 5.42 kHz, which is much larger than the pass band (5 Hz) of the LPF for the SA data in Fig. 2. So the distortion introduced by the switching process can easily be filtered out. In this case, the four sampling channels have equivalent influence on the processing of each input signal, which means the equality of effective gains for all input signals, i.e., the measurement errors caused by the long term fluctuation of electronics are greatly suppressed.

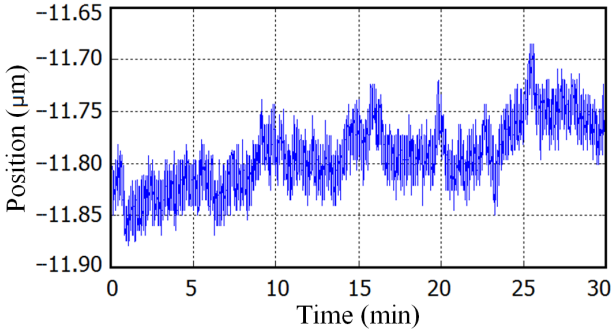

Fig. 9. (Color online) Y position waveform of the SA data with the interleaved distribution scheme.

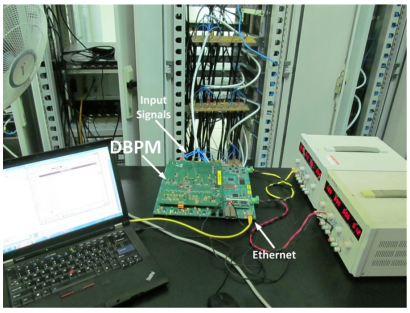

Fig. 10. (Color online) DBPM under commissioning tests in SSRF.

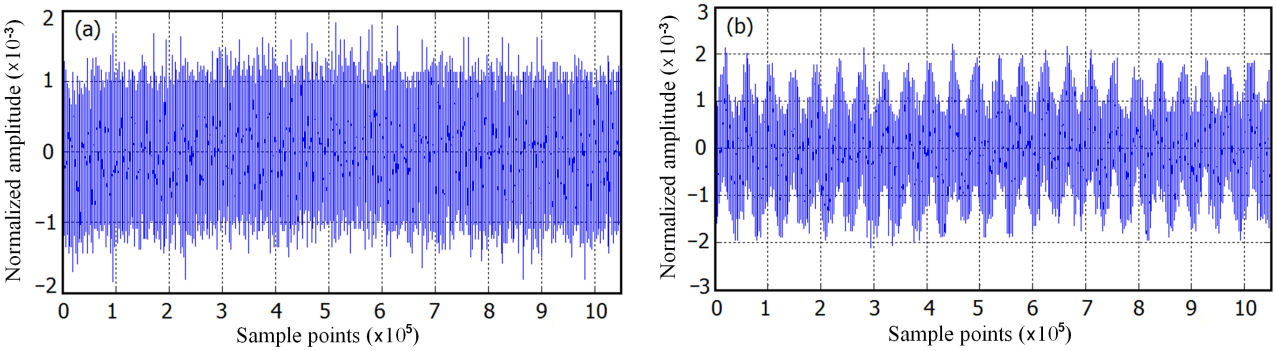

Fig. 11. (Color online) Amplitudes in synchronization sampling (a) and off-tune sampling (b).

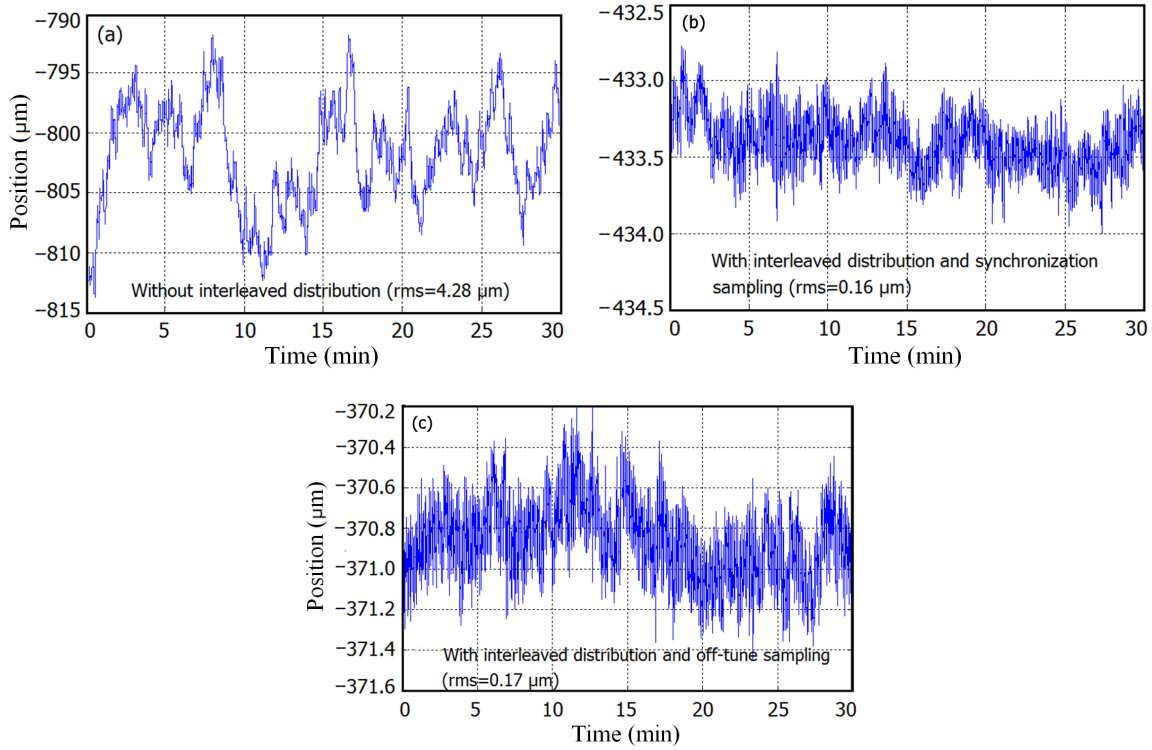

Fig. 12. (Color online) Y position waveform of the SA data under different conditions.

Results of initial tests conducted in laboratory are shown in Fig. 9. The position information of the SA data in 30 min is stable and the resolution is around 0.032 μm, rather than 0.832 μm in Fig. 7.

V. TEST RESULTS

To evaluate overall performance of the DBPM in different sampling methods, we conducted commissioning tests in SSRF (Fig. 10). The modulated RF signals from pickups were sent to the DBPM through four coaxial cables. After manipulating the signals, the DBPM sent the beam position information to a remote PC through ethernet for further analysis.

A. Results of the TBT data

We tested the TBT data in two modes: the synchronization sampling and the off-tune sampling. The normalized signal amplitudes of the TBT data in both sampling modes are shown in Fig. 11. Fluctuation can be clearly observed in Fig. 11(b), just as discussed in Sec. II. Therefore, the synchronization sampling is chosen for the TBT data, and the position resolution is around 0.61 μm.

B. Results of the SA data

As shown in Fig. 12, the interleaved distribution scheme we designed can improve performance of the SA data significantly; the position resolution of a 30-min data collection test could be enhanced from 4.28 μm to 0.17 μm. And similar performance can be achieved in the synchronization sampling and the off-tune sampling, as shown in Figs. 12(b) and 12(c). This is probably due to the good performance of the analog front-end in the DBPM system.

VI. CONCLUSION

Different kinds of sampling methods are studied to optimize the performance of the DBPM designed for SSRF, including the synchronization sampling, the off-tune sampling and the interleaved distribution scheme which aims to address the long term stability. The commissioning test results in SSRF indicate that with an optimized sampling method, a TBT position resolution is better than 1 μm. It was found that the SA resolution can be effectively enhanced to 0.17 μm using an interleaved distribution scheme. Both the position resolutions of the TBT and the SA data exceed the technical requirements.

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