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Magnetic flux leakage analysis and compensation of high-frequency planar insulated core transformer*

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A novel high-frequency and high power density planar insulated core transformer (PICT) applied to high voltage DC generator is introduced. PICT's operating principle and fundamental configuration are described, and preliminary experimental results in self-designed PICT apparatus are presented. Emphatically, magnetic leakage flux (MFL) giving rise to the output voltage drop is analyzed in detail both theoretically and by finite element method (FEM). Showing good consistency with experimental result, FEM simulation is considered to be practicable in physical design of PICT. To cancel out leakage inductance and improve the voltage uniformity, compensation capacitor is adopted and experimental verification is also presented. All shows satisfactory results.

Keywords: Planar insulated core transformer, Load operation, Magnetic flux leakage, Leakage inductance, Finite element analysis, Flux compensation.

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I. INTRODUCTION

Planar insulated core transformer (PICT) is a novel high-voltage and high power direct current (DC) generator demonstrating both properties of insulated core transformer (ICT) [1–3] and planar transformer [4, 5]. Being advantageous over conventional line-frequency transformers [6, 7] in its compact structure, low stored energy, excellent transient response, high efficiency, good fault tolerance and high reliability, PICT is promising to be used in DC power supply below 1 MV.

PICT is driven by switching power supply and generally its magnetic core is made of ferrite. Secondary coils are arranged as tracks on printed circuit boards (PCB). Plurality of PCB stacks are connected in series so that output stage can generate a DC voltage in excess of 100 kV and a current of 50–200 mA.

Figure 1(a) shows schematically an experimental PICT implementation we developed. Energized by a 33 kHz AC signal generated by pulse width modulated inverter, the PICT has 5 turns in primary windings, and comprises 27 PCB stacks. Each PCB circuit contains 32 identical secondary modules, and each module consists of 2 turns of secondary coils and a full wave bridge rectifier (Fig. 1(b)).

Assuming no losses, when excited by an excitation signal of amplitude U_{P}, the output DC voltage U_{DC} is

$$U_{\mathrm{DC}} = 2\frac{N_2}{N_1}U_{\mathrm{P}} = 2\frac{32\times 27 n_2}{N_1}U_{\mathrm{P}}, \qquad (1)$$

where N_1 and N_2 are the number of turns in primary and secondary windings, respectively; and n_2 is the number of turns in each secondary module.

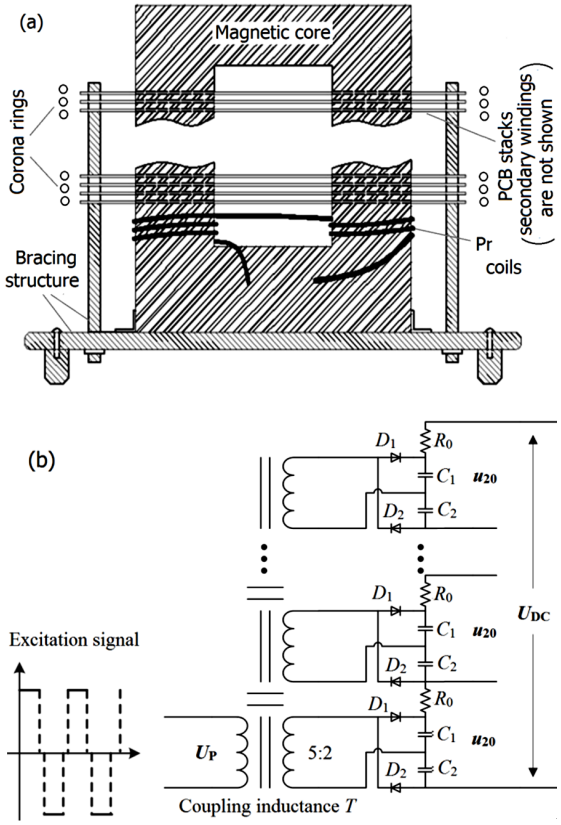

Fig. 1. Sectional view (a) and circuit (b) of the PICT.

Sized at just Φ500 mm × 600 mm, the PICT works at $U_{\mathrm{P}} =$ 520 V in a tank filled with SF6. According to Eq.(1), it shall output a DC voltage of over 300 kV. However, from open-loop experiments, we had $U_{\mathrm{P}} = 400$ V and $U_{\mathrm{DC}} = 220$ kV in the no-load test; with the load, we had $U_{\mathrm{P}} = 200$ V and $U_{\mathrm{DC}} = 100$ kV at output current of 15 mA due to limited power of the front-end power supply.

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II. THEORETICAL ANALYSIS OF MAGNETIC FLUX LEAKAGE IN PICT

The measured DC output of the PICT exhibited a severe drop compared to theoretical value, and magnetic leakage flux (MFL) was considered as an essential reason. To isolate associated ferrite tiles from neighboring magnetic core, adjacent PCB stacks were isolated by insulating films of low magnetic conductivity μ to form gaps in the magnetic circuit. MFL occurred at fringes of gaps in form of "by-pass" flux, as a result the upper section of the magnetic core carried less flux. Figure 2 is a schematic diagram of insulating film and by-pass flux.

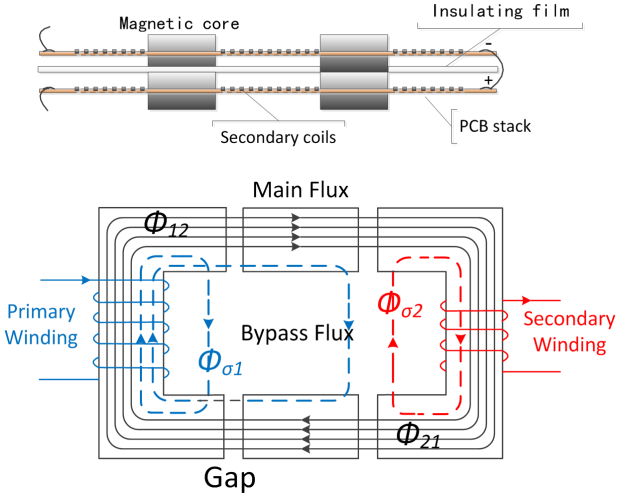

Fig. 2. (Color online) Insulating film (a) and by-pass flux (b) in transformer.

Number the 27 PCB stacks as $m_1, m_2, \cdots, m_N, \cdots, m_{27}$ from bottom to top. The 28 magnetic gaps introduced by 27 isolation layers give rise to flux leakage $\Delta\Phi$, which is proportional to the main flux Φ of that position [8, 9], i.e.,: $\Delta\Phi \propto \Phi$. $\Delta\Phi$ makes $K_N < 1$, where K_N is the magnetic coupling efficiency in the N^{th} PCB. So the output voltage U_N determined by K_N decreases along the vertical

$$U_N = U_0 K_N \qquad (0 < K_N < 28, \quad 0 < N < 28), \quad (2)$$

where, K_N is mainly up to the width of gap, i.e., thickness of insulating films.

Therefore, the MFL causes voltage losses through reducing K_N of the upper stages. The MFL-caused leakage inductance in the equivalent circuit is shown in Fig. 3, where $T = 5 : 2$ is the ratio of coupling inductance; the subscripts L, P and S denote the load resistance, primary coil and secondary coil, respectively; L_{kp} and L_{ks} are the leakage inductance; and C_{P} and C_{S} are the stray capacitance. In the no-load test, the R_{L} branch was a high impendence path, so L_{kp} and L_{ks} formed with C_{S} a series resonant circuit and did not reduce the voltage across R_{L}. When the current flowing through R_{L} became mA level, electric resonance would disappear, by then the voltage would be allocated to leakage inductance and R_{L} voltage will reduces.

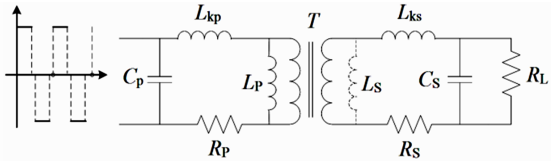

Fig. 3. Equivalent circuit of one module in PICT

MFL is often a significant single factor in degrading the performance of PICT. It not only leads to voltage drop but also break the voltage uniformity between PCB stacks. So it is necessary to figure out the value of K_N and then manage to compensate it. Our early studies [10, 11] with a preliminary no-load test on a primitive PICT apparatus comprising 5 PCB cards showed different properties from reality. To study the characteristics of MFL in load operation, finite element simulation and experiments were carried out.

III. MAGNETIC FIELD ANALYSIS USING CST

Theoretically, by analyzing magnetic field energy contained in the transformer windings [12, 13], leakage flux can be calculated, but it is only suitable for qualitative analysis. Finite elements analysis is more applicable to numerical analysis. Using CST FEM studio, we performed magnetic field simulation of the PICT. In the model, the primary windings have 5 turns, and the exciting current is 50 A. The cross section of magnetic core is 0.01 m^2. The relative permeability μ_0 is 2400 and the gap width is 0.15 mm. The mesh number is 6×10^5, and the computational accuracy is 10^{-6}. CST gives the magnetic field density B in model space. The results are shown in Fig. 4. The by-pass flux is the foremost source of leakage flux.

Integrating B across the 27 PCB sections to get magnetic flux Φ, we had the magnetic flux data of 27 PCB stacks gapped 0.15 mm, as shown in Fig. 5. The Φ curve is close to an exponential distribution, being $\Phi_1 = 7.791 \times 10^{-4}$ Wb for the bottom planar and $\Phi_{27} = 6.672 \times 10^{-4}$ Wb for the top planar. In the simulation $B = 800$ Gs, so theoretically Φ should be 8.0×10^{-4} Wb. It can be calculated $K_1 = 0.974$ and $K_{27} = 0.834$. Figure 5 shows also simulation results of 0.1- and 0.3-mm gap widths, with $K_1 = 0.980$ and $K_{27} = 0.887$ at 0.1-mm gap width, while $K_1 = 0.944$ and $K_{27} = 0.740$ at 0.3-mm gap width. As discussed above, the gap width is the most significant factor affecting the leakage flux, and using thinner insulating films is beneficial to lessen leakage flux.

IV. EXPERIMENTAL PHENOMENON

Tests with and without load were performed. To measure DC output voltage of all PCB stacks, in each PCB the input terminals were grounded and output ports were connected to load resistance R_{L}. The insulating films are 0.15 mm thick-

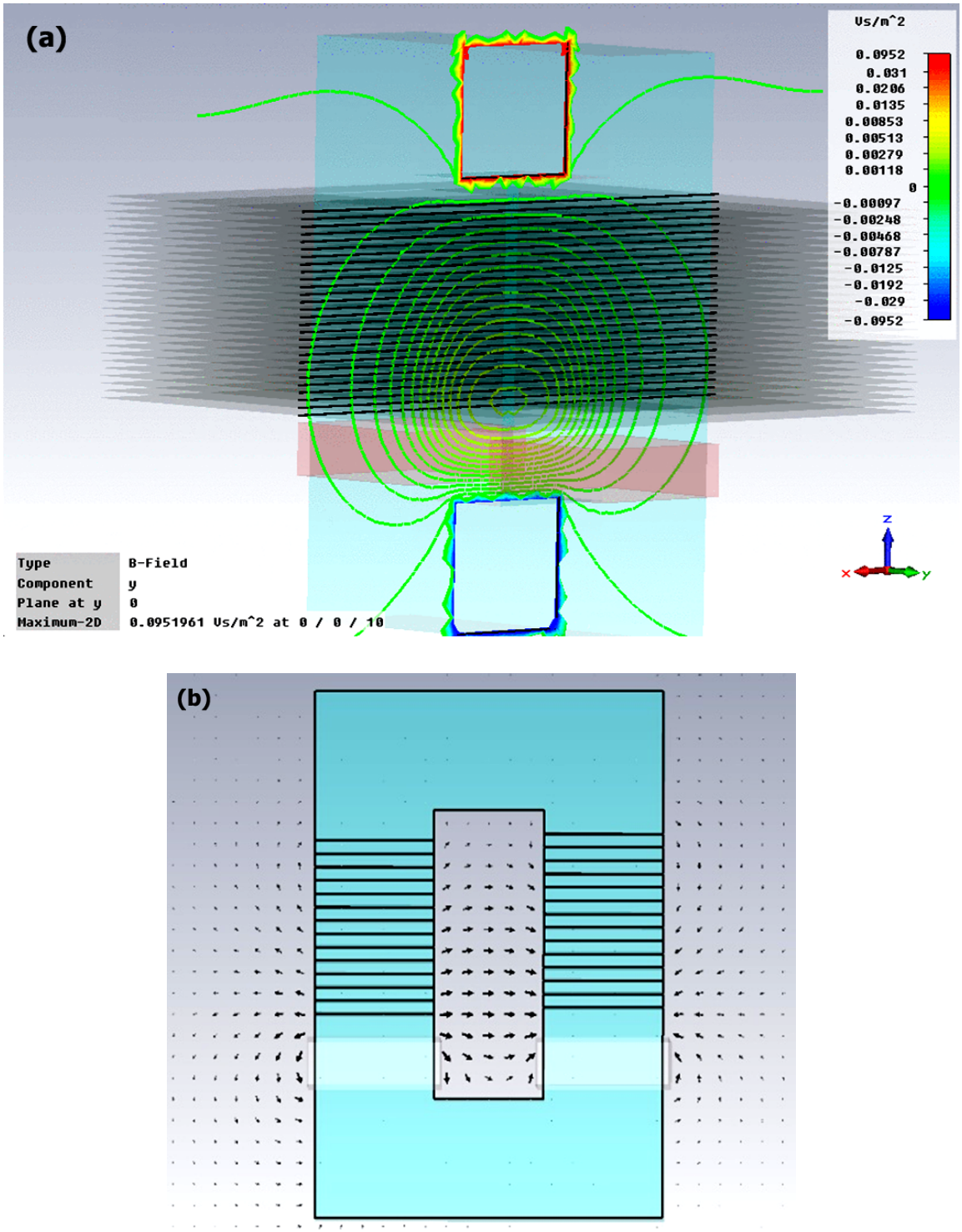

Fig. 4. (Color online) By-pass flux in PICT. (a) contour line of by-pass flux across XZ plat, (b) magnetic field line of by-pass flux.

ness. In the load test, $R_{\mathrm{L}} = 120\,\mathrm{k\Omega}$ and the load current was 7 mA; while in no-load test, $R_{\mathrm{L}} = 1000\,\mathrm{M\Omega}$. Figure 6(a) shows the voltage curve. The bottom PCB output was 824 V and the top one was 704 V in the load test, with a 14.6% drop. By contrast, the no-load output values were quite similar. The two curves show a broad distinction consistent with theoretical analysis. According to repeated tests, the drop between the bottom and top PCB was 13%–17%, showing a good coincidence with CST simulation. Figure 6(b) shows the experimental results and the CST simulation.

Conclusively, in load operation of the PICT, MFL causes a lower generated voltage on the upper PCB stacks and reduces

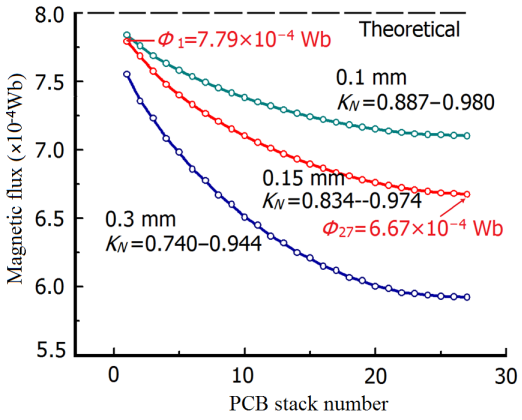

Fig. 5. (Color online) The magnetic flux in models of different gap width.

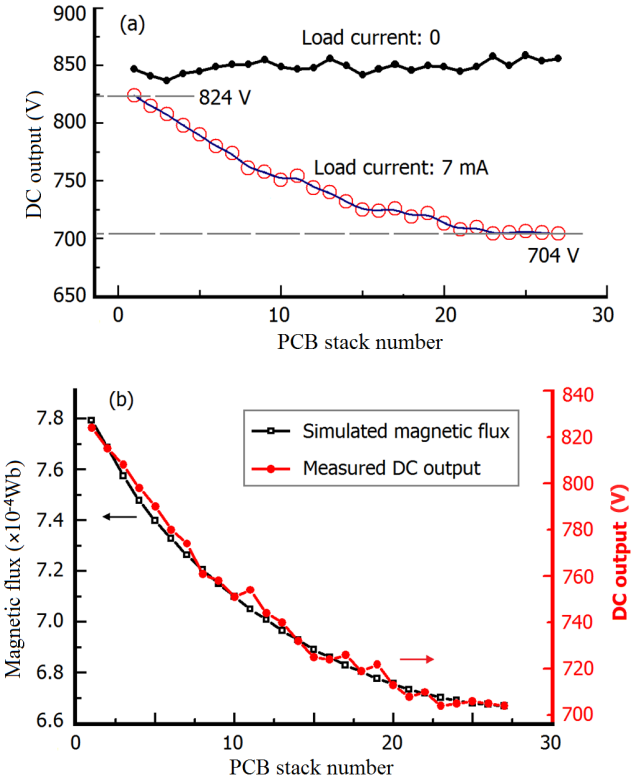

Fig. 6. (Color online) By-pass flux in PICT. (a) contour line of by-pass flux across XZ plat, (b) magnetic field line of by-pass flux.

voltage efficiency. A numerical basis for PICT design can be provided by accurate CST calculation of the magnetic field.

V. COMPENSATION TO FLUX LEAKAGE

After obtaining the value of leakage flux, which working as leakage inductance in equivalent circuit, we managed to compensate it. The method of winding more secondary coils proposed in Ref. [3] is not suitable to PICT. A more practical alternative is to connect suitable compensation capacitor across the secondary coil [10, 11, 14–16].

We calculated and optimized the value of compensation capacitor using Multisim. To make DC voltage of the upper PCB stacks of low K_N output similar to the bottom ones, 33 nF capacitor is required in our PICT apparatus. What noteworthy is that the capacitances in different PCB stacks are nearly equal.

To evaluate performance of the compensation capacitor, Multisim simulation over three individual secondary modules of different K_N was carried out. The simulation circuit is the same as circuit shown in Fig. 2. The three coupling inductances were T_1, T_2 and T_3, where the coupling efficiency of T_1 was 0.8, representing the top PCB; the coupling efficiency of T_2 was 0.9, representing the intermediate PCB; and the coupling efficiency of T_1 was 0.98, representing the bottom PCB. The compensation capacitors across the secondary coil were 33 nF. Figure 7 shows the output voltage before and after compensation, where the red, green and blue lines are outputs of T_1, T_2 and T_3, respectively. The three outputs are distinct before compensation, while after compensation they are pretty much the same, in a higher value than before.

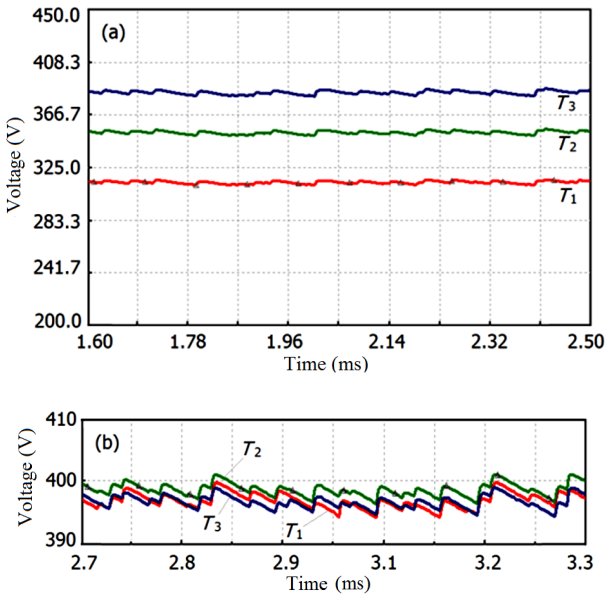

Fig. 7. (Color online) Multisim simulation of output voltage before (a) and after (b) compensation.

To verify above simulation, 2.2 nF and 33 nF capacitors were installed in the topmost PCB and DC voltages were measured. The results are given in Table 1. The 33 nF capacitor made voltage generation being equally distributed between PCB stacks, while other two did not. All these demonstrate that proper capacitance selection of the compensation capacitor is an effective and satisfactory way to improve magnetic leakage of the PICT.

TABLE 1. The effect of compensation capacitor

Value (nF) of capacitor	Bottommost PCB (V)	Topmost PCB (V)	
		No compensation	Compensated
0.0	552	470	470
2.2	550	470	473
33.0	556	472	570

VI. CONCLUSION

In this paper MFL in PICT is studied and proved to be a significant factor causing voltage drop. CST calculation is introduced, and the comparison between experiment and simulation results indicate that CST can describe MFL clearly by quantitative calculation. Compensation capacitor is used to minimize leakage inductance in load test and the desired results are achieved through experimental verification. This research has scientific and applied significance for the construction of new style of high-power DC source.

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