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Nuclear Science and Techniques, Vol.17, No.1 (2006) 29–33
NUCLEAR SCIENCE AND TECHNIQUES

Numerical study of self-heating effects of small-size MOSFETs fabricated on silicon-on-aluminum nitride substrate

DING Yan-Fang [1] ZHU Ming [2] ZHU Zi-Qiang [1] LIN Cheng-Lu [2]

[1](*Department of Electronics Science and Technology, East China Normal University, Shanghai 200062, China)*

[2](*Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China)*

Abstract Compared with bulk-silicon technology, silicon-on-insulator (SOI) technology possesses many advantages but it is inevitable that the buried silicon dioxide layer also thermally insulates the metal – oxide – silicon field-effect transistors (MOSFETs) from the bulk due to the low thermal conductivity. One of the alternative insulator to replace the buried oxide layer is aluminum nitride (AlN), which has a thermal conductivity that is about 200 times higher than that of SiO_2 (320 $W \cdot m^{-1} \cdot K^{-1}$ versus 1.4 $W \cdot m^{-1} \cdot K^{-1}$). To investigate the self-heating effects of small-size MOSFETs fabricated on silicon-on-aluminum nitride (SOAN) substrate, a two-dimensional numerical analysis is performed by using a device simulator called MEDICI run on a Solaris workstation to simulate the electrical characteristics and temperature distribution by comparing with those of bulk and standard SOI MOSFETs. Our study suggests that AlN is a suitable alternative to silicon dioxide as a buried dielectric in SOI and expands the applications of SOI to high temperature conditions.

Key words Self-heating effect, Silicon-on-aluminum nitride (SOAN), Drain current, Temperature distribution

CLC numbers TN305.3, TN403

1 Introduction

Silicon-on-insulator (SOI) technology possesses many advantages over bulk silicon technology such as the reduction of parasitic capacitance, excellent sub-threshold slope, elimination of latch up, and resistance to radiation.[1] Hence, it is preferred for high-speed, high-temperature, and low-power microelectronic devices. SOI MOS devices employ a thin layer of insulating material, usually made of silicon dioxide, to electrically insulate the device from the bulk of the semiconductor. It is inevitable that this thin insulating layer also thermally insulates the MOSFET from the bulk due to the low thermal conductivity of the oxide. [2] The result is that heat generated in the SOI MOSFET causes a much greater temperature rise than in a bulk device under similar conditions, and the self-heating effect becomes an inherent issue for MOSFETs built in SOI. The self-heating effect results in reduced carrier mobility and corresponding decrease in the drain current transconductance and speed. As the device geometries shrink and the transconductance as well as current density increase with MOS scaling, the self-heating effect becomes more pronounced. To reduce the temperature rise due to self-heating effect, reduction of the buried oxide thickness, quasi-SOI technology, and other methods were used.[3] But these solutions cause other disadvantages.[4-6] So, some new structures of SOI have been studied, such as silicon-on-aluminum nitride (SOAN),

Supported by the Special Funds for Major State Basic Research Projects (No.G2000036506) and the National Natural Science Foundation of China (No. 60476006)

Received date: 2005-11-07

SOI multi-layers (SOIM), ground planes SOI (GPSOI), GeSi-on-insulator (GeSiOI), and silicon-on-nothing (SON).

One of the interesting candidates for such novel buried insulators is aluminum nitride (AlN),[7] owing to its excellent thermal conductivity, thermal stability, high electrical resistance, and a thermal expansion coefficient close to that of silicon. In particular, the thermal conductivity of AlN is almost 200 times higher than that of SiO_2 (3.2 $W \cdot cm^{-1} \cdot K^{-1}$ v.s. 0.014 $W \cdot cm^{-1} \cdot K^{-1}$) and that of silicon itself (1.45 $W \cdot cm^{-1} \cdot K^{-1}$). [8] All these properties cause AlN to be used as a buried insulator material in SOAN structure to mitigate self-heating produced in SOI materials. Hence, SOI devices can be used in high temperature conditions.

In this paper, as a first step to address the self-heating effect, numerical simulation was conducted comparing the electrical characteristics and thermal distribution of bulk, SOI, and SOAN MOSFETs. The analysis was carried out using a two-dimensional device simulator called MEDICI run on a Solaris workstation. [9]

2 Device design and simulation

The device simulator MEDICI has been widely used by researchers. It can accurately describe the behavior of MOSFET by solving the electron and hole's energy balance equations, Poisson's equation, electron and hole's continuity equations as well as electron and hole's current density equations. There is a lattice temperature advanced application module (LT-AAM) in the MEDICI simulator, which can couple electrical and thermal characteristics without any complicated experiments. The simulation can provide fast turn-around and quick design time. To describe the self-heating effects of devices, the temperature of lattice T_L is introduced into MEDICI in our simulation. Poisson's equation, current continuity equation, and heat equation are solved in a completely coupled manner to obtain T_L. In our simulation, two sets of curves are generated for the cases with and without lattice temperature effects by solving the above equations. To use MEDICI to solve these equations, a MOS device structure and relevant geometrical and technological parameters, shown in Table 1, were used.

The channel lengths of SOI and SOAN devices are 30 nm, 50 nm, 60 nm, and 90 nm, respectively. For comparison, simulation was also conducted on MOS devices fabricated in bulk Si and standard SOI using SiO_2 as the buried insulator. It should be emphasized that no attempt was made here to optimize the device structure because the focus of this work was high temperature applications of SOAN, and so only one simple structure was chosen for demonstration.

Table 1 Basic parameters of SOI MOSFET used in MEDICI simulation

Parameters	Values
Length of channel / nm	30, 50, 60, 90
Thickness of top silicon (t_{Si}) / nm	20
Thickness of gate oxide (t_{ox}) / nm	2
Thickness of buried oxide ($t_{AlN,\ SiO_2,\ Si}$) / nm	50
Doping of channel (p-type) / cm^{-3}	1×10^{15}
Doping of source/drain (n-type) / cm^{-3}	1×10^{20}

3 Simulation results and discussion

With the channel length of 50 nm, our investigation on the high-temperature performance of MOS device fabricated in SOAN in comparison with those fabricated in bulk Si and SOI substrate included the simulation of the drain leakage, output characteristics, and temperature distribution. Furthermore, we investigated the nuances of the MOS devices fabricated in SOAN with different channel lengths.

3.1 Drain leakage simulation

In this case, the gate bias V_G is held at 0 V, and the drain bias is ramped up to 3 V. The drain leakage current simulation results are shown in Fig. 1.

As is already known, the leakage current due to electron–hole pair generation in the source and drain p-n junction depletion regions will be larger in a bulk device than in the SOI device, as the former has much thicker depletion regions. However, in our simulated curves, we noticed that the bulk leakage was lower in SOI and SOAN. This is because the top silicon layers of our chosen SOI and SOAN devices were fully depleted, which means that the drain depletion region is able to punch through to affect the source-channel energy barrier. Hence, the barrier to electron flow be-

tween the source and drain is much lower in the SOI and SOAN device than in the bulk device, and consequently, the SOI leakage is higher.

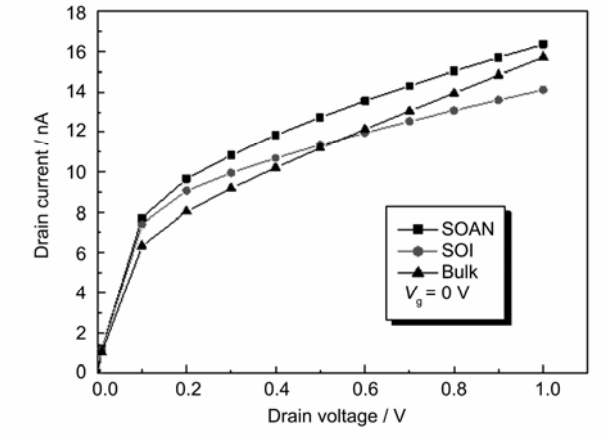


Fig.1 Simulated leakage drain currents of bulk, SOI, and SOAN devices.

3.2 Output characteristics simulation

In this simulation, the gate bias is held at 1 V because the length of the channel is only 50 nm. The drain bias is ramped up from 0 to 2 V. In this operating region we tested whether the self-heating effect occurs at low gate and drain biases despite smaller channel lengths. The simulation result is shown in Fig. 2.

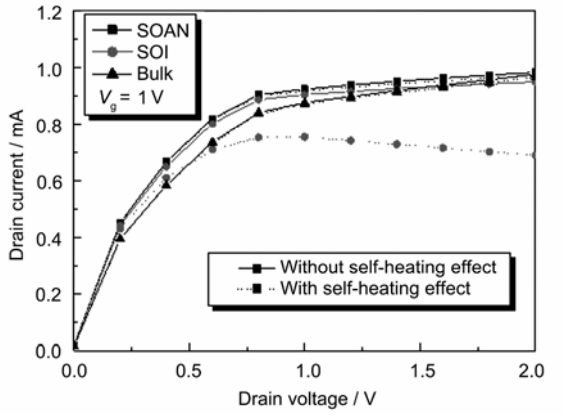


Fig.2 Simulated output characteristics of bulk, SOI, and SOAN devices.

As shown in Fig.2, the SOI device shows strong negative differential resistance (NDR), but on the other hand, both the SOAN and bulk devices display weak NDR under the same conditions. It is known that the higher the self-heating effect, the more obvious the NDR.. As the mobility is sensitive to the temperature and decreases as the temperature rises, the drain current also diminishes due to the degradation in the mobility and emergence of the NDR. We thus examined the self-heating effect by studying the NDR on the I_{DS}-V_{DS} curves and it can be concluded that the SOI device is subject to a higher self-heating effect than that in SOAN and bulk devices under the same operating conditions. This is because AlN has a thermal conductivity that is about 200 times higher than that of SiO_2 and roughly equal to that of silicon itself.

3.3 Temperature distribution simulation

The temperature distribution obtained under the same simulation conditions is consistent with the output characteristics. Fig. 3 shows the relation between the channel temperature and the drain voltage, where it can be found directly that when SOI devices are operating, the channel temperature will rise extremely fast with the increase of drain voltage but in SOAN devices, it will not. It is because the heat generated in the operation of the device could not be expelled due to the low thermal conductivity of SiO_2 and naturally the self-heating effect comes into being.

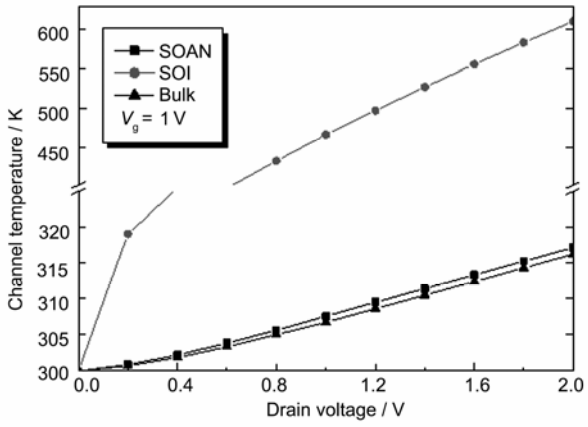
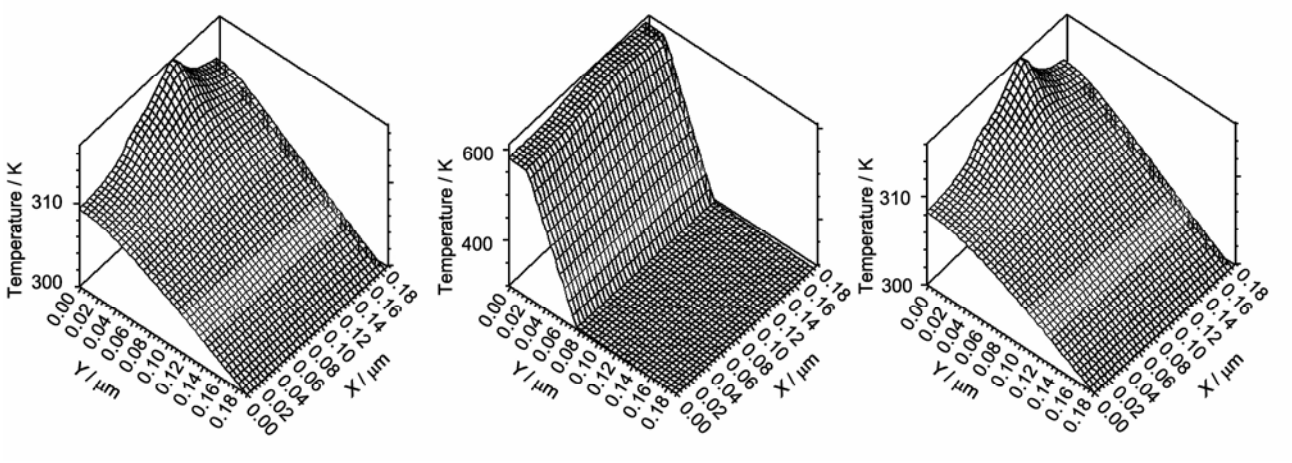


Fig.3 T_c—V_d relationship in bulk, SOI, and SOAN devices.

The three-dimensional (3-D) temperature distribution patterns in the SOAN, SOI, and bulk devices are displayed in Fig. 4(a), (b), (c), respectively. The *x* and *y* axes represent the horizontal and vertical dimensions of the device, respectively. The gate bias is held at 1V and the drain bias is at 2 V. The temperature in the substrate is only 300 K, but because of self-heating, the channel temperature in SOI device rises to 610 K. The channel temperature in SOAN and

bulk devices decreases significantly to about 316 K, which is only slightly higher than the substrate temperature. Our results indicate that the influence of self-heating effect in SOI is much more serious than in SOAN and bulk silicon, because the majority of the heat generated during the operation of the device could spread into the silicon substrate through the buried AlN layer in the SOAN device like in the bulk device.



(a) SOAN device (b) SOI device (c) Bulk device

Fig. 4 Simulated 3-D temperature distribution of (a) SOAN, (b) SOI, and (c) the bulk device.

3.4 Simulation in SOAN and SOI devices with different channel lengths

McDaid[10] reported a formula pertaining to the difference between the channel and ambient temperature ΔT_C:

$$\Delta T_c = \frac{P_t \cdot t_b}{K_b A}$$

where t_b is the thickness of the buried layer, K_b is the thermal conductivity of the buried layer, and A is the area over which the power is generated (taken as the effective channel length multiplied by the device width). So on second thoughts, we investigated the nuances of self-heating effects in the SOAN devices and in SOI devices due to different channel lengths. The results are shown in Fig.5 (a) and Fig.5 (b).

As shown in Fig. 5(a) and Fig.5 (b), at the same room temperature and thickness of the buried insulator in SOI and SOAN device, ΔT_c of the SOAN structure used in a small-size device is much smaller than that of the SOI device according to the above formula no matter what the channel length (30, 60 or 90 nm) is. So we could predict that because of the significantly larger thermal conductivity of AlN compared to that of SiO_2, the small-size MOSFETs fabricated on SOAN substrate are more attractive than those on SOI substrate in micro-electronic applications where thermal effects are to be taken into account, particularly when thermal dissipation is needed.

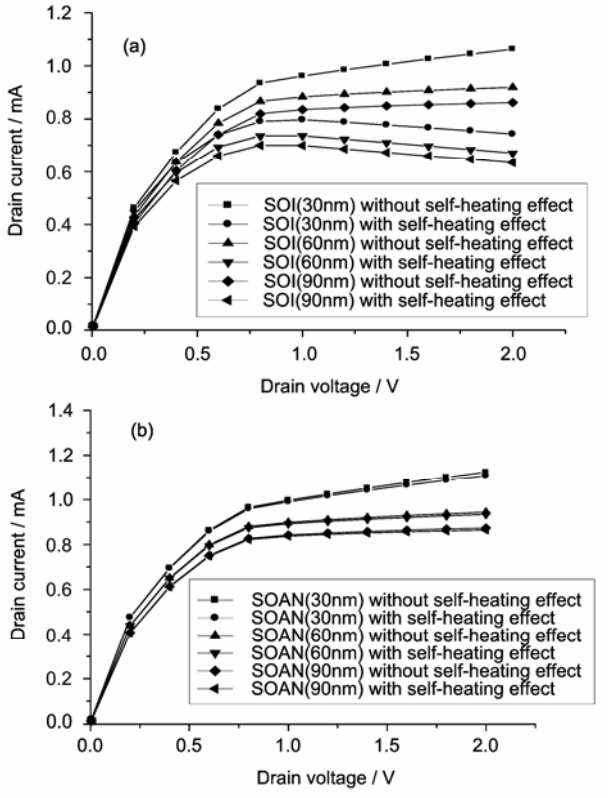


Fig. 5 Simulated output characteristics with the channel lengths of 30, 60, and 90 nm, respectively.
(a) SOI device, (b) SOAN device

4 Conclusion

To theoretically investigate the self-heating effect in small-size MOSFETs fabricated on SOAN substrate, a device simulator called MEDICI run on a Solaris workstation was used to simulate the electrical characteristics and temperature distribution by comparing with those of bulk and standard SOI MOSFETs. The SOAN devices of a small size are shown to have good leakage and output characteristics, and the channel temperature and negative differential resistance (NDR) are also reduced during high-temperature operation. This shows that SOAN can effectively mitigate the self-heating effect in MOSFETs devices and AlN is a suitable alternative to SiO_2 as a buried insulating layer in SOI, and as such SOAN devices in small-size MOSFETs could allow SOI use in high temperature conditions.

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