

An automatic phase-matching technique of CYCIAE-100 cyclotron

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Abstract The RF system of CYCIAE-100 cyclotron has two cavities, which are driven separately by two identical 100-kW RF amplifiers. Due to the power on sequence issue of the three DDSs in the LLRF systems, each time when the system is individually switched on, the phase relationship may not satisfy the requirements of beam acceleration. Instead of adding an extra reset logic to the system, a search and validation algorithm based on the decision tree has been carried out to make sure the phase of the two cavities is correct right after applying power to the cavities, taking advantage of existing hardware resources. In the first year of operation, there are more than 20 times of scheduled shutdown of the cyclotron system. For each time when the cyclotron RF system is completely shutdown and powered on again, the operator confirmed that the phase matching of the two cavities can be done automatically within 30 s. The related work, including the optimization of the phase detector and the development and validation of the algorithm, is reported in this paper.

Keywords CYCIAE-100 · Phase control · Decision tree

1 Introduction

CYCIAE-100 [1–6] is an AVF cyclotron, which provides continuously adjustable energy (75–100 MeV) and a high-intensity (200–500 μA) proton beam. The RF system

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of the CYCIAE-100 cyclotron consists of two half-wave cavities [7], two 100-kW RF amplifiers [8], and two sets of LLRF control systems [9, 10]. The two cavities are installed in the two opposite valleys and driven by two RF amplifiers [11] independently. It is different from the cavity of the CYCIAE-10 [12–16] cyclotron in that the two cavities are independent from each other. Thus, a phase close-loop control has to be used to make sure the two cavities are in phase [17].

The LLRF system of the CYCIAE-100 cyclotron is a flexible and modular system. It consists of six modules, which are 1: amplitude control board; 2: tuning control board; 3: signal control board; 4: clock reference board; 5: beam buncher RF signal control board; 6: remote control board. It can be used to control a RF system of a singlecavity cyclotron like CYCIAE-14 with modules 1, 2, 3, and 6. It also can be used to control RF systems of multicavities cyclotron like the CYCIAE-100 or the CYCIAE-800(in the future) with modules 1, 2, 3, 4, and 6. Figure 1 shows the RF system of the CYCIAE-100 cyclotron. The clock reference board provides a clock source and four phase reference RF signals for the RF system. The two signal control boards, which are comprised of a phase detector and a phase shifter (AD9954), share the clock source and two phase reference signals and drive the two cavities independently.

2 Phase control strategy

Rather than using one RF signal source and splitting it into two phase reference signals for the two LLRF systems, the LLRF system of the CYCIAE-100 cyclotron uses three DDSs to control the phase of the two cavities. One of them



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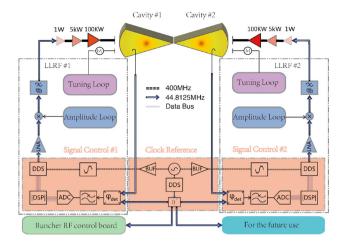
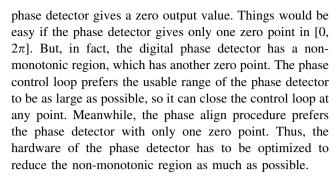


Fig. 1 (Color online) RF system of CYCIAE-100 cyclotron

is served as the traditional signal source, and the other two DDSs are unique in their LLRF system design. This structure makes it easy to modulate amplitude and phase of the RF system. The frequency of the three DDSs is fixed to 44.8125 MHz for the CYCIAE-100 cyclotron. The amplitude of which is controlled for the start-up logic, which uses a low power to protect the equipments when the system is power on. The phase of which is controlled for fast beam modulation [10]. The two cavities are psychically independent; thus, the spark and recover procedure in one cavities will not affect the other cavities. In this point of view, this independent driven method gives a better availability over the hard connected cavities solution. However, one issue needed to be addressed before this RF system be put into daily usage: The two LLRF systems don't power on at the same time, so the value of phase accumulator in the DDS may be different from each other; this will result in a phase difference between the two LLRF systems.

The phase problem may be solved by modifying the hardware system, such as 1. using a UPS as the power supply of the clock reference board and the signal control boards; or 2. adding another reset signal to the two DDSs in the signal control boards; or 3. using another power switch to make sure the two systems power on at the same time. But these methods may need hardware modification. Therefore, it is not the most cost-effective way to the designer. An alliterative way to make sure the system has a correct phase after the power is on is to use a software strategy to solve this problem. In short, the system will use the DDS as a phase shifter to search and validate the phase of the two systems. The relevant phase control circuits are marked with orange color in Fig. 1.

When the two pickup signals from two cavities are in phase with respect to the phase reference signal, the phase error of the two cavities is zero degree. In this case, the



2.1 Digital phase detector

The 2π edge-triggered phase detector is used in the phase control board because the output voltage of the 4π phase detector is not favorable for this application [18]. A limiter is used to extend the dynamic range of the phase detector. The core of the digital phase detector consists of two ECL logic D flip-flops and an exclusive NOR gate. The duty factor of the exclusive NOR gate output is proportional to the phase error. The digital output signal goes through a low-pass filter to generate a DC voltage. The circuitry is shown in Fig. 2a, and the timing diagram is shown in Fig. 2c. This phase detector belongs to Type II edge-triggered three-state phase detector, and its operating range is $[0, 2\pi]$. In theory, the output of the circuit is given by [19]:

$$V_{\text{out}} = K * V_{\text{od}} * \frac{\text{PW}_{\text{up}} - \text{PW}_{\text{down}}}{\text{PW}_{\text{f}}}, \tag{1}$$

where K is the gain factor, which can be adjusted by changing the resistor in the feedback loop of the OPAMP. $V_{\rm od}$ is the output voltage level. $PW_{\rm f}$ is the pulse width of the input RF signal.

Because of the switching times of the D flip-flop, near zero degree, the circuits involved in phase detection can be equivalent to Fig. 2b. The timing diagram of the circuits (as in Fig. 2b) is shown in Fig. 2d. Compared to the normal mode in Fig. 2c, it is obvious that the D flip-flop cannot distinguish the two clocks and treats them as one clock in $U(0,\delta)$. But the output of the D flip-flop (Q1 and Q2) is still proportional with respect to the input phase error in $U(0, \delta)$ and the duty factor is changed. Therefore, in the inside region where $\phi \in U(0, \delta)$, the transfer function of the circuit is different from Fig. 2a. When the phase goes into the boundary near δ , the circuits begin to transfer from one to the other one. In this region, not only the output amplitude will be affected but also the monotonicity may not be guaranteed (as in Fig. 4). An oscilloscope screen snap, which contains of the RFA, RFB, Q1, and Q2 signals, is shown in Fig. 3. The snap is taken when the detector is entering the region and oscillating in between the two equivalent models, which are shown in Fig. 2a, b, respectively.



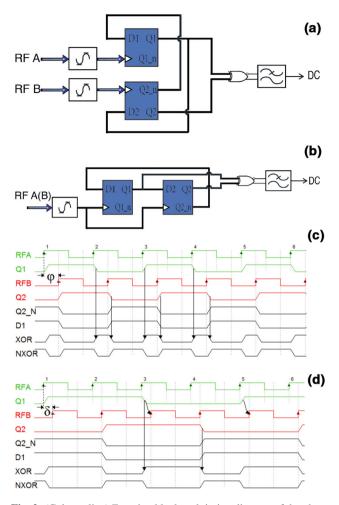


Fig. 2 (Color online) Function block and timing diagram of the phase detector

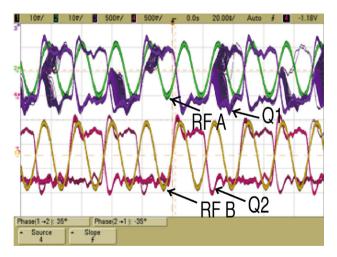


Fig. 3 (Color online) Output of the phase detector in the dead zone

To minimize the range of the non-monotonic region, the hardware has been optimized for three aspects: (a) Change the location of the pull-up resistances closer to the D flip-

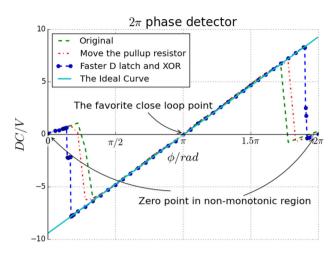


Fig. 4 (Color online) Comparison of the hardware optimization

flop; (b) change the exclusive NOR gate to a faster one; and (c) change the D flip-flop to a faster one. Figure 4 gives the results and comparisons before and after these optimizations.

After the optimization, the non-monotonic region is $\phi \in [0,\pi/6] \cup [1.9\pi,2\pi]$. There is a zero point in this region, which is an unfavorable point for phase control. According to the hardware optimization, the non-monotonic region is determined by the input signal frequency and the manufacturing technique of the D flip-flop and the NOR gate, especially the switching times (e.g., raise and fall time, the propagation delay) of the chips. The switching times of the D flip-flop would not be eliminated, so the non-monotonic region would exist all the time. The hardware optimizations can only reduce the non-monotonic region and cannot eliminate it. Using a software method to solve this problem may be easier than continuing to optimize the hardware.

2.2 Auto-phase matching

In order to reduce the influence of the non-monotonic region and generate a closed-loop control in the linear region, the LLRF control system uses an automatic phase-matching technique. The essence of this technique is an algorithm based on the decision tree. The decision tree [20] is one of the most commonly used and supervised learning classification techniques in the machine learning filed. The classifier analyzes the training data first, then constructs the classification rules (decision tree), and then classifies the dataset using the rules. The construction procedures are: 1. Collect the phase–voltage value samples of the phase detector using DDS and ADC. 2. Plot the phase–voltage curve of the phase detector and fit the phase detection function $y = f(\phi)$. Comparing the function with the ideal function $u = k * \phi + b(\phi \in [0, 2\pi], b \in \mathbb{R})$ and get the



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Table 1 Data of phase detector

Sample	Zero?	In region $(\phi_0 - \delta, \phi_0)$, linear value?	In region $(\phi_0, \phi_0 + \delta)$, linear value?	Expected zero point?
1	Yes	No	No	No
a	Yes	No	No	No
10	Yes	No	No	No
11	No	Yes	Yes	No
a	No	Yes	Yes	No
1795	Yes	Yes	Yes	Yes
a	Yes	Yes	Yes	Yes
1800	Yes	Yes	Yes	Yes
a	Yes	Yes	Yes	Yes
1805	Yes	Yes	Yes	Yes
1806	No	Yes	Yes	No
a	No	Yes	Yes	No
3600	Yes	No	No	No

^a These data are omitted

non-monotonic region of the detector $\phi \in U(0, \delta)$. 3. Disperse the dataset as Table 1 shows. Each sample consists of three features and a label. 4. The information for symbol x_i , which can take on multiple values, is defined as

$$l(x_i) = \log_2 p(x_i),\tag{2}$$

where $p(x_i)$ is the probability of choosing a class.

The Shannon entropy is the expected value of all the information of all possible values of the class. This is given by

$$H = -\sum_{i=1}^{n} p(x_i) * l(x_i),$$
(3)

where n is the number of classes.

Calculate the Shannon entropy of the dataset in step 3, compare the information gain among all the features, and return the index of the best feature. Split the data set based on the best feature and forming a branch. 5. Call the step 3 recursively until all the instances in a branch are in the same class. 6. Plot the decision tree. 7. Test the decision tree. 8. Realize the algorism on DSP and classify the phase difference voltage online.

The decision tree in step 6 is shown in Fig. 5. According to the decision tree, the procedures in step 8 are shifting the phase of the output signal step by step and reading the output voltage of the phase detector. Each step is 0.1° . This step won't stop until the zero point $(\phi_{\text{zero}}, 0)$ is found. But in fact, the ADC may be effected by noise signal, which then the absolute zero point couldn't be found easily. Instead, the algorism tries to search a set of points $(\phi_{\text{zero}}, \{x | |x| < 0.01\})$. Once it finds one point to satisfy the rules, it will switch to a closed-loop PID control, which

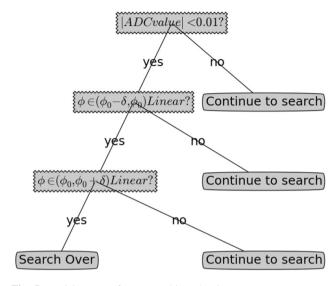


Fig. 5 Decision tree of auto-matching algorism

will take care of the small phase difference between the points $(\phi_{zero}, \{x||x| < 0.01\})$.

After finding a zero point, judge the linearity of the data in $\phi \in U(\phi_{\rm zero}, \delta)$. If the output of the detector in $\phi \in U(\phi_{\rm zero}, \delta)$ is nonlinear, then drop this zero point and keep on searching, or else the searching procedure is over and returns to the zero phase to the PID controller. Then the phase of the two cavities is correct right after applying power to the cavities, and the PID controller generates a closed-loop control of the cavity phase.

The linearity of the output in $\phi \in U(\phi_{\rm zero}, \delta)$ is determined as follows: Split the region into two regions: $\phi \in (\phi_{\rm zero} - \delta, \phi_{\rm zero}) \cup (\phi_{\rm zero}, \phi_{\rm zero} + \delta)$. Calculate the rake ration of the line determined by the two terminal points and compare it with the idle rake ration of the phase detector. If the two rake rations are almost equal, the value of the phase detector is leaner; the other results are nonlinear in this region.

The time complexity of the auto-matching algorism is calculated as follows: The time complexity of the linear judgment program is O(n) and its condition is 2/n; the time complexity of the phase shift program is O(n), so the time complexity of the algorism is O(n).

3 Experiment and discussion

To evaluate the performance of the algorism, it was tested with the RF system of the CYCIAE-100 cyclotron. The online test is under the condition of full RF power, 32 kW. To minimize the influence of the transmission cables to phase error, the oscilloscope is placed on the top of the cyclotron. Two pickup signals from the two independent cavities are chosen as the input signal for test. These two



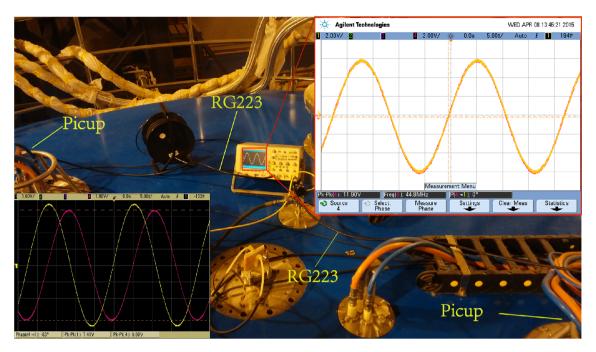


Fig. 6 (Color online) Online test of the auto-phase-matching technique

signals go through two same length (two meters) RG223 transmission cables to the Agilent DSO6054A oscilloscope. The measuring position and equipment with their transmission cables are shown in Fig. 6. This bench test is aimed to test the phase-matching time and the residual phase error of the system. After several tests, the measurement results show that the auto-phase-matching technique can align the phase of the two cavities automatically within 30 s and the residual phase error is approaching the under measurement limit of the oscilloscope, as shown in the zoomed in part of the oscilloscope in Fig. 6. The phase error is later measured by a dynamic signal analyzer, and the result shows the phase control precision is about 0.08°.

On July 4, 2014, the first 100 MeV proton beam was extracted out of the cyclotron. On July 25 of the same year, the CYCIAE-100 cyclotron maintained its beam at about 25 μ A for about 9 h [21]. In the first year of operation, there were more than 20 times of scheduled shutdown of the cyclotron system. For each time when the cyclotron RF system is completely shutdown and when the cyclotron is powered on again, the operator confirmed that the phase matching of the two cavities can be done automatically within 30 s, usually 20 s. If the operator turn off the automatic phase-matching function, the phase of the two RF system may not satisfy the requirements of beam acceleration. An oscilloscope screen snap in this situation is shown in the left bottom of Fig. 6.

Increasing the phase step in the searching state may reduce the matching time. After the DC output value of the phase detector is smaller than 0.5 V, the algorism switches

to the fine control of the phase to search the zero point. This would be a effective way to reduce the searching time in the monotonic region. This is the fastest algorism till now, and we will keep on studying the algorism or try other algorisms to make it faster in the future.

4 Conclusion

The CYCIAE-100 cyclotron takes a software technique to match the phase of the two cavities. The phase detector has been optimized for three aspects to reduce the non-monotonic region. Then, an automatic phase-matching technique based on the decision tree is used to avoid the influence of the non-monotonic region to the phase control loop and match the phase of the two cavities automatically. This technique is successfully used in the CYCIAE-100 cyclotron RF system. It matches the phase of the RF cavities in 30 s, and the phase control precision is better than 0.08°. This technique not only provides experiences for the tuning loop of the CYCIAE-230 cyclotron, but also can be used in the similar cyclotron RF system.

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