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# Design and simulation of charge sensitive preamplifier with CMOS FET implemented as feedback capacitor $C_{fp}$

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**Abstract** In this paper, to design a new preamplifier for optimum performances with charged-particle or heavy-ion detectors, the CMOS FET is implemented as a feedback capacitor $C_{fp}$, so that the entire system should be built only with MOSFET. This work is a revolution design because to realize an ASIC for a preamplifier circuit, the capacitor will also be included. We succeed after a simulation to maintain a rise time less than 3 ns, the output resistance less than 94 Ω and the linearity almost good.

**Key words** Charge sensitive preamplifier, CMOS transistor, Feedback capacitor, Simulation

**CLC numbers** TN722.7+3, TL8

## 1 Introduction

Investigating studies are on preamplifier for detecting radiations or ions in high energy physics, nuclear physics or astrophysics. To name a few, we can find that, during the realization of an ASIC (Application-Specific Integrated Circuit), certain components could not be integrated because it is difficult to minimize their sizes. For example, Ref.[1] shows two ASICs mounted on the board with test capacitors near ASIC-1, because in reason these capacitors could not be integrated as the ASIC element. To improve the functionality of any preamplifier, we will propose and show how to realize the minimized size of a capacitor using the CMOS transistor after studying the Equivalent Circuit of Enhancement-Mode MOSFET[2] and the manner to use the different pins (terminals). The MOSFET is a component used for different purposes, we saw in many studies how MOSFET was used as diode, resistor, and switch control[3-6]. In this paper, we want to extend the use of MOSFET to a capacitor, just the feedback capacitor in the preamplifier.

New preamplifiers were developed with MOSFET[1,7-9]. In our design, by simulating, the system can work and be prepared to transform to an ASIC like the other components in the design to meet the requirements.

## 2 CMOS field-effect transistors (CMOS FET)

An equivalent circuit for the MOSFET is shown in Fig.1. The input resistance of the MOSFET is exceptionally high because the gate behaves as a capacitor with very low leakage ($r_{in}$=~$10^{14}$ Ω). The output impedance is a function of $R_{ds}$ (which is related to the gate voltage) and the drain and source bulk resistances ($R_d$ and $R_s$). To turn the MOSFET "on", the gate-channel capacitance $C_{g(ch)}$, and the Miller capacitance $C_{gd}$, must be charged. In turning "on", the drain-substrate capacitance $C_{d(sub)}$ must be discharged. The resistance of the substrate determines the peak discharge current for this capacitance. The described FET is called an enhancement-type MOSFET. A depletion-type MOSFET can be made in the following manner[2].

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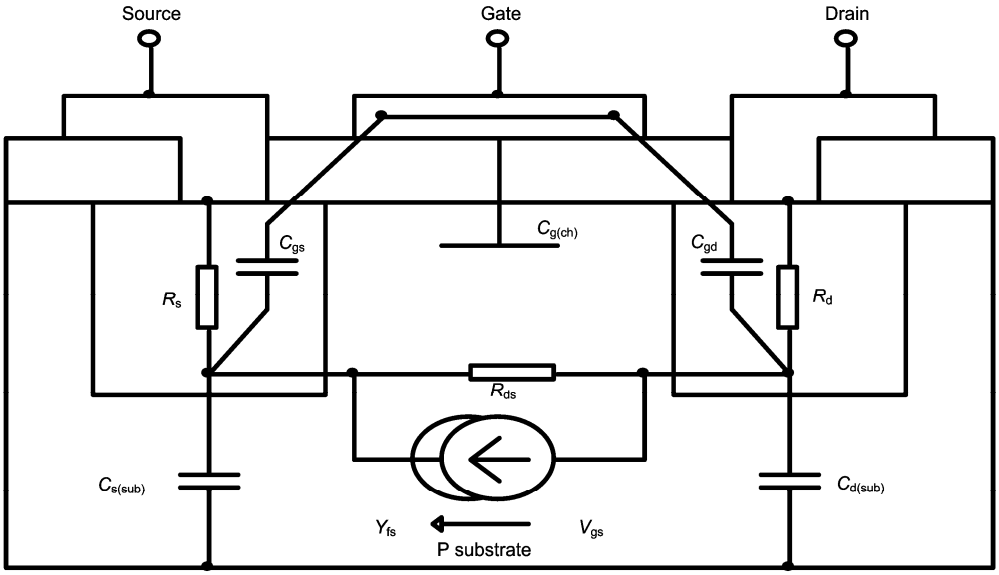


**Fig.1** Equivalent circuit of Enhancement-Mode CMOS FET. $C_{g(ch)}$, distributed gate-to-channel capacitance representing the nitride-oxide capacitance; $C_{gs}$, gate-source capacitance of the metal gate area overlapping the source; $C_{gd}$, gate-drain capacitance of the metal gate area overlapping the drain; $C_{d(sub)}$ and $C_{s(sub)}$, junction capacitances from drain to substrate and source to substrate, respectively; $Y_{fs}$, transadmittance between drain current and gate-source voltage, $R_{ds}$, the modulated channel resistance; $R_d$ and $R_s$, bulk resistances of the drain and source, respectively.

## 3 Modes of operation of CMOS capacitor

When the gate and drain terminals are connected together on a CMOS FET, the operation is similar to a *p-n* junction diode, but when the gate and the drain terminals are connected together on the CMOS FET and the source terminal is connected to the ground, the gate and the substrate (body) terminals will operate as a capacitor pins as shown in Fig.2.

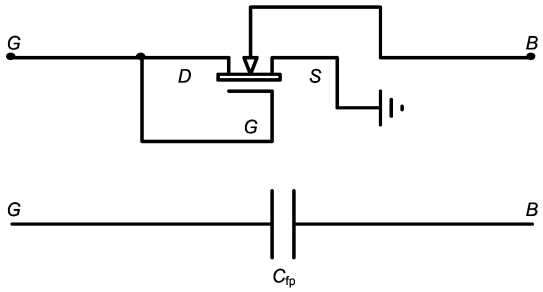


**Fig.2** CMOS FET used as a capacitor.

From these connections and the equivalent circuit above, the couples ($C_{gs}$, $C_{s(sub)}$) and ($C_{gd}$, $C_{d(sub)}$) stand to be in series respectively. The couples in series will look like two capacitor circuits in parallel when one considers certain particular values of the other parameters contained in the equivalent circuit (Fig.1). These particular values will depend on the various biasing on different terminals (pins) of CMOS FET. And the capacitors in the CMOS FET can be equivalent as a capacitor $C_{fp}$, which can be calculated according to Eq.(1):

$$C_{fp} = \frac{C_{gs} \times C_{s(sub)}}{C_{gs} + C_{s(sub)}} + \frac{C_{gd} \times C_{d(sub)}}{C_{gd} + C_{d(sub)}} \quad (1)$$

where $C_{gs}$ is the gate-source capacitance of the metal gate area overlapping the source, $C_{gd}$ is the gate-drain capacitance of the metal gate area overlapping the drain, $C_{s(sub)}$ is junction capacitance from source to substrate, and $C_{d(sub)}$ is junction capacitance from drain to substrate.

## 4 Circuit design

### 4.1 Core amplifier

The core of the preamplifier is shown in Fig.3. CMOS field effect transistors are used with the advantage of negligibly small equivalent input noise current. One can easily see the input PMOS FET M1 (PMOS has been selected over NMOS because of its lower flicker noise) and the cascode FET M2. The input is cascoded M2 in order to minimize the Miller capacitance seen at the gate of M1, which suppresses voltage swing at the drain of M1. The gate of M1 is the preamplifier input and the drain of M2 is the

preamplifier output[1]. In order to have a low resistance output, M3 is placed as a follower, and then the source of M3 becomes the preamplifier output. Output and input are connected through the feedback resistor $R_{fp}$ implemented as a CMOS FET M4 and feedback capacitor $C_{fp}$ also implemented as a CMOS FET M5.

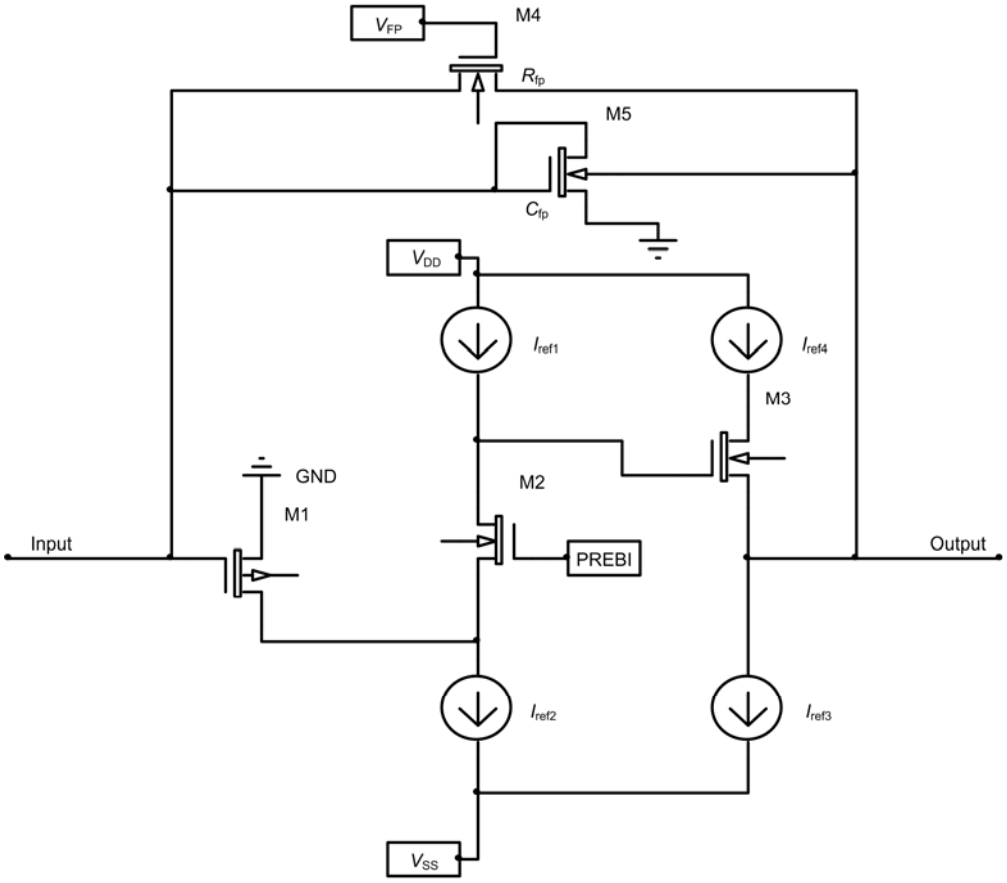


**Fig.3** Schematic drawing of the preamplifier, which is implemented as a charge sensitive amplifier.

### 4.2 Simulation results and discussion

A good preamplifier collects the full signal charge and avoids parasitic capacitances, otherwise, it would lead to cross talk, noise and bandwidth limitation. The circuit was simulated by Proteus analog simulator[10]. The pulse generator at time $t_0$ generates a short signal current at the input and the biasing at the gate M1 changes. Accordingly, currents in the drain-source of M1 and M2 change, however, their sum remains constant. The voltage at the M3 output steps down and stabilizes at $-q/C_{fp}$. The pulse signals flow through the feedback circuit. The bias voltage VFP is activated, FET M4 operated as the feedback resistance $R_{fp}$ conducts the dc-current, and the feedback capacitance made also by a FET M5 conducts the pulse signal. The signal charge $q=C_{fp}V_{in}$ is stored in $C_{fp}$ which discharges slowly *via* $R_{fp}$ on time constant $\tau= R_{fp}\cdot C_{fp}$. Fig.4 shows the measurement of the simulation.

Now, we replace the CMOS transistor M5 by the real capacitor in the Fig.3 accordingly to the same values shown in Fig.4. The curves obtained in Fig.5 are with those represented in Fig.4.

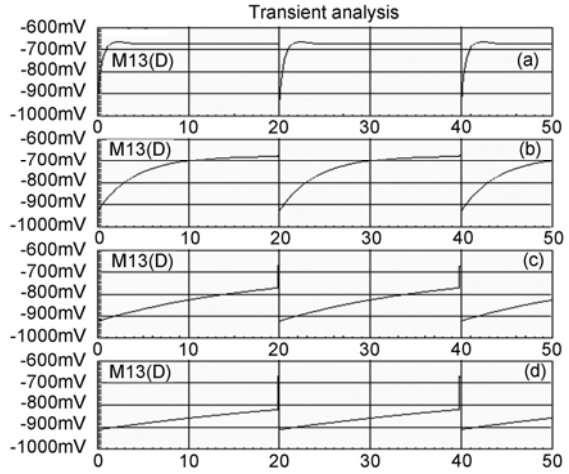


**Fig.4** CMOS transistor implemented as capacitor M13(D). Output signal at $C_{fp}$=0.1 pF, $R_{fp}$=5 M (a), output signal at $C_{fp}$=1 pF, $R_{fp}$=5M (b), output signal at $C_{fp}$=5 pF, $R_{fp}$=5 M (c), output signal at $C_{fp}$=10 pF, $R_{fp}$=5 M (d).

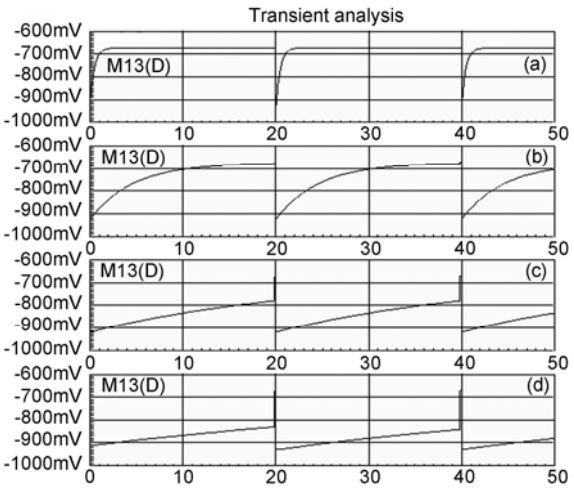


**Fig.5** Real capacitor M13(D). Output signal at $C_{fp}$=0.1 pF, $R_{fp}$=5M (a), output signal at $C_{fp}$=1 pF $R_{fp}$=5 M (b), output signal at $C_{fp}$=5 pF, $R_{fp}$=5 M (c), output signal at $C_{fp}$=10 pF $R_{fp}$=5 M (d).

One can just find a slight difference especially at curve $C_{fp}$ = 0.1 pF where presenting the undershoot size of the signal due to the other parameters which also characterize the equivalent circuit of CMOS transistor, or because all other active components, field effect transistors generate a certain amount of noise. The noise figure for field-effect transistors is normally specified on the data sheet as "spot noise", referring to the noise at a particular frequency. The noise figure will vary with frequency and also with the resistance at the input of the device[2].

### 4.3 Preamplifier rise time

The rise time of the preamplifier is measured with analog software electronic[10]. Fig.6 shows that the rise time is less than 3 ns and it doesn't really change when $C_{fp}$ increases with $R_{fp}$ remaining constant. Also, the magnitude of the output signal reduces slightly when the capacitor $C_{fp}$ increases. Therefore one can say that the rise time decreases slightly when $C_{fp}$ increases considerably.

## 5 Conclusions

After designing the new circuit with CMOS FET implemented as capacitor to replace the feedback capacitor in the preamplifier circuit, computer simulation was carried out by PSPICE simulator using BSIMV3.3 parameters of the Proteus and the nearly same results were obtained both when the simple capacitor is used as feedback capacitor and when

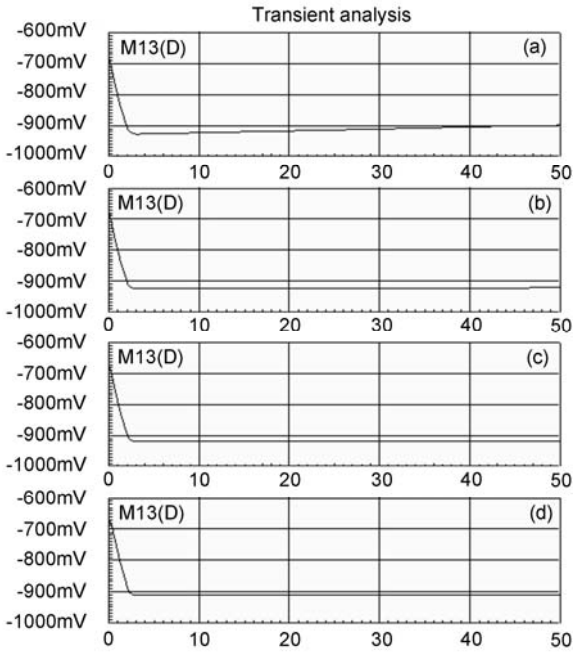


**Fig.6** Output signal M13(D) at Cfp=0.1 pF, Rfp=5 M (a), Cfp=1 pF, Rfp=5 M (b), Cfp=5 pF, Rfp=5 M (c) and Cfp=10 pF Rfp=5 M (d).

CMOS FET is implemented as feedback capacitor. The advantage of this design is to be capable of integrating feedback capacitor like any other components that can be integrated to construct the preamplifier[1]. The rise time is still maintain to less than 3 ns with CMOS implemented as a feedback capacitor.

For further investigations, the future direction of the work is to implement the performance of the design so that it should be completed as an ASIC design.

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