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A novel testing approach for SSRF digital power supply controllers

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Abstract Digital power supply controller is one of the key parts of SSRF high resolution high stability magnet power supply system. It is very essential to keep any degradation of these excellent properties by any stages as small as possible via careful testing when the controller is developed. In this study, a novel testing approach was presented, with which a novel closed control loop without actual power converter was constructed, and the new developed SSRF *Digital Controller* can work well in it.

Key words SSRF, Digital power supply controller, PWM, Low pass filter

CLC numbers TL503.5, TM571.6$^+$5, TM930.12$^+$8

1 Introduction

Digitally controlled switching power supplies are increasingly seen in industries, using controllers of high performance DSP (Digital Signal Processor) controllers at decreasing cost.

At Shanghai Synchrotron Radiation Facility (SSRF), hundreds of high resolution and high stability magnet power supplies are needed for its electron beam control[1]. A TMS320F2812 based digital power supply controller, referred here as *Digital Controller*, was developed to satisfy performance requirement of SSRF, and to trace the trends of applications of digital power supplies in accelerator technology.

In this paper, we report a new approach of testing the *Digital Controller* without the actual power converter circuits, which is practical and much safer. Structure of the digitally controlled switching power supply is analyzed. Descriptions are given to the *PSBoard*, a novel close-loop construction designed to substitute the real power converter circuits. Frequency characteristics of the whole system were tested based on the *PS Board*.

2 System structure of the power supply and the *Digital Controller*[2-4]

Fig.1 shows a simplified block diagram of the digitally controlled power supply system. It consists of a power converter, an ADC/DAC card, a digital controller card and the magnet, which are short for the *Converter*, the *ADC/DAC,* the *Controller* and the *Magnet,* respectively, in the text below. And we refer the *ADC/DAC* and the *Controller* as the *Digital Controller*. The DC link voltage, the load current and the load voltage are sampled and digitalized by the *ADC/DAC*. The digitized signals are sent to the *Controller*. The DSP based controller is responsible for the duty ratio computation with typical PID (Proportion-Integral-Derivative) control concept. It generates PWM (Pulse Width Modulation) waveforms, which are sent to a driver to drive the IGBTs (Isolated Gate Bipolar Transistors) with switching frequencies from 10 kHz to 100 kHz. In addition to communication with the *ADC/DAC*, the *Controller* communicates to the *Local Control*, *Global Control* and *Digital I/Os*, monitoring failure signals of the power supply system.

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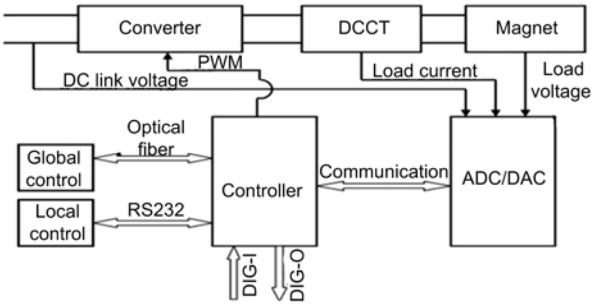


Fig.1 Structure of the SSRF power supply.

3 *PS Board* design

For magnet power supply systems, the *Converter* and the *Digital Controller* have significant impacts on performance of the power supplies. If the *Converter* can be determined, the *Digital Controller* will be vital to performance of the whole systems. However, as the *Digital Controller* is interfaced to the *Converter* in the test, one can hardly decide on whether a problem is due to the *converter* or the *controller*. In addition, IGBTs are critical electronic parts that shall be dealt with carefully, and would be damaged if the controller had a fault when it is tested with the real power converters. Therefore, one has to find a way to test a newly developed *Digital Controller*.

The *Digital Controller* has six high resolution PWM outputs, which are variable duty cycle square-waves of 5-V amplitude. Each of the signals can be decomposed into a D.C. component plus a new square-wave of identical duty-cycle but with time-average amplitude of zero, as shown in Fig.2a. When the PWM output passes an analog low-pass filter, most of the high frequency components can be removed, ideally leaving only the D.C. component (Fig.2b)[5]. This is the basis to design the *PSBoard*.

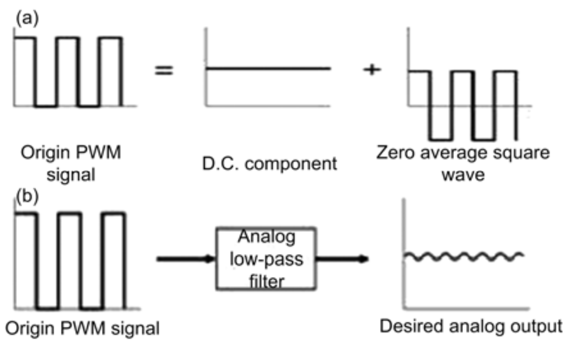


Fig.2 Decomposition (a) and analog filtering (b) of a PWM signal.

3.1 Active second order low pass filter design

Performance of this approach relates directly to ability of the low-pass filter to remove the high-frequency components of the PWM signal. To have increased attenuations without degrading the signals one is interested in, a usual way is to cascade several RC filters together. Unfortunately, as the impedance of one RC section affects the next, the "knee" or transition between the pass and stop bands may not become very sharp. Besides, the converter should copy the characteristic of a power supply as much as possible, hence at least a second order conjugate pole in most of power supplies with magnet load. Here, an active second order low pass filter is a good choice (Fig.3).

The transfer function of the circuit in Fig.3 is:

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)}=\frac{1+\dfrac{R_4}{R_3}}{1+(R_2C_2+R_1C_1+R_1C_2-(1+\dfrac{R_4}{R_3})R_1C_1)s+R_1R_2C_1C_2s^2} \quad (1)$$

It looks much different from the standard form, and the following substitutions can be made.

$$K=1+\frac{R_4}{R_3},\omega_n=\frac{1}{\sqrt{R_1R_2C_1C_2}},$$
$$Q=\frac{\sqrt{R_1R_2C_1C_2}}{R_2C_2+R_1C_1+R_1C_2-KR_1C_1},S=\frac{s}{\omega_n} \quad (2)$$

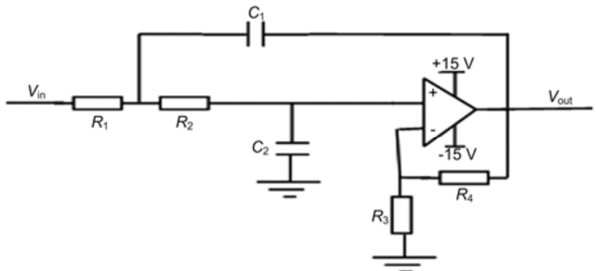


Fig.3 Active second-order low pass filter.

And then Eq.(1) can be simplified to Eq.(3):

$$\frac{V_{\text{out}}(S)}{V_{\text{in}}(S)}=\frac{K}{1+\dfrac{1}{Q\omega_n}S+\dfrac{1}{\omega_n^2}S^2} \quad (3)$$

where K is the gain of this loop, ω_n is the characteristic angular frequency, and Q is the quality factor.

To make sure the bandwidth we are interested in is flat enough, we choose Q<1, for example the second order Butterworth filter has a Q value of 0.707. Set the corner frequency at about 1 kHz for filtering the PWM. Comparing Eq.(3) with the general transfer function of a low pass filter, one has

$$\frac{V_{\text{out}}(S)}{V_{\text{in}}(S)}=\frac{K}{\prod_i(1+a_iS+b_iS^2)} \tag{4}$$

The coefficients can be obtained in the Filter Coefficients Table[6], i=1, a_i = 1.4142, b_i = 1.000, Q_i = 0.707.

Given C_1=C_2=0.02 μF and solving R_1–R_4 from Eq.(2), the real values are R_1=5.6 kΩ, R_2=11 kΩ, and R_3= R_4=33 kΩ.

The amplifier is a dual power TL084CN (STMicroelectronocs), which is a quad operational amplifier with high SR and high GBP up to 4 MHz.

3.2 Novel close-loop control system construction

Fig.4 shows a block diagram of the novel constructed close-loop control system without the real *Converter,* which is now substituted by *PSBoard*. Note that the input voltage range of the ADC on the *ADC/DAC* is 0~5 V. Therefore, the output D.C from the active low-pass filter must be attenuated with precision resistor division.

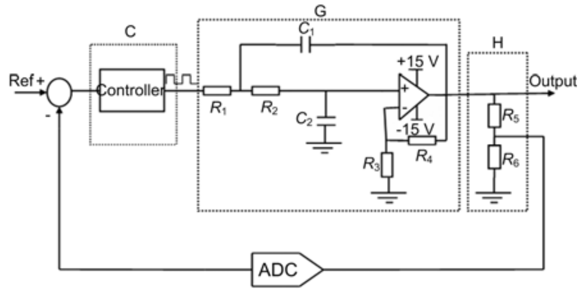


Fig.4 Block diagram of the novel constructed close-loop control.

4 Testing results

In Fig.4, the dashed boxes of C, G and H compose a close-loop system. As mentioned in Section 2, typical PID control scheme was used in SSRF digital power supply controllers. The *s*-domain transfer function of the *Controller* is:

$$C(s)=\frac{K_{\text{p}}(s+K_{\text{i}})}{s(s+K_{\text{lp}})} \tag{5}$$

where K_{p} is the proportional coefficient, K_{i} is the integral coefficient, and K_{lp} is the cutoff frequency of the digital low pass filter before PID computation. The three parameters can be adjusted to match different Gs. For the referred active second-order low pass filter G, K_{p} =3, K_{i} =200, and K_{lp}=5000. The continuous-time close-loop Bode for this system is plotted in Fig.5 using the MATLAB control design toolbox of SISOtool. Add a sine wave on the Output with a function generator HP 33120A and adjust its frequency from D.C. to higher frequency, the close-loop frequency characteristics of the whole system can be tested with a Tektronics TDS 3014 oscilloscope. The results are shown in Figs.6 and 7. Comparing Fig.5 with Figs.6 and 7, the real *Controller*'s bandwidth can be very close to that of G, and in the passband of the system, the phase shift and the gain of the Bode plot are consistent very well with the testing results.

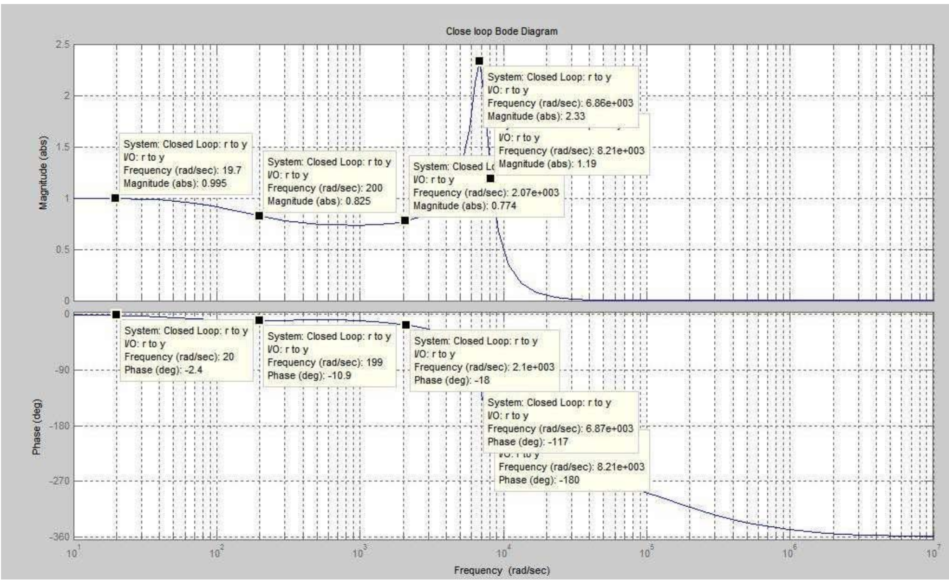
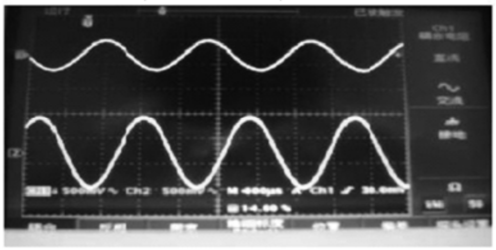
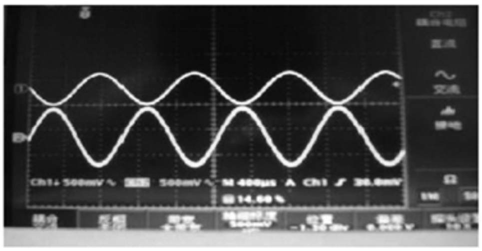


Fig.5 Close-loop Bode diagram.

$K_p = 3$, $K_i = 200$, $K_{ip} = 5000$



(a) $f = 910$ Hz, Gain = 2.33, Phase shift = 141°



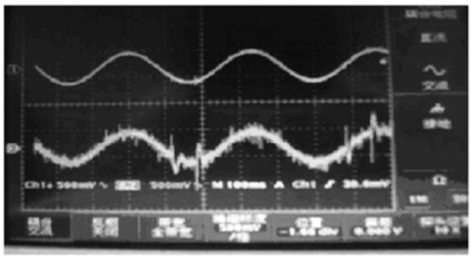
(b) $f = 980$ Hz, Gain = 1.8, Phase shift = 180°

Fig.6 Close loop testing results on critical state.

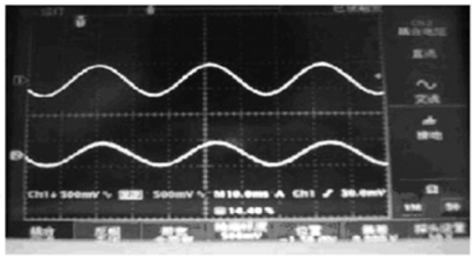
5 Conclusion

Based on this novel constructed closed control loop, some parameters of the *Digital Controller* we interested in can be tested, such as close-loop frequency response, bandwidth, time delay between ADC and DSP, PWM outputs and digital I/O driving abilities. Limited to space, only a set of the testing results of close-loop frequency response of the referred system is listed in this paper. The corresponding testing methods for each parameter and different topologies of power supply will be investigated. Therefore, this work is important to the development of SSRF digital power supply controller, and to manufacturers of the power supplies.

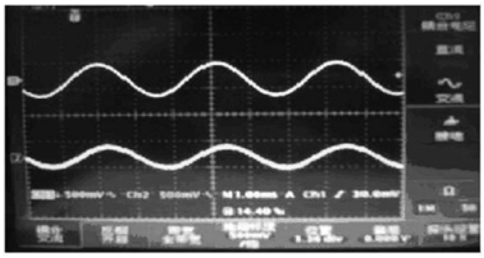
$K_p = 3$, $K_i = 200$, $K_{ip} = 5000$



(a) $f = 3$ Hz, Gain = 600 mV / 600 mV = 1, Phase shift = 0°



(b) $f = 32$ Hz, Gain=480 mV/600 mV=0.8, Phase shift=11°



(c) $f = 320$ Hz, Gain=450 mV/600 mV=0.75, Phase shift=22.5°

Fig.7 Close loop testing results upon different frequencies.

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