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Phase control system for SSRF linac

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Abstract The design of phase control system in Shanghai Synchrotron Radiation Facility (SSRF) linac is presented in this paper. And digital phase detecting algorithm, the key for phase control system, is fully described. The testing results for phase control system in 100MeV linac are discussed in detail.

Key words Digital phase detector, Phase control system, Linac, SSRF

CLC number TL506

1 Introduction

As a third generation light source, SSRF consists of a 3.5 GeV storage ring, a 3.5 GeV booster and a 150 MeV linac. The linac, as an injector for the booster, includes a thermionic cathode electron gun, a 500 MHz sub-harmonic buncher, a 2998 MHz buncher and four accelerating sections. The accelerating section is of constant gradient accelerating structure, working at 2998 MHz, six times of the RF frequency of the storage ring.

As shown in Fig.1, Klystron A is used for the 2998 MHz buncher and accelerating sections of A1 and A2, while Klystron B, for accelerating sections of A3 and A4. The klystrons are driven separately by a solid-state power amplifier.

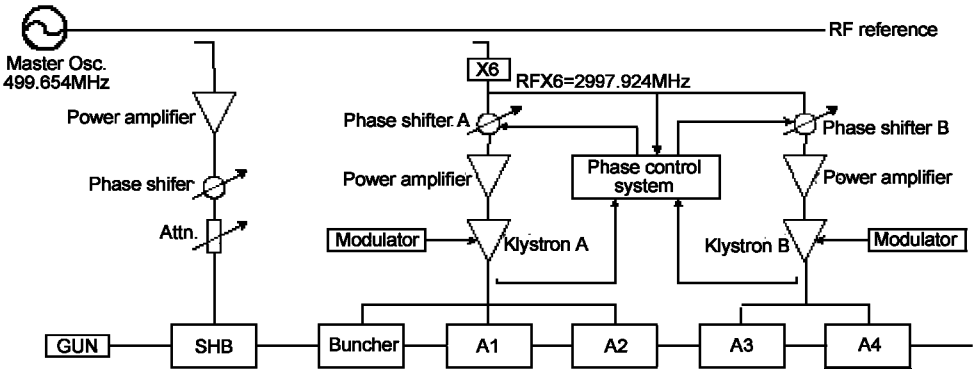

Fig.1 Layout of the 150 MeV linac.

To reduce energy spread of the electrons from the linac, a phase control system is needed to control the pulse-by-pulse phase shift of the klystron forward signal to within ±1°.[1] The phase shift is acquired by comparing the phase of klystron forward signal with the phase of frequency multiplier output signal (RF reference signal in phase control system). The voltage variable phase shifter is placed between frequency multiplier and power amplifier, and is adjusted on the basis of phase shift data. To satisfy the physics requirement, the control loop for phase control system, which contains phase shifting acquisition, control algorithm calculation and phase shifter execution, must be finished within linac injection interval (500 ms).

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2 Phase detecting algorithm

Performance of phase shift acquisition determines whether the phase control system can meet the requirement of <±1° shift. Digital phase detecting system, for which phase detecting algorithm is the key, is advantageous in terms of noise resistance, linear range and adjustment convenience [2], in comparison to conventional analog phase detecting system,

ADC (Analog Digital Converter) input signal can be assumed by

$$x(t) = A\cos(2\pi f_0 t + \varphi) + B \tag{1}$$

where f_0, φ, A and B are the frequency, initial phase, amplitude and offset, respectively. Sampling frequency is set to four times of input signal frequency. ADC module samples four points continued in one period, which can be given by

$$\begin{cases} x(4m) = A\cos(\theta_r + \varphi) + B \\ x(4m+1) = -A\sin(\theta_r + \varphi) + B \\ x(4m+2) = -A\cos(\theta_r + \varphi) + B \\ x(4m+3) = A\sin(\theta_r + \varphi) + B \end{cases} \tag{2}$$

where θ_r is the random phase of the ADC's random sampling. Then digital I/Q can be obtained by

$$\begin{cases} I(n) = [x(4m) - x(4m+2)]/2 = A\cos(\theta_r + \varphi) \\ Q(n) = [x(4m+3) - x(4m+1)]/2 = A\sin(\theta_r + \varphi) \end{cases} \tag{3}$$

But the objective of phase detecting algorithm is to attain the phase difference between two channels, so the working mode for ADC two channels is set to simultaneous sampling mode. Based on Eq. (3), digital I/Q of two channels can be written as

$$\begin{cases} I_1 = A_1\cos(\varphi_1 + \theta_r) \\ Q_1 = A_1\sin(\varphi_1 + \theta_r) \\ I_2 = A_2\cos(\varphi_2 + \theta_r) \\ Q_2 = A_2\sin(\varphi_2 + \theta_r) \end{cases} \tag{4}$$

where φ_1 and φ_2 are the initial phase of two channels, respectively.

Then we have ΔI and ΔQ with Eq.(5)

$$\begin{aligned} \Delta I &= I_1 * I_2 + Q_1 * Q_2 = A_1 A_2\cos(\phi_1 - \phi_2) \\ \Delta Q &= Q_1 * I_2 - I_1 * Q_2 = A_1 A_2\sin(\phi_1 - \phi_2) \end{aligned} \tag{5}$$

where A_1 and A_2 are the amplitude of two channels, respectively.

A desired phase difference can be attained from ΔI and ΔQ. Therefore, we can make a block diagram of the phase detecting algorithm based on Eqs. (3~5), as shown in Fig.2.

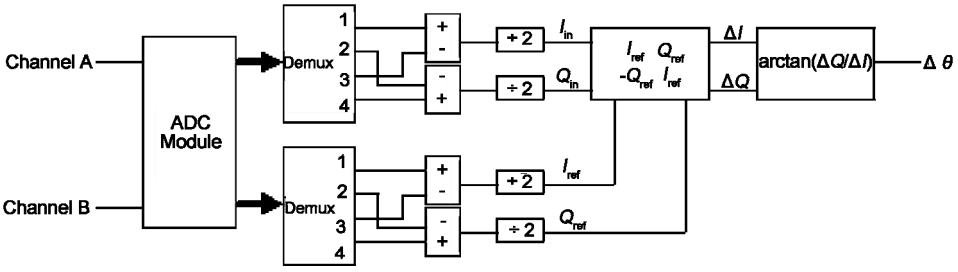

Fig.2 Block diagram of phase detecting algorithm.

In practice, ADC module's performance may introduce phase detecting error, or may involve phase detecting resolution. So it is necessary to analyze the relationship between ADC module's performance and phase detecting algorithm performance.

Based on stochastic process theory, the main factors of ADC performance, which involve phase detecting error or resolution, can be deduced. The formulas are listed below:

1) Cross talk between two channels

Cross talk could introduce measurement error, which is given by

$$\theta_{err} = |\sin\Delta\theta| \times (\frac{B}{A} + \frac{A}{B}) \times \alpha \tag{6}$$

where $\Delta\theta$ is the phase difference between two channels, α is the coefficient of cross talk, and A and B are the amplitude of two channels, respectively. So, the error can be eliminated by adjusting the phase difference.

2) Sampling clock jitter of the two channels

Sampling clock jitter of the two channels affects measurement resolution by

$$\mathrm{rms}[\theta_{noise}] = \frac{\sqrt{3}}{2}\sigma_p \tag{7}$$

where σ_p is the RMS (root mean square) value of phase noise caused by the sampling clock jitter. For an NI PXI5122 ADC module having sampling clock jitter of 1 ps, for example, σ_p is 0.036° under 100 MHz sampling frequency.

3) Amplitude noise of the two channels

Amplitude noise of the two channels worsens measurement resolution by

$$\mathrm{rms}[\theta_{\mathrm{noise}}]=\frac{\sqrt{2}}{2}\times\sqrt{\frac{\sigma_A^2}{A^2}+\frac{\sigma_B^2}{B^2}} \tag{8}$$

where σ_A and σ_B are the RMS value caused by amplitude noise of the two channels. So, the resolution can be improved by increasing input signal amplitude within ADC input range.

4) Difference between sampling frequency and input signal frequency

Difference between sampling and input signal frequencies does not introduce measurement error, but measurement resolution can be affected by

$$\mathrm{rms}[\theta_{\mathrm{noise}}]=\sqrt{2}\left|\sin\Delta\theta\right|\times 2\pi\left(\frac{4f_0}{f_s}-1\right) \tag{9}$$

where f_0 is input signal frequency and f_s is sampling frequency.

3 Design of the phase control system

The phase control system was designed under the following philosophy:

—Use ADC and DAC modules that are commercially available and built in PXI platform.

—Use passive coaxial RF components to down-convert RF signal to IF signal.

—Apply digital phase detecting algorithm to attain phase difference between RF reference IF signal and klystron forward IF signal.

The detailed layout of phase control system is shown in Fig.3.

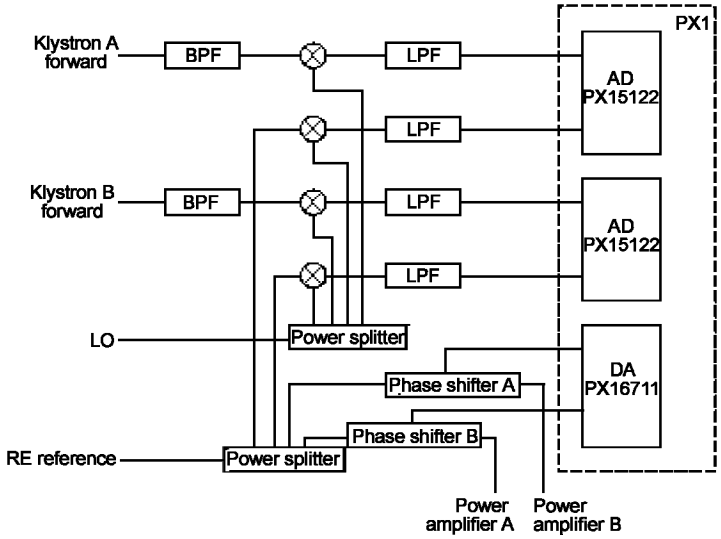

Fig.3 Layout of phase control system.

The ADC is NI PXI5122, a 2-channel 100 MHz 14-bit high-speed digitizer that works in simultaneous sampling mode. The DAC is NI PXI6711, a 4-channel 1 MHz 12-bit DA module, which generates DC voltage to control voltage variable phase shifter.[3,4]

The phase shifter can be adjusted within 360° under 0~10V, and the NI PXI6711 output range is set to 0~10V.

Working mode of the NI PXI5122 is set to external trigger, internal 100 MHz sampling frequency, ±0.1V input range, and 2-channel simultaneous sampling. So, the frequency of IF signal must be 25 MHz in order to apply digital phase detecting algorithm. External trigger is synchronized with the linac injection trigger.

The function of RF front-end is to down-convert RF signal (2998 MHz) to IF signal (25 MHz). To improve phase detecting resolution in Eq. (9), LO (local oscillator) frequency is adjusted to set IF signal frequency close to the one fourth of NI PXI5122 sampling frequency.

The NI PXI5122 and NI PXI6711 are controlled by the PXI controller, in which phase control software is run under Windows XP operating system. The software control sequences are:

1) Trigger NI PXI5122 by external trigger,

2) Continued sample four points in each channel of NI PXI5122,

3) Calculate the phase difference by applying phase detecting algorithm,

4) Compare measured phase difference with set point, and calculate their difference,

5) Input this difference into PID control algorithm to calculate NI PXI6711 setting value,

6) Set desired value in NI PXI6711,

7) Wait for next external trigger.

In Windows XP, the sequences in phase control software could finish within 500 ms, which satisfies the physics requirement for time consumption of phase control loop.

The phase difference between klystron forward and RF reference is acquired within 40 ns (4 points in 100 MHz sampling frequency). This is more practical than the averaged phase difference within the whole pulse of klystron forward signal, in that it is meaningful to measure the klystron phase shifting in the interval (about 1ns) of beam drifting in accelerating section. By adjusting external trigger delay, the interval of beam drifting in an accelerating section can be within the interval of NI PXI5122 acquisition, hence the improvement of pulse-by-pulse phase control performance of the linac.

EPICS IOC is applied in phase control software, so the phase control system is easy to be integrated into the SSRF control system.

4 Test on a 100MeV linac

The phase control system was tested on a 100 MeV linac at SINAP. Background noise of phase measurement in the 100 MeV linac was checked first (Fig.4). And as shown in Fig.5, the phase measurement resolution (RMS) of background noise is about 0.05°.

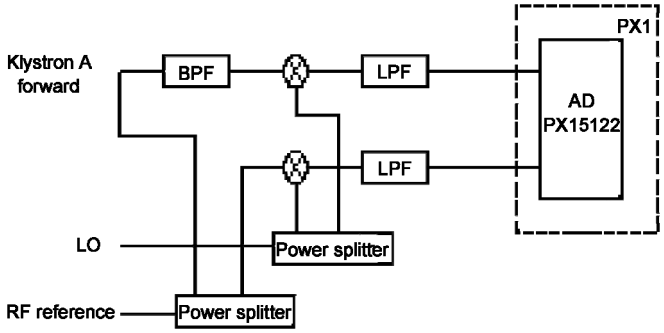

Fig.4 Testing diagram for background noise.

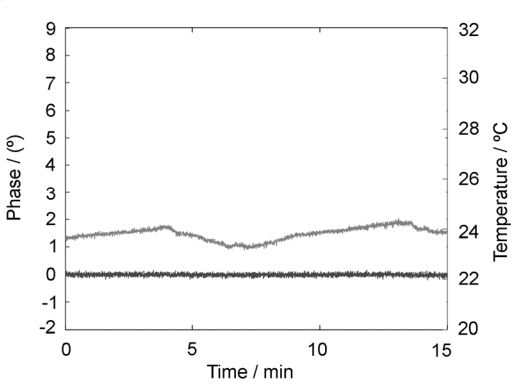

Fig.5 Background noise of phase measurement.

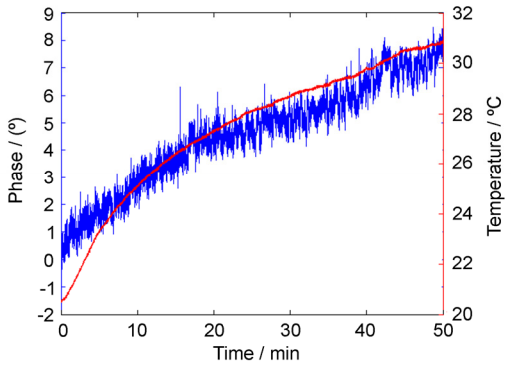

Fig.6 Phase shifting of klystron forward in open loop.

Then, by changing surrounding temperature of phase control system on the linac, phase shifting of klystron forward could be observed in the condition of open loop for the phase control system. The testing results are shown in Fig.6 with temperature shifting curve.

Finally, performance of the phase control system was tested in the condition of close loop by changing surrounding temperature. As shown in Fig.7, the pulse-by-pulse phase shift (RMS) of klystron forward could be controlled to about 0.3°.

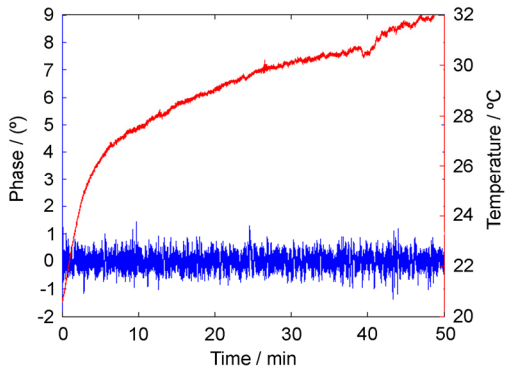

Fig.7 Phase shifting of klystron forward in close loop.

In conclusion, the phase control system can well control pulse-by-pulse phase shift of the klystron forward and it is expected to satisfy the physics requirement for SSRF linac operation.

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