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A new TOF system for target recoil-ion momentum spectroscopy at IMP

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Abstract A high resolution time measurement system with high data transfer rate was designed for the COLTRIMS (Cold Target Recoil-Ion Momentum Spectroscopy) system in Institute of Modern Physics, Chinese Academy of Sciences. It is used to measure the Time of Flight (TOF) with a high resolution for all 20 channels. Based on the PCI Extensions for Instrumentation (PXI) standard, the readout electronics system consists of one Clock-Trigger fan-out module and four TOF modules. Test results show that the system meets the demands of COLTRIMS, with a time resolution of better than 25 ps and a data transfer rate over 20 MB/s.

Key words Time of Flight, PXI, Burst transfer

1 Introduction

In atomic physics, fully differential cross sections (FDCS) are a key to mechanisms of correlated dynamic reaction of charged particles. With the development of experimental techniques, large area position-sensitive detectors [1], and time of flight (TOF) measurements, are exploited to coincidently detect the reaction products of an atomic collision, making it possible to perform an FDCS measurement[2]. The Cold Target Recoil-Ion Momentum Spectroscopy (COLTRIMS) in Institute of Modern Physics (IMP), Chinese Academy of Sciences, allows detection of three-dimensional momentum vector of the recoiling ions from ion-, electron- or photon-atom collisions with 4π solid angle and high resolution[3].

The architecture of a COLTRIMS system at IMP is shown in Fig.1[4]. The ion beam from an all permanent magnetic ECR ion source collides with a target, and four position sensitive detectors (PSDs) are used to generate signals carrying position and time information of the fragments, including the projectile ions, recoil ions, and electrons. The signals are discriminated by corresponding constant fraction discriminator (CFD) systems, and transmitted to the TOF readout modules and the data acquisition system.

In the 1990s, a TOF system named CAMAC-TDC was built by IMP, and a 1-ns time resolution was achieved by electronics based on CAMAC bus. Our new design for the COLTRIMs system aims to improve the time resolution to better than 25 ps. Considering an average trigger rate of 100 kHz, the system data transfer rate to the remote personal computer (PC) is around 20 MB/s.

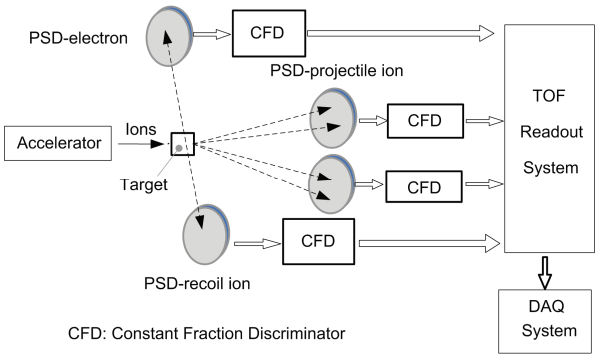

Fig.1 The architecture of a COLTRIMS system at IMP.

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2 The time of flight readout system

A PSD in the COLTRIMS system provides 5 channels, for two pairs of signals from two-dimension delay lines[5] and one signal for readout of Micro Channel Plate (MCP) of the PSD. The readout system measures the TOF and positions of the collision fragments. The one-dimension position is determined by the arrival time difference of pulses propagating toward the ends of a delay line, and the two-dimension position is calculated by its delay lines. Therefore, the key is high precision time measurement, i.e the time resolution of better than 25 ps. The segments produced by hit of ion on the target have different final speeds, hence a TOF dynamic range as wide as 10 μs.

2.1 System architecture

To achieve a data transfer rate of around 20 MB/s, the readout system is designed using the PCI Extensions for Instrumentation (PXI) 3U standard. As shown in Fig.2, it consists of four TOF readout modules and a Clock-Trigger fan-out module in the PXI chassis of NI PXI-1033. The Clock-Trigger module generates four synchronous clocks and fans the trigger signal from the CFD system out to the four TOF modules with a skew of less than 1 ns [6]. When matching the same trigger, time measurement information of different TOF modules is packed with the same event mark to rebuild the event.

The signal-arriving time is digitized and processed in the TOF modules. For the data transfer, a PCI-to-MXI Express Bridge is integrated in the PXI chassis. This bridge receives the measurement results from the TOF modules through the PCI bus, and transfers them to the remote PC through the Multisystem Extension Interface (MXI) cable. On the remote PC, Graphic User Interface (GUI) software, which is responsible for data analysis and display, is designed to acquire data from the PXI chassis.

2.2 TOF readout module

A high performance time-to-digital converter chip (HPTDC) is used in the TOF readout modules for precise time measurement in a resolution of 25 ps. The HPTDC chip was designed by the microelectronics group at CERN using a commercial CMOS 0.25 μm technology, and has been successfully applied in the readout electronics for TOF detectors of several particle experiments, such as ALICE[7], STAR[8], and BESIII[9]. A block diagram of the TOF module is shown in Fig.3.

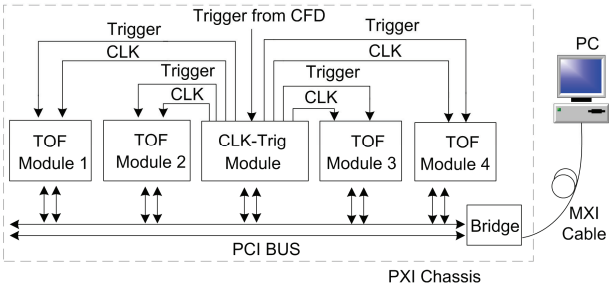

Fig.2 The TOF readout system.

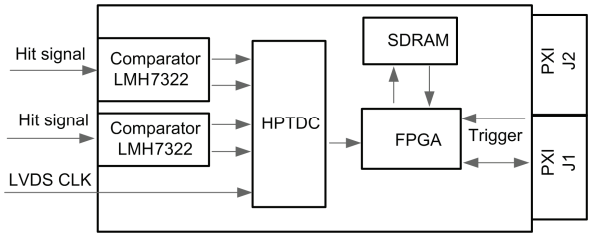

Fig.3 Structure of TOF module.

The NIM signals up to 8 channels are buffered and converted to LVDS (Low Voltage Differential Signaling) signals (a leading or trailing edge is called 'hit'), and transmitted to the HPTDC for time measurement. Triggers are distributed to every TOF module by the star trigger buses. After measuring the hit signals by the HPTDC, the time data corresponding to the trigger signals are transferred from the HPTDC to the FPGA, where the data processing, acquisition, and the configuration, are completed. A PCI core is integrated in the FPGA to transfer the data to the PC for further analysis and storage.

According to datasheet of the HPTDC, the ≤25-ps time resolution is good enough for the requirement. Its recommended measurement range of 25 μs is well beyond the required 10 μs. Moreover, its pair pulse resolution of 10 ns is sufficient to distinguish two segments coming into one PSD during one hit.

2.2.1 Time measurement

The HPTDC has also a time stamp TDC[10] to record several stop time points correlated to one single start.

Unlike a traditional start/stop TDC, this enables measuring several segments from one hit in high energy experiments[11].

An external 40 MHz clock of HPTDC is generated, and its signal is multiplied by an on-chip Phase Locked Loop (PLL) up to 320 MHz, to drive a counter to provide a coarse time value since the start of HPTDC. A 32-element Delay Locked Loop (DLL) performs time interpolation down to 98 ps for each bin (LSB). Further, an interpolation within a DLL cell is obtained by sampling four times the DLL signals, which is controlled by an on-chip R-C delay line, achieving the finest time resolution of 25 ps.

Also, the HPTDC is remarkable for its flexibility. It has four modes of resolution: low (800 ps), medium (200 ps), high (100 ps) and very high (25 ps). In the first three modes, it provides a total of 32 time measurement channels. The last mode has just 8 channels, but Integral Non-Linearity (*INL*) calibration is implemented, for achieving the ≤25-ps resolution.

Data configuration and readout of the HPTDC is controlled by the FPGA. On powering the system, a special file for the configuration is written to the FPGA. For data readout, the HPTDC generates a 4-byte data packet, including header, trailer and time information of a hit signal, and stores it in a 256-word FIFO, waiting to be matched with the triggers. The final results are transferred to the FPGA and further the remote PC.

To assure the high time measurement performance, closer attention to the Signal Integrity (SI) is paid in the hardware design. The NIM-to-LVDS signal convertion is in fast slew rate, with good anti-interference ability. The impedance is carefully matched to decrease the reflection in signal transmission, besides the PCB design, such as providing large plates for grounding and power supplies, and reducing the crosstalk with careful PCB routing.

2.2.2 Data processing

A single FPGA chip (EP1C12F324) is employed to process digital signal and transfer data. The main logic consists of the Read Control Logic, INL Calibration Logic, SDRAM Control Logic and PCI Interface Logic (Fig.4). The data generated with the HPTDC is acquired by the Read Control Logic, compensated by *INL*, and buffered in a 16 MB SDRAM. Finally, the results are transferred to the remote PC through the PXI interface.

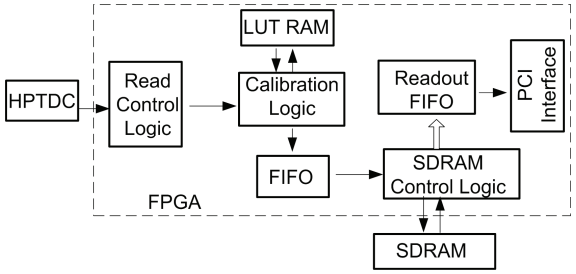

Fig.4 The architecture of FPGA logic.

Data transfer between the HPTDC and FPGA is based on the synchronous 40 MHz clocks. The 'data ready' signal is asserted by the HPTDC; and the 'get data' signal, by the Read Control Logic in the FPGA, thus registering the data from the HPTDC. The 'get data' signal is checked by the HPTDC to check whether the FPGA responds correctly. When the configured HPTDC works in very high resolution mode, the INL deteriorates the resolution of time measurement. Considering an INL repeating pattern of every 1 024 bins, caused by the HPTDC structure, a Look-Up Table (LUT) of 1 024 depth is used for INL calibration[9,12,13]. The principle of INL calibration is that a sample falling in a certain bin of the TDC is corrected by subtracting the INL value of the bin in the LUT.

A PCI core is integrated in the FPGA to achieve a data transfer rate of around 20 MB/s. An external SDRAM is used to cache the measurement results, and its memory is big enough to avoid data loss during the transfer. Further, a 1 024-word Readout FIFO is used to buffer the data from SDRAM to the PXI bus with a 100 MHz writing clock and a 33 MHz reading clock.

2.2.3 Buffer

For the COLTRIMS, the biggest average trigger rate is around 100 kHz. In average, each module from one ion impact generates about 10 hit signals. Thus, the average data transfer rate is 100 kHz ×10 hits × 4 Bytes / hit =4 MB/s, and there will be up to 16 MB/s transfer rate in the four modules. To achieve this, we

use the PCI burst transfer (1 MB block size for each burst) with its peak rate of 132 MB/s[6] being well beyond the requirement.

When the bus is occupied by transfer process of one module, the other modules must buffer their data and wait for their turns. For example, the last module waits until the other three modules complete their transfer of the total 3 MB data (1 MB data block for each module), and the data generated in the last module are well buffered. Considering an average transfer rate of 16 MB/s, the buffer size at the worst situation is no less than 1.75 MB (1 MB + 1 M × 3 modules /16 MB/s×4 MB/s·module). A SDRAM chip of MT48LS4M32B2 with 16 MB guarantees the sufficient buffering.

The FPGA controls the SDRAM, including its initialization, refreshing and burst reading/writing. A clock signal is produced by the PLL in the FPGA for data transfer with the SDRAM. Taking the refreshing and transfer process into account, the designed clock frequency of 100 MHz matches the peak rate of the PCI burst transfer.

2.2.4 Trigger

The trigger signal from the CFD system is used to reject a false hit with the trigger match function in the HPTDC. Because the hits on all detectors in a certain period of time may depend on the ion beam energy and distances of the PSDs from the hit position, a trigger is generated by the CFD system, transmitted to the Clock-Trigger module, and distributed by the star trigger buses to the TOF modules with skews of less than 1 ns. Further, the distributed triggers are delayed by the FPGA with a certain time to ensure that each trigger enters the HPTDC after all the correlative hit signals arrive. When matching the trigger, the hit time information is chosen out.

2.2.5 PCI interface logic

The PCI interface is used, and the PCI IP core is integrated in the FPGA for the data transfer to the remote PC. In Fig.5, there are two transfer modes for the PCI core of the target and the master modes, corresponding to the Target and Master Control Logic, with the module and remote PC function as the target and master. A single write or read process for the target mode is performed under the control of the PC, while the burst transfer is available for the master mode. Considering the different transfer rates, the burst transfer is selected in the master control logic for the data readout, while the target mode is used for the configuration of the master mode after initialization.

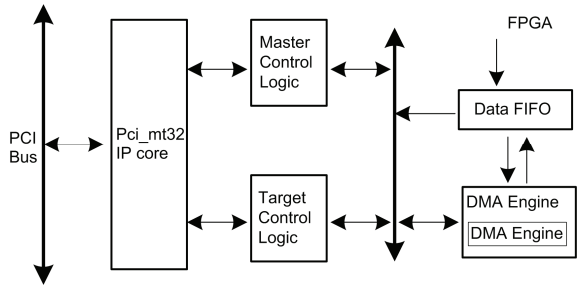

Fig.5 The structure of PCI interface logic with master control mode.

In test measurements, the DMA data transfer rate from the modules in the PXI chassis to the PC memory of the remote PC is around 90 MB/s. Compared with the peak rate of 132 MB/s, this transfer rate deterioration is probably due to the time spent on the communication between the PCI core and the remote PC. Considering the time to write the data to disks, the final data transfer rate of the whole system is still over 20 MB/s.

2.3 Clock-Trigger module

A 40 MHz high performance clock is essential to achieve the 25-ps time resolution of the HPTDC. This clock signal is generated and distributed as the working clock signals of the HPTDCs on the TOF modules (Fig.6). A temperature-compensated crystal oscillator (TCXO), EX-380, is used to remove the temperature shift effect and generate a low jitter (RMS<8 ps) LVCMOS clock. To reduce influence of the Electro Magnetic Interference (EMI), the LVDS standard is used in the clock transmission. The clock generated by the TCXO is fanned out and converted to 5 LVDS signals by a high performance clock distributor SY89113U, four of the signals being transmitted to the TOF modules, and the fifth being reserved for future use.

Also, this module distributes trigger signals from the CFD system to the 4 TOF modules via the star trigger buses of the PXI interface. The Clock-

Trigger module is located in the first peripheral slot adjacent to the system slot, to provide precise trigger signals for other peripheral slots with the dedicated lines of the star trigger buses.

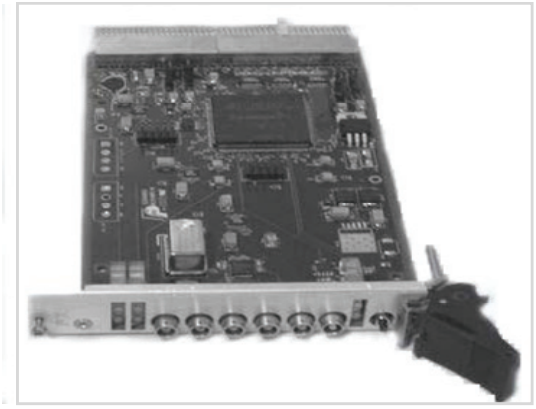

Fig.6 The Clock-Trigger distribution module.

2.4 Design of the software suite

To monitor the hit positions on PSDs, a software suite is designed to adjust system parameters. Being GUI running on the remote PC, based on Visual C++ and combined with the MATLAB platform (Fig.7), it is responsible for controling the data acquisition, analysis and display.

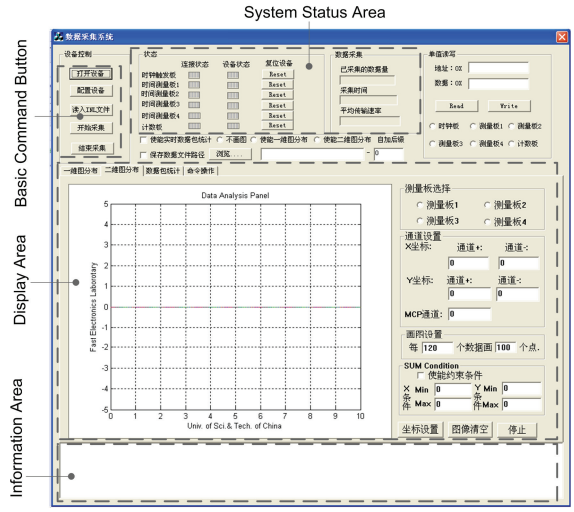

Fig.7 The picture of the GUI software.

3 Test results

A series of laboratory tests were conducted to evaluate performance of the TOF system.

3.1 The integral non-linearity test

INL describes deviation of bin characteristic of the HPTDC. Delay differences between cells engender changes in the Least Significant Bit (*LSB*) through the dynamic range. The *INL* is caused by non-ideal topology, non-uniform parasitic reactance, technological spread of the device parameters, and on-chip crosstalk from the logic part of the HPTDC chip.

A code density test was conducted for the *INL* calculation. A programmable pulse generator TEK AFG3251 was used to provide the input signal of the TOF module under test. The input signal was non-synchronous with the HPTDC working clock, thus expecting an equal number of codes in each bin. Then, the actual bin widths could be calculated by analyzing the number of hits in each bin[9].

The *INL* values can be described by Eqs.(1) and (2).

$$T_j = \sum H(i)/N_i \quad (i = 0,\ 1,\ 2,\cdot,\ j) \tag{1}$$

where, $H(i)$ is the number of counts in the i^{th} bin, and N_t is the total number of samples.

$$INL_j = (T_j - j\ LSB)\ /LSB \tag{2}$$

where, T_j is the actual cumulative bin width up to the j^{th} bin, and the j *LSB* is the ideal value.

By statistical analysis of the numbers of counts (1024 bins), the T_j obtained is used to calculate the *INL*, to correct the measurement value of the HPTDC and reduce the time measurement error. As shown in Fig.8, the worst *INL* value was 10 *LSB*, and it was improved to less than 4 *LSB*s after calibration.

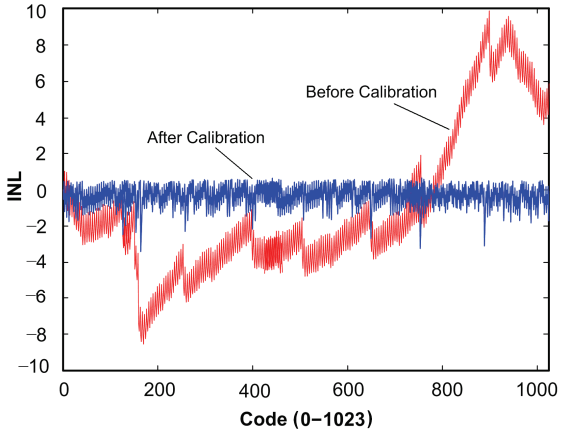

Fig.8 *INL* of HPTDC.

3.2 Time resolution test

To estimate the system's time resolution, a delay line test was conducted. Two signals generated by the AFG3251 were transmitted to the TOF module by delay lines of different lengths (insert of Fig.9). The standard deviation (RMS) of the delay time was obtained, and the time resolution of single channel was calculated by dividing the RMS by $2^{1/2}$. In Fig.9, 17.5 -ps time resolution of a single channel I was achieved after the *INL* calibration.

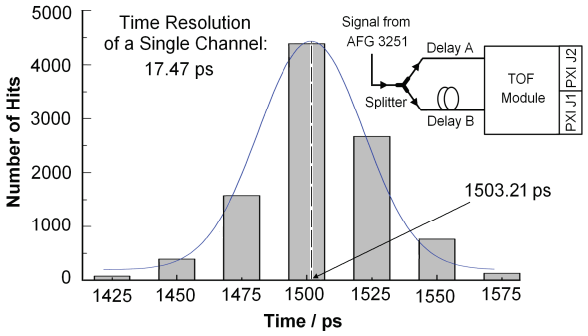

Fig.9 The result of time resolution test. The Gauss curve is fitted with the result. The insert is cable delay setup.

Fig.10 Readout system working with the COLTRIMS.

3.3 Physics experiment results

The time measurement and readout system works well at IMP on the cold target recoil-ion momentum spectroscopy (COLTRIMS) system shown in Fig.10.

He^{2+} collision on Ar was conducted. In the collision, the recoil Ar ions of different charge states were accelerated to different speeds by the electric field in the COLTRIMS, and their charge states were distinguished by measuring the TOF (Fig.11a). The hit position in PSD was calculated by signal time of the delay lines [5] (Fig.11b). The ellipse stands for sensitive area of the PSD; and the tiny points, for hit positions of most ions.

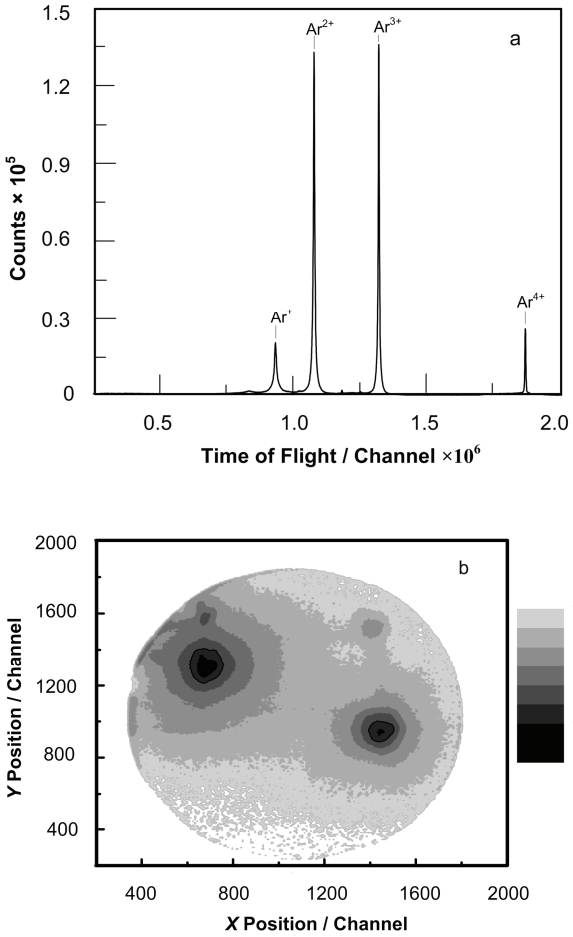

Fig.11 TOF of Ar^{+}, Ar^{2+}, $Ar^{3+}$and Ar^{4+} ions in electric field (a) and hit positions in the PSD (b)

4 Conclusions

Electronics modules of the TOF system were tested for the COLTRIMS system at IMP. The test results show that this system achieves a time resolution of better than 25 ps and a data transfer rate of over 20 MB/s. It has been working nicely in physics experiments on the COLTRIMS.

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