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Particle detector readout integrated circuit of 0.18 μm technology with 164 e equivalent noise charge

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Abstract Integrated circuits of deep submicron (DSM) CMOS technology are advantageous in volume density, power consumption and thermal noise for multichannel particle detection systems, but there are challenges in the front-end circuit design. In this paper, we present a 0.18 μm CMOS front-end readout circuit for low noise CdZnTe detectors in tens of pF capacitance. Solutions to the noise and gate leak problems in DSM technologies are discussed in detail. A prototype chip was designed, with a charge sensitive preamplifier, a 4th order semi-Gaussian shaper and several output drivers. Test results show that the chip has an equivalent noise charge of 164 e, without connecting it to a detector, with an integral nonlinearity of <0.21% and differential nonlinearity of < 3.75%.

Key words Particle detector, Readout circuit, ASIC, Low noise, Deep submicron

1 Introduction

Multichannel integration is a trend of particle detectors. Deep submicron (DSM) CMOS (Complementary Metal Oxide Semiconductor) front-end readout ASIC (application-specific integrated circuits) is attractive for designing the multichannel detection system, because DSM technologies are advantageous in power consumption, volume density, cost, and reliability[1–2], and a smaller size device contributes lower thermal noise owning to a greater g_m/C_{gs} ratio. G. De Geronimo *et al.*[3] proposed an ASIC in a 0.18 μm process. Luciano Musa *et al.*[4] presented a 32-channel general purpose charge readout chip, including analog-to-digital converters and digital signal processing part in 0.13 μm. Paul O'Connor *et al.* [5] discussed the impact of scaling down on noise optimization and pointed out the advantage of DSM technology on thermal noise.

However, DSM technologies face challenges in designing the front-end analog circuit. First, classical models[6–8] are not DSM-suitable because the noise optimization evolves more design factors. Next, for 0.18 μm processes, the gate leakage current density can be several pA/μm^2, while the input transistor of preamplifier is sized at thousands of μm^2, hence the gate current is on the order of nanoamperes, which can cause hundreds of mV voltage drop between the input and output of preamplifiers due to the feedback resistance in hundreds of MΩ. This means the input leak current must be compensated even if the detector and readout IC are AC-coupled without the electro-static discharge circuits. Finally, low supply voltage reduces swing range of the maximum output signal and the permitted overdrive voltage of transistors. For instance, the required output swing of this work is about 2.6 V, whereas the power supply voltage of 0.18-μm technology is 1.8 V. The limited overdrive voltage makes the current source noise notable, too.

Several reset and compensation methods were suggested against the gate leakage issue[9–12]. However, the normal MOSFET (MOS Field Effect Transistor) resistor configuration[9–10] is feasible only when the leakage is low and the feedback resistance is not very large. Low frequency feedback loop compensation [11] brings considerable noise because of compensation G_m block. And the configuration proposed in Ref.[12] uses a current sink to compensate input leakage current and provides discharge current, but it can only compensate leakage current in one direction by sourcing current to the preamplifier input, and is not adjustable.

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In this paper, we present a new low noise front-end readout ASIC fabricated in 0.18-μm CMOS technology, with solutions to the problems mentioned above. A backbone circuit is used as one channel of a multichannel detection system. The requirements to the ASIC are as follows: The circuit serves in a multi-channel count-mode detection system under about 10 kp/s count rate, where noise performance is of the top concern. The objective sensor is made of CdZnTe with about 20 pF parasitic capacitance. And the maximum power dissipation allowed is 10 mW. The circuit uses an enhanced noise model and an adjustable FCS (Feedback Current Sink) reset configuration is suitable for leak current of a wide range in any direction. The new FCS configuration can achieve short reset time and keep low parallel noise at the same time.

2 Architecture of whole channel

Architecture of the whole channel is shown in Fig.1. It consists of a charge sensitive amplifier (CSA), a 4th order semi-Gaussian shaper, and a Class AB output driver. The CSA is a preamplifier to convert the charge into voltage. The shaper, as a band pass filter, is the main amplifier to improve signal noise ratio[6].

The CSA is of AC-coupling with the sensor. The reset subsystem in the CSA stabilizes the preamplifier operation point and discharges the feedback capacitance (C_f). The reset part of this circuit can be equivalent to a resistor (R_f). An improved feedback current sink reset configuration, which is suitable for leakage current in any direction, is adopted to compensate the input leakage current without large voltage offset.

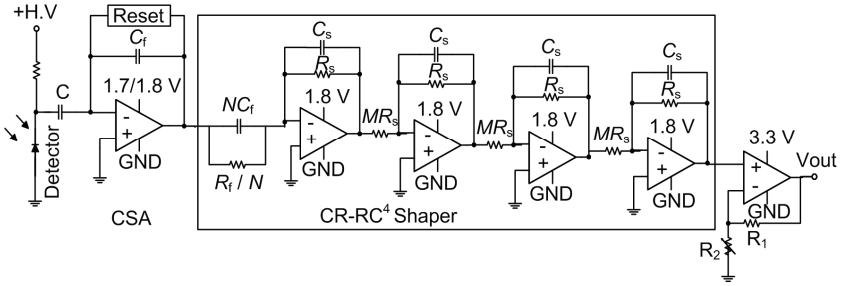

Fig.1 Architecture of the readout ASIC.

The semi-Gaussian shaper is composed of a C-R stage and four 1st order integrators. Transfer function of the CR-(RC)^4 filter is given by

$$H(s) = [NR_s/(M^3R_f)]\,[(1+s\tau_f)/(1+s\tau_s)^4] \quad (1)$$

where, N is ratio of the C-R stage capacitance to C_f, M is the close loop DC gain of every integrator, $\tau_f = R_f C_f$ is the time constant of the CSA feedback circuit, $\tau_s = R_s C_s$ is shaping time, and s is Laplace operator. The peaking time is 4 times τ_s for such a 4th order shaper. Both N and M are decided by the gain of the whole channel. The zero produced by the C-R stage is able to cancel the pole produced by the feedback part of CSA when the resistance and capacitance of the C-R stage is selected to be equal to R_f/N and NC_f, respectively. The last stage is a Class AB output driver. The gain of driver can be adjusted.

The circuit has three supply voltage levels. The supply voltages of input transistor are 1.7 V and 1.8 V. According to the design requirement, the gain of whole channel is 300–400 mV/fC, and the input charge of 1000–20 000 e, hence corresponding to output pulse peak is about 2.6 V. Therefore, the output driver adopts the Class AB configuration with 3.3 V supply voltage. For the other circuits, 1.8 V is used, which is the standard voltage of 0.18 μm technology.

3 Optimizing the preamplifier and shaper

3.1 Core amplifier

The input device is of importance in noise characteristic of the whole channel, and its noise optimization is the primary issue. The noise of front-end is mainly composed of the channel thermal noise and the flicker noise of the input transistor, and the shot noise related to the detector bias and leak current. The equivalent noise charge (*ENC*) related to the input transistor can be written as Eq.(2),[2]

$$ENC^2 = (C_{in} + 2C_{ov}W + C_{gw}W)^2 \left[\frac{\alpha_w n\gamma 4kT}{\tau_p g_{mw} W} b_w + \frac{K_f (2\pi)^{\alpha_f}}{C_{ox} WL \tau_p^{1-\alpha_f}} b_f(\alpha_f) \right] + 2qI_l \tau_p b_p \quad (2)$$

where, C_{in} is the detector capacitance, C_{gw} is the unit width gate capacitance of input MOSFET, W is the gate width, L is the gate length, g_{mw} is the unit transconductance, K_f is the coefficient of flick noise, n is the sub-threshold slop coefficient, τ_p is the peaking time, α_w is the excess noise factor, α_f is a coefficient of technology, b_w, b_p, τ_p, and $b_f(\alpha_f)$ are determined by the filter[2], and I_l is the gate leakage of the input transistor. The first term of Eq.(2) is the thermal noise, the second term is the flicker noise, and the last one corresponds to the parallel noise.

According to Eq. (2), PMOS is chosen as the input transistor because of its lower gate current and flicker noise than NMOS. With a desired shaping time of 1.5 μs, the flicker noise shall contribute more than thermal noise. Therefore, the PMOS drawback of relatively low transconductance becomes a secondary factor.

For the input transistor, an EKV model-based noise optimization model is used. Its noise components are expressed with design parameters of W, L and i (inversion coefficient). Then, the first two terms in Eq.(2) become

$$ENC_{wf}^2 = \left(C_{in} + 2C_{ov}W + C_g(i)WL \right)^2 \left[\frac{\alpha_w T(i)}{\tau_p W/L} b_w + \frac{K_f (2\pi)^{\alpha_f}}{C_{ox} WL \tau_p^{1-\alpha_f}} b_f(\alpha_f) \right] \quad (3)$$

$$T(i) = \frac{n^2 [0.5 + \frac{1}{6}(i+1)^{-1}] 4kT\varphi_T}{if(i) I_{dst}}, \qquad C_g(i) = C_{ox} \left[\left(\frac{3}{2} + \frac{1}{if(i)} \right)^{-1} + \frac{n-1}{n} \left(1 - \frac{f(i)}{1 + 1.5if(i)} \right) \right]$$

where, ϕ_T is the thermal voltage, $f(i)=(i+0.5\times i^{0.5}+1)^{-0.5}$ is $g_m/(I_D n\phi_T)$, I_{dst} is the transition current between strong inversion and weak inversion, and $T(i)$ and $C_g(i)$ are the impact of i on thermal noise component and flicker noise component, respectively. Thus, ENC_{wf} is the secondary effects of DSM MOSFET in moderate inversion in a continuous function.

Based on Eq.(3), an MATLAB program was developed to optimize the parameters of W, L and i, taking the noise contribution of non-input transistors and stability requirements into account, as they affect the optimization of the input MOSFET in DSM technologies. For instance, the thermal noise of transistors M4 and M5 in Fig.2 increases with their g_m. In the DSM technologies, the current source noise is among the top 5 noises, because the overdrive voltages of current source transistors are limited by lower supply voltage. The same drain current has higher g_m and produces more thermal noise. As a result, the selection of drain current of input transistor should consider the impact of drain current value on the current source noise. Additionally, the power and stability requirements limit the parameter selection of input transistors. Therefore, with the MATLAB program, optimum range could be defined by influences of other transistors noise optimization, requirement of power dissipation, and the given product of gain and bandwith. Details of the enhanced noise optimization model and its derivation can be found in another article[13]. Finally, parameter of the input FET decided by the optimization program are W = 4.83 mm, L = 470 nm.

Also, secondary noise components of the preamplifier were considered in the noise optimization [2]. The contribution to the equivalent input noise voltage by substrate noise of the input transistor, R_B, is in proportion to $R_B(g_{mb}/g_m - 1)^2$. To minimize the g_{mb}, the source-substrate junction is reversely biased. In Fig.2, this is realized by reducing the source voltage of M1 to 1.7 V while connecting the bulk to 1.8 V. A reversed bias of the junction reduces static power of the input stage, too. Besides, power of the input device dominates power of the amplifier.

The second noise is produced by current source (M4 and M5) as mentioned above. In Fig.2, the core amplifier uses a single-ended input split-leg dual cascode configuration[11], which has smaller total bias current for the same input transistor drain current. As

argued in Ref.[14], adding source feedback resistors to M4 and M5 can minimize their flicker noises. The additional cascode transistor suppresses the Miller effect of the gate-drain capacitance of M1 and reduce the charge shared away.

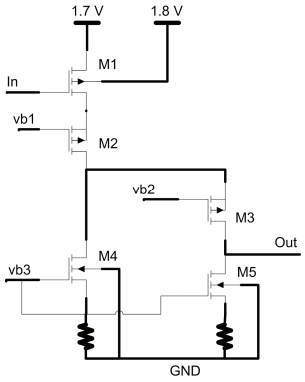

Fig.2 Schematics of the core amplifier.

3.2 Improved FCS configuration

Figure 3(a) shows an FCS reset configuration[12]. The M1 works as a current sink to generate the discharge current of $C_{f,}$ and compensate the input leak current. A negative feedback amplifier composed of M4 and M3 controls gate voltage of M1. The M2 and C_2 work as the C-R stage of the shaper to cancel the pole of the FCS-C_f part.

But this FCS is not suitable for the variation of the input leakage current because it compensates leakage current in pull direction only. Fig.3(b) shows an equivalent circuit about input node currents. Three resistors are connected to the input node. When the compensation circuit is off, the R_{iu} and R_{id} are the equivalent resistance of the DC leak paths (through the ESD protection circuit, gate oxide of M1 or detector) to V_{DD} and ground, respectively. The compensation aims to stabilize the input and output at desired operating voltages. Therefore, the current through R_f should equal to the defined I_f under stable situation for a given R_f. Then the compensation current (I_c) should be $I_c=I_u-I_d-I_f$.

The I_u and I_d depend on R_{iu} and R_{id} in determining operation point of the input node. If I_u-I_d is less than the value of I_f, a push compensation leakage ($I_c<0$) will be required. But the R_{iu} and R_{id} vary with process and ambient temperature, and it is difficult to estimate them accurately in the design because the SPICE models of 0.18 μm process do not contain gate leak information. Therefore, a post-silicon tuning mechanism generating I_c in both directions with different values is necessary. In order to generate push compensation current, a complementary part is added into the reset block. At the same time, an additional external bias current is introduced into the feedback amplifier to make the operating point of amplifier tunable.

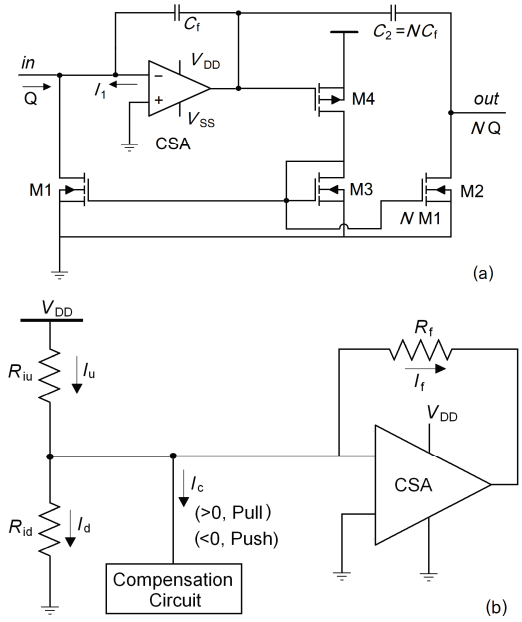

Fig.3 Schematics of (a) the feedback current sink configuration and (b) the simplified model of the improved configuration.

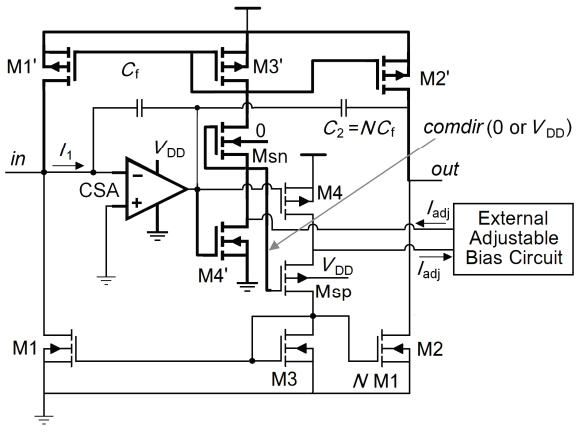

Fig.4 Schematics of the adjustable configuration.

The complete reset block configuration is shown in Fig.4. The devices in bold form the push part to provide push compensation current, with the M1–M4 and M1′–M4′ forming two symmetric structures. Msn and Msp are two switch transistors. With a full compensation current, *comdir* is connected

to ground, Msn is switched off and Msp is switched on, then only the pull part works; while with the need of a push compensation current, *comdir* is connected to V_{DD}, Msn is turned on, and Msp is turned off.

In addition, two identical adjustable bias currents (I_{adj}) in opposite directions are fed into M4 and M4′, respectively. Thus, the bias current of M4 is

$$I_{d4}=I_{adj}+BI_1=k_4(V_{DD}-V_{G4}-V_T)^2 \quad (4)$$

$$V_{G4} = V_{DD} -[(I_{adj}+BI_1)/ k_4]^{1/2} +V_T \quad (5)$$

where, I_1 is the drain current of M1, and B is the size ratio of M3 to M1, and k_4 is the gain factor of M4. Therefore, V_{G4}, the output node of the CSA, can be fixed by adjusting I_{adj} when I_1 deviates from the value expected. If I_1 is less than expected, I_{adj} should increase; otherwise it should decrease. The case of push part is similar.

The noise contribution of this reset circuit involves just M1. However, noise originating at the gate of M3 generates a current through M1, C_f, and C_2, and the current is fully absorbed by M2, hence no noise contribution to the output[12], while the adjustable bias circuit does not increase the noise. The noise of M1 is the parallel noise. According to Eq.(2), we have

$$(ENC)^2_{M1}= (8\ k\ Tg_{m1}\tau_p\alpha_p)/3 \quad (6)$$

where, g_{m1} is the transconductance of M1. Compared with original FCS, noise caused by the complementary part is negligible because it is fully cut off when the other part is active. The main noise comes from the additional input capacitance, which is negligible compared with detector capacitor in tens of pF.

Equivalent resistance of the reset block (R_f) is

$$R_f= (g_{m3}/g_{m1}g_{m4}) =(B/g_{m4}) \quad (8)$$

where, g_{m3} and g_{m4} are the transconductances of M3 and M4, respectively. The adjustable bias current (I_{adj}) increases the static current of M4 and M4′, which leads to larger g_{m4}, and R_f becomes lower than the original one for the same leak current. This facilitates shortening the decay time of CSA output steps. Smaller decay time is in favor of suppressing pileup. Since the ENC_{M1} is independent of current of M4 and M4′, introducing I_{adj} has little impact on noise performance.

3.3 The shaper

The semi-Gaussian shaper in Fig.1 is widely adopted in particle detector readout circuits[6,14,15]. Although a higher order integrator has better noise performance, we decided the order number is 4, and four first order stages with similar circuits are used, because integrators of orders above 4 does not bring much *ENC* improvement (less than 2 e), as our simulation results show. The peaking time of τ_p= 1.5 μs is an optimized result to minimize the noise of output signal under the given detector capacitance of 20 pF. The feedback resistors and capacitances (R_s and C_s) are realized with passive components because the noise performance is not sensitive to the shaping time.

The noise performance was estimated using a circuit shown schematically in insert of Fig.5(a). C_d is the detector capacitance. A 52-MΩ resistor is shunt at the input node to simulate the noise current (1 nA) associated with the detector and its bias network by its thermal noise. The voltage source applies a block pulse (in amplitude of V_s) on a test capacitor (C_{source}) at the input, with the V_sC_{source} being approximately the input charge.

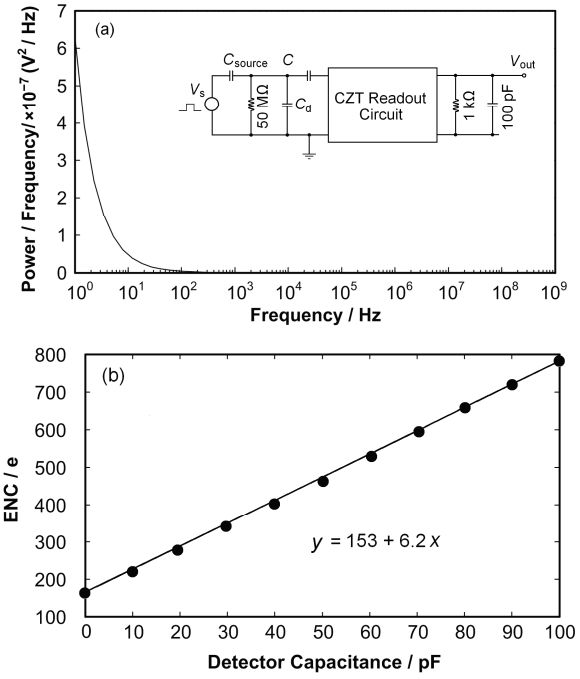

Fig.5 Simulated noise power spectrum of output node and ENC *vs* detector capacitance (τ_s=1.5 μs). The insert in Fig.5(a) is the equivalent circuit for simulating the *ENC*.

The power spectrum of output noise was simulated (Fig.5a) and its integral is the total output noise power. The *ENC* was obtained by dividing it using the voltage/charge gain of the circuit. The *ENCs* simulated with respect to different detector capacitance at typical corner are shown in Fig.5(b). The *ENC* is about 274 e with the detector capacitance of 20 pF. Simulated with the Spectre code, the total power dissipation of the circuits was about 10 mW.

4 The fabricated chip and test results

4.1 Chip

A prototype chip was designed and fabricated in the SMIC 0.18 μm CMOS mixed-signal process, containing several output buffers of intermediate signals for testing the circuits. The input pad connected with detector has electro-static discharge protection circuit. The chip, sized at 1.33 mm×0.725 mm, is shown in insert of Fig.6.

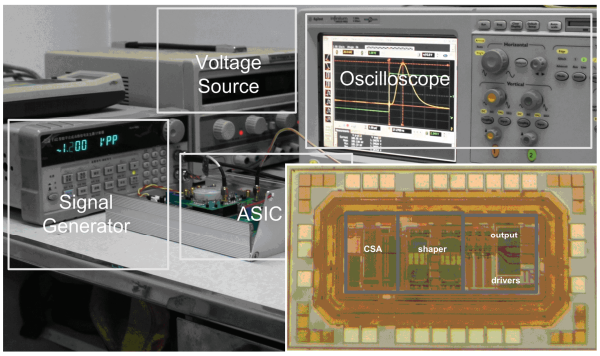

Fig.6 The instruments to test the fabricated circuit (the insert).

4.2 Testing method

The test instruments are shown in Fig.6. The input signal from a square-wave was generated by a generator after an attenuation of 200:1, and fed to input pin through an on-board 0.5 pF coupling capacitor and a 100 pF DC isolating capacitor. The test chip worked correctly by connecting the *comdir* to ground. Fig.7 gives the tested waveforms of the input square wave and the output signal of the shaper. The peaking time of test chip is 1.31 μs.

The decay time and DC voltage of the CSA output are adjustable through the external bias. Fig.8 shows that the CSA output waveforms at one input pulse under different I_{adj} values. The CSA output amplitude was normalized. The I_{adj} was adjusted to make the chip work in the best status, but the optimal I_{adj} was larger than the designed value, indicating that the actual leak current is lower than the expected. All the following tests are performed under the optimized I_{adj} value.

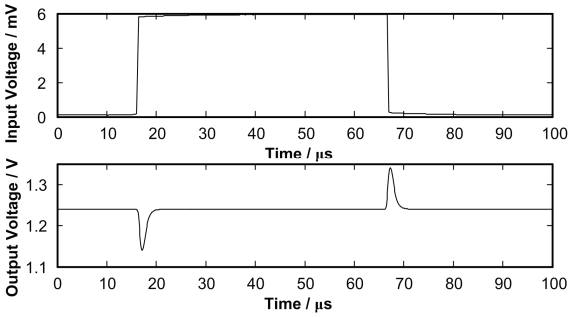

Fig.7 Testing waveform of input and output signal.

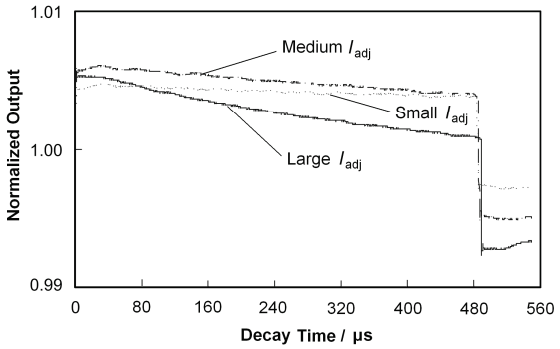

Fig. 8 Normalized CSA output for different I_{adj} values.

4.3 Equivalent noise charge evaluation

The method of measurement is as follows: First, peak-to-peak voltage of the attenuated input signal was set as V_{s1}=3.5 mV, with about 11000 e input charges, and frequency of the input signal was 10 kHz. The average output amplitude, V_{o1}, was calculated after 256 samplings. Next, peak-to-peak voltage of the input signal was $V_{s2.}$ = 6 mV, with about 19 000 e input charges, and the output amplitude V_{o2} was obtained in the same way as V_{o1}. Then, the gain of chip was calculated by $Gain=[(V_{o2}-V_{o1})/(V_{s2}-V_{s1})]C_{source}$. Finally, root-mean-square (RMS) voltage of output signal was measured by the oscilloscope under sampling rate of 50 M/s, which is about the forth power of the bandwidth of shaper (about 2.7 MHz). Fig.9 shows a section (about 650 μs) of output noise and its power density in frequency domain.

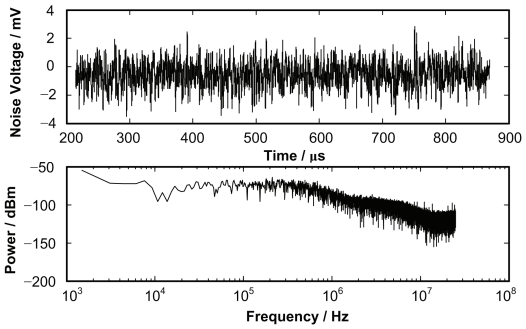

Fig.9 Noise voltage and power spectrum of output when turning off input.

The stable mean value after several minutes was read out as the RMS estimation (V_{rms}), and the *ENC* was calculated by $ENC = V_{rms}/Gain$. The V_{rms} was estimated at about 892 μV, and the *Gain* was measured at about 33 mV/fC. Thus, the *ENC* was about 168 e without the connecting detector. The difference between the measured and simulated values could be caused by noise from the test system, the parasitic capacitors of input pad, ESD protection circuit, bonding wire and on-board pin, and changes in voltage and temperature. Nonetheless, the error on input charge is estimated and corrected, and the error from the injected charge was shared away by the coupling 0.5 pF capacitor. Thus, the actual injected charge had a coefficient of about 0.976, which equals to 20–20.5 pF (the input capacitance of the testing IC is 20 pF). After correction, the *ENC* is 164 e.

4.4 Integral nonlinearity and differential nonlinearity

Figure 10 shows the measured output amplitude of shaper *vs* peak-to-peak voltage of input pulse from 0.1 to 1.2 V. The measured integral nonlinearity (*INL*) is 0.21%, and differential nonlinearity (*DNL*) is 3.75%.

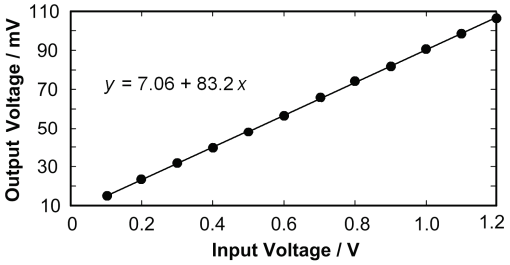

Fig.10 Testing data of output peak voltage vs. input voltage.

4.5 Performance comparison

The performance of this work and the designs in Ref.[4,11,12,15] are listed in Table 1. Generally, the designs in DSM process (this work, Musa[4] and BNL2004[12]) have lower noise. Our work, with the improved FCS leak compensation configuration, has lower noise than the design of G_m method (BNL 2007 [11]). If our work achieves the same *ENC*-capacitance slope as the simulation result of 62 e /10 pF in Fig. 5(b), its noise would be lower than the others.

Table 1 Performance of the ASICs.

Design	Our work	Musa[4]	BNL2004[12]	PKU[15]	BNL2007[11]
ENC	164e⁻(w/o det.)	300e⁻@12 pF	250e⁻@5 pF	500–700e⁻(w/o det.)	350e⁻(w/o det.)
Peaking time / μs	1.31	0.100	0.600	0.6–1.6	0.100
INL / %	0.21	/	0.2	0.8	/
DNL / %	3.75	/	/	/	/
Gain (mV/fC)	33–396	/	/	13–130	4.5–31.7
Static power dissipation / mW	10	9	/	/	9.6
Process / μm	0.18	0.13	0.25	0.35	0.35

5 Conclusions

This paper presents a front end ASIC in a deep submicron CMOS technology. The ASIC is designed for the CdZnTe particle detectors. This work proposes that a reset configuration can compensate the gate leakage current of a DSM transistor and the current is adjustable. The core operating amplifier is optimized based on a novel more accurate noise model. The novel model takes the special effects of DSM technology into account. The final output driver uses 3.3 V for the purposed of providing enough swing range to output signal. With these techniques, about 153 e + 62 e /10 pF *ENC* in simulation can be

achieved by the presented ASIC. The fabricated chip can work correctly with ESD protected input PAD, and has 164 e *ENC* without connected detector, 0.21% *INL*, and 3.75% *DNL*.

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