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A time-sharing multi-channel pulse amplitude analyzer

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Abstract A conventional multi-channel pulse amplitude analyzer acquires single energy spectrum, but provides no information on its tendency with time. To address the limitation, we propose a scheme of time-sharing multi-channel pulse amplitude analyzer (TSMCA). A dual-port random access memory is divided into two storage spaces, one for current energy spectrum data acquisition and another for previous energy spectrum data storage. The two tasks can be performed simultaneously, and the time-related variation tendency of energy spectrum can be obtained. A prototype system of TSMCA is designed. It performs nicely, with maximum channel number of 4096 in capacity of 2^{32}/Ch, minimal time-sharing slice of 25 ms, the differential nonlinearity of <1.5%, and the integral nonlinearity of <0.3%.

Keywords Multi-channel pulse amplitude analyzer · MCA · Time-sharing · ADC · Dual-port RAM

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1 Introduction

MCA, a basic instrument in nuclear electronics, is extensively applied in nuclear measurements [1, 2], and it has been in continuous development [3, 4], including various data processing and data transmission codes, and various types of devices, such as data processors based on field programmable gate array (FPGA) [5, 6], complex programmable logic device (CPLD) [7], advanced RISC machines (ARM) [8, 9], and digital signal processors (DSP) [10], data transmission systems based on universal serial bus (USB) [11], Ethernet network [12], and direct memory access (DMA) transmission [13], as well as the controlling software based on the Linux [14] or Windows [15] platform.

However, a conventional MCA [16, 17] has a major limitation. It cannot implement continuous measurement to obtain time-related energy spectral variation tendency. In this paper, we propose a time-sharing multi-channel pulse amplitude analyzer (TSMCA) utilizing DPRAM (dual-port random access memory) to implement the time-sharing measurement. By using successive approximation register ADC (SAR ADC), the good property of differential nonlinearity (DNL) and integrated nonlinearity (INL) is preserved.

2 Principle of scheme

2.1 Peak holding circuit (PHC)

Figure 1 shows schematically the peak holding circuit (PHC). It mainly consists of a voltage amplifier U1, peak detector diode D1, feedback resistor R1, holding capacitor

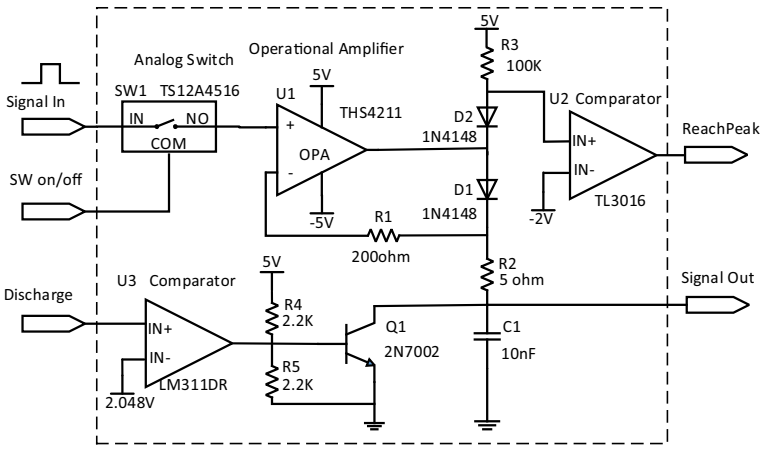

Fig. 1 Schematics of the peak holding circuit

C1, and a damping resistor R2. U1 amplifies the difference between the input and output voltages (V_{in} and V_{out}). If V_{out} is less than V_{in}, C1 is charged by V_{out} through D1; if V_{out} is greater than V_{in}, D1 is cut off and the voltage of C1 remains unchanged. Analog switch SW1 is used for controlling whether the input signal is allowed to enter into the next level circuit or not. U3 receives "discharge" signal from MC; then, Q1 provides a discharge path for C1. R3 and D2 are used for the peak signal detection, and U2 is used for "ReachPeak" signal shaping.

2.2 SAR ADC

ADC is an important element in an MCA. An SAR ADC is of high conversion speed, with worse DNL, though. In our design, by dropping lower bits of ADC, the SAR ADC shows a preferable DNL. To elaborate the relationship between preferable DNL and dropping bits, we take the SAR ADC (model AD7674 [18], ADI company) for example. The conversion time is 1.5 μs (counting rate 666 kSPS), the resolution is 18 bits, and the maximal DNL is 1.75 LSB (least significant bit). By keeping the higher 12 bits and dropping the lower 6 bits, the new minimum step size is 2^7 LSB, then the $NEW\ DNL = 1.75/2^7 = 0.0137$ LSB. After our modification, the DNL performance can be improved significantly.

2.3 DPRAM

Generally, DPRAM [19] has one storage space and two independent operation ports. In our design, we divide the storage space into two identical parts, one part and the left port are used for data acquisition and storage of current spectrum, another part and the right port are used for the storage and transmission of previous spectrum data. These two parts will be switched according to the time slice.

2.4 TSMCA

Figure 2 shows the block diagram of our TSMCA. The PHC holds peak amplitude of input signal. The ADC converts the peak amplitude into digital bits. The DPRAM stores time-sharing spectrum data. The main controller (MC) controls ADC and the left port of DPRAM for data storage. The transfer controller (TC) obtains the time-sharing spectrum data through the right port of DPRAM, then uploads it to USB controller, while controls the switch of two storage spaces according to the time slice. The USB controller receives the instruction from PC and transmits the time-sharing spectrum data to it. The PC controls the system and processes the received data.

The system procedure works as follows (taking the DPRAM with 2^{12} bit storage space for example):

1. PC sends relative parameters to TSMCA for its initialization, the storage space of DPRAM is set at zero. After that, TC sets $L\_ADDR12 = 0$, $R\_ADDR12 = 1$. It means MC can store the acquisition data into low storage space, while the higher storage space is idle.
2. After TSMCA receives "start" from PC, USB controller sends "ready" to MC. Then, MC sends "SW on" to PHC, which opens the analog switch to allow the signal enters into the next level circuit. The PHC holds the peak amplitude and sends it to ADC, and sends "ReachPeak" to MC. Then, MC sends "Cnvst#" to ADC to start the conversion and sends "SW off" to PHC to close the analog switch to prevent the signal from entering in. After conversion, the output digital bits of ADC are sent to the left port of DPRAM as its address information. Then, MC reads the corresponding "*DATA*" at the address, makes $NEW\ DATA = -DATA + 1$, and writes the "*NEW DATA*" to the same address. After that, MC opens the analog switch by sending "SW on" to PHC, the system waits for next signal input.

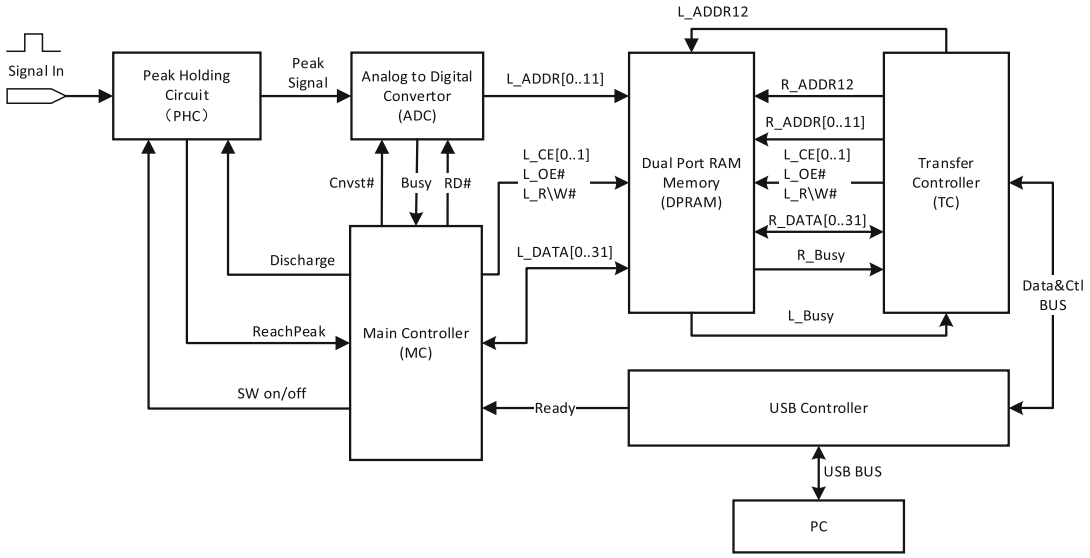

Fig. 2 Block diagram of the TSMCA

3. When the time slice is up, TC switches the two storage space by setting $L\_ADDR12 = 1$, $R\_ADDR12 = 0$. The acquired data are stored in the higher-address storage space, while TC reads the stored data in the lower-address storage space, transmits it to PC, initializes the lower-address storage space, and waits for the next time slice.
4. When the next time slice is up, TC switches the two storage space by setting $L\_ADDR12 = 0$, $R\_ADDR12 = 1$. The acquired data are stored in the lower-address storage space, while TC reads the stored data in the higher-address storage space, transmits it to PC, initializes the higher-address storage space, and waits for the next time slice.
5. Steps 3 and 4 are repeated. By switching storage spaces, current data acquisition and previous data transmission can be performed simultaneously.
6. On receiving "stop" instruction from PC, the system stops data acquisition and transmission.

3 Results and discussion

The critical IC chips are listed in Table 1. The prototype system of TSMCA we designed is shown in Fig. 3. The system performance is demonstrated in a test environment.

Table 1 List of critical IC chips

Chips	Model	Manufacturer
Operational amplifier	THS4211 [20]	TI
ADC	AD7674	ADI
Dual-port RAM	CY7C056V	Cypress
USB controller	CY7C68013 [21]	Cypress

The signal generator outputs its generated pulse to the TSMCA through a coaxial cable, and then, TSMCA uploads its processed data to PC for analysis.

3.1 The response characteristic of pulse amplitude

The output of signal generator is set at 3 μs of width, 20 kHz of repetition rate, and 0 mV–4.0 V of adjustable pulse amplitude. The TSMCA channel address as a function of the input pulse amplitude is shown in Fig. 4, with a good linearity of $y = -27.94 + 1.01x$. The intercept is the electronics bias, so the input signal amplitude must be greater than 27.94 mV.

3.2 INL property

According to the channel address of each input pulse, we can get the array (m_{pi}, A_{pi}), where m is the input pulse amplitude, and A is the channel address. Then, the deviation between each measured point and the fitted curve is

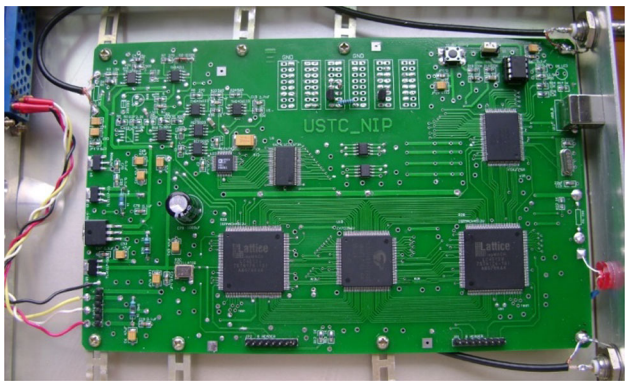

Fig. 3 PCB of the TSMCA

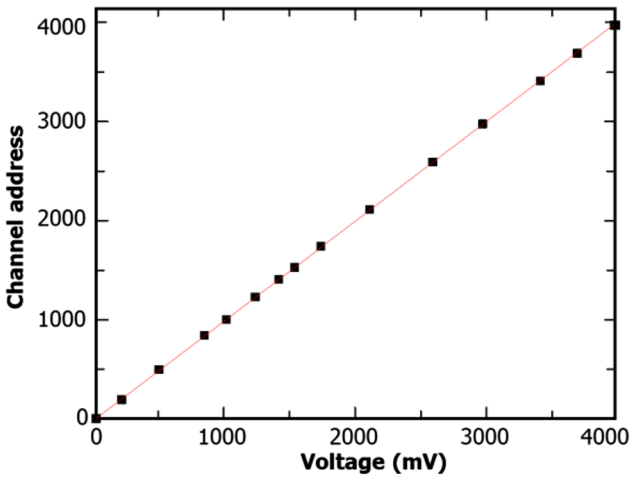

Fig. 4 Linearity between voltage and channel address

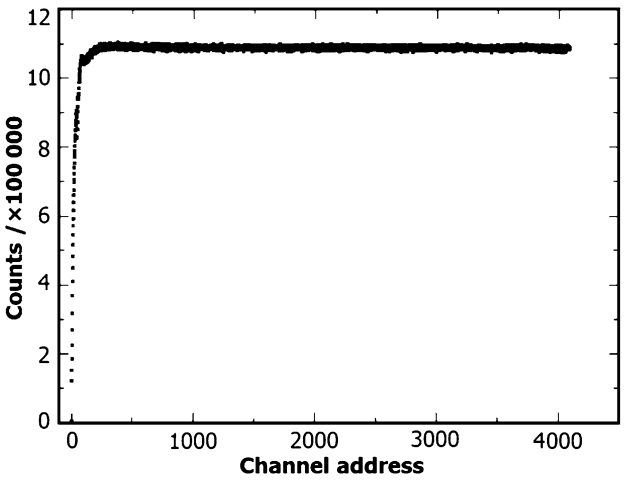

Fig. 5 Counts of channel address

calculated as ΔA_{pi}. The INL property is determined by $INL = (|\Delta A_{pi}|_{max}/A_{max}) \times 100\%$, with $A_{max} = 4096$ and $|\Delta A_{pi}|_{max} = 10.79$, thus $INL = 0.26\%$.

3.3 DNL test

The signal generator is a slip pulse generator, which outputs rectangular pulse sequence with variable amplitude, frequency, and pulse width. In a slip cycle, the amplitude increases linearly from zero to maximum value and then reduced linearly from the maximum value to zero. In this test, the slip pulse generator outputs 0 mV–4.16 V pulses of 2.8 μs width, 100 kHz repetition rate, and 25 s triangular-wave modulation period. Record the time-sharing spectrum data, and stop the test when the accumulated count of each channel reaches 1,100,000. The counts as a function of channel address of TSMCA are shown in Fig. 5. The counts are uniform and smooth for channel addresses of 200–4095, but the DNL value worsens at lower channel addresses, due to the poor linearity of PHC in the small signal region.

The counts of channel addresses of over 200 are picked out for analyzing DNL performance, with a proportion of 95% in the total channel address. DNL is calculated by $DNL = (|N_i - N_{mean}|_{max}/N_{mean}) \times 100\%$, where N_i is the count of each channel address, N_{mean} is the average count of total channel address. The DNL distribution of channels 200–4095 is shown in Fig. 6. With a maximal DNL of 1.41%, the DNL performance is good.

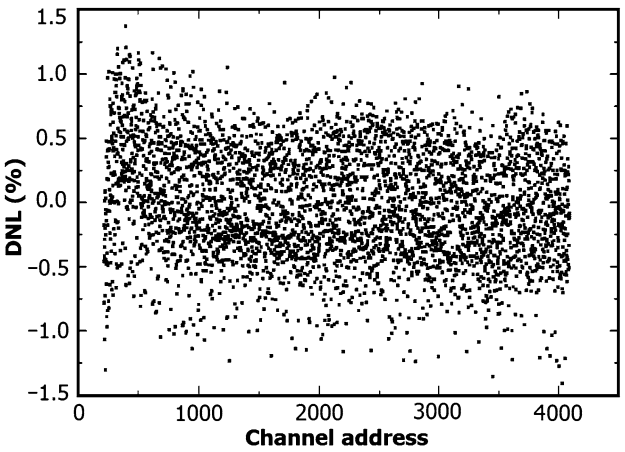

Fig. 6 Results of DNL analysis (Channels 200–4095)

3.4 Energy resolution

The output of signal generator is set at 3 μs width, 100 kHz repetition rate, and 3.2 V pulse amplitude. The counts in corresponding channel address are shown in Fig. 7. The channel address indicates the energy information. The

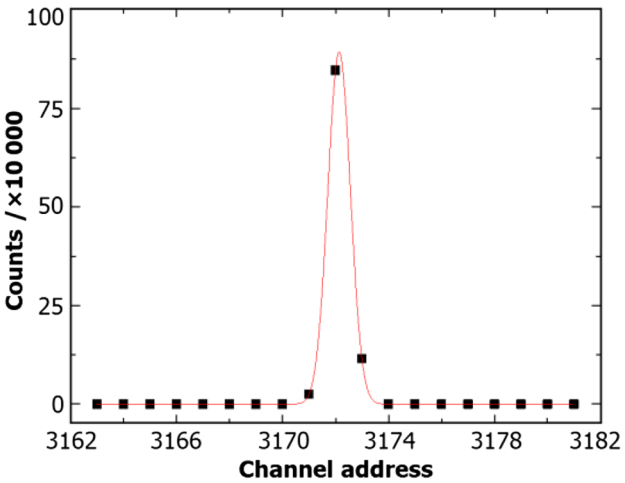

Fig. 7 Results of energy resolution test

Table 2 Performance of TSMCA and conventional MCA

I Items	II TSMCA	III BH1324
Channel number	4096	4096
Channel capacity	2^{32}–1	2^{24}–1
DNL (%)	<1.5(channels 200–4095)	≤1.6%
INL (%)	<0.3%	≤0.1%
Input signal (V)	0.3–4.096 V	0.1–5.5 V
Time slice	25 ms to 107,374,182.4 s, in 1 ms steps	–

FWHM of the peak is just 1 channel, showing good energy spectrum resolution of the TSMCA.

3.5 Time-sharing energy spectrum

The output of signal generator is set at 3 μs width, 20 kHz repetition rate, and 3.2 V pulse amplitude, and TSMCA works in time-sharing mode at 1000 ms time slice and 10,000 ms total test time. Record each count of time-sharing energy spectrum, the count variations show the varying tendency of energy spectrum. Since the output of signal generator is a periodic signal, the values of these counts are nearly identical.

3.6 Performance comparison

Performance of TSMCA and a conventional MCA (BH1324 [22], Beijing Nuclear Instrument Factory) is shown in Table 2. It can be seen that the TSMCA has the additional function of the time-sharing measurement, while achieving similar technical performance as the conventional MCA.

Considering future development, the TSMCA can be improved from two aspects:

1. Since the TSMCA performance is closely related to the ADC, higher counting rate can be achieved by using a higher speed ADC, and better DNL performance can be achieved by using a higher resolution ADC.
2. The time slice of TSMCA is limited by transmission time. To get shorter time slice, faster transmission media can be chosen, such as Gigabit networks, USB3.0, and peripheral component interface express (PCIE) bus.

4 Conclusion

The basic idea of a prototype TSMCA has been presented. Compared to conventional MCAs, TSMCA can achieve continuous measurement and thereby capture the energy variability with time. By separating the storage space of DPRAM, the current and previous spectrum data transitions can be performed simultaneously and independently. By comparing the time-sharing spectra, the time-related energy variation tendency can be obtained. By using SAR ADC, the good property of DNL and INL can be preserved. Test results of the prototype TSMCA show good linearity between voltage and channel address, with the INL of 0.26% and maximum DNL of 1.41%, which is very close to the theoretical value 1.37%. The energy spectrum resolution (FWHM) is just 1 channel. Our scheme of the TSMCA is feasible, and the design idea of TSMCA can be extended to other fields.

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