Research on total-dose irradiation effect of hardened partially-depleted NMOSFET/SIMOX

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Abstract In this work, top and back gate characteristics of partially-depleted NMOS transistors with enclosed gate fabricated on SIMOX which is hardened by silicon ions implantation were studied under X-ray total-dose irradiation of three bias conditions. It has been found experimentally that back gate threshold shift and leakage current were greatly reduced during irradiation for hardened transistors, comparing to control ones. It has been confirmed that the improvement of total-dose properties of SOI devices is attributed to the silicon nanocrystals (nanoclusters) in buried oxides introduced by ion implantation.

Keywords Silicon on insulator, Ion implantation, Total-dose irradiation effect, Enclosed gate, Threshold voltage shift, Leakage current

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1 Introduction

Silicon-on-insulator (SOI) technology offers some hardness advantages over bulk-silicon technologies for space and other applications. For example, properly designed SOI circuits are less prone to single-event upset from energetic cosmic particles than equivalent bulk-silicon ICs. However, the positive charge buildup in buried oxide (BOX) makes hardening SOI devices for use in total dose radiation environments (e.g., space) much more challenging than for bulk-Si devices[1,2]. Large concentrations of oxides-trapped charge cause large negative threshold-voltage shifts, even result in device failure by shifting the operating voltage. Positive charge trapping in the buried oxide can reverse the back-channel interface of partially-depleted n-channel transistors, forming a conductive channel between the source and drain. This can lead to large increases in leakage current in ICs using partially-depleted transistors.

Ion implantation has been proved to be an effective way to prepare rad-hard materials. There has been considerable research on hardening SIMOX materials in recent years, developing a variety of hardening techniques as discussed below. Multiple oxygen implantation followed by multiple annealing after each implantation can improve the BOX by reducing its sensitivity to irradiation. Supplemental oxygen implantation is used to improve the top Si-BOX interface properties and reduce the number and size of Si islands in the buried oxide without significantly damaging the electron trapping and hole trapping during irradiation. Internal thermal oxidation can improve the quality of the top Si-BOX interface and reduce the number of the charge traps. Fluorine ions are implanted into SIMOX to improve the conductivity property of BOX so as to harden SOI devices under radiation conditions. Nitrogen ions are implanted into SIMOX to harden buried oxides, for the nitrogen annealed buried oxides, the enhancement in hardness can be attributed to the formation of an interracial oxynitride layer, which would introduce deep electron

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trap to lead to reduction in back-gate threshold voltage shift. Nitrogen-oxygen co-implantation can also result in the formation of an interracial oxynitride layer.

Recently, silicon ions implantation has been an attractive and promising method to harden the buried oxides of SIMOX. A number of studies[3,4] has been done to research the irradiation properties and its mechanism of silicon-implanted SIMOX and transistors fabricated on SIMOX. Our research is concentrated on the total-dose irradiation effect of hardened partially-depleted NMOS transistor with edgeless enclosed gate fabricated on silicon-implanted SIMOX.

2 Experimental

The studied NMOS/SOI transistors were fabricated on SIMOX wafers with front silicon thickness of 200 nm and BOX thickness of 380 nm, which is appropriate for scaled deep submicron devices. One wafer was hardened by implanting silicon at a dose of $1\times10^{15}cm^{-2}$ and then annealed at 800℃ in N_2 ambience, the other wafer was not implanted (control).

Enclosed gates (Fig.1) are employed in the tested devices on both hardened and control samples. Transistors with gate-enclosed layout can be used in radiation environments to prevent the onset of any leakage current through a radiation induced lateral path under the bird's beak or at the shallow trench corner, they can effectively survive such failure mechanisms as the increase of drain-to-source leakage current due to turn-on of parasitic transistors[5]. The gate oxide thickness is 41nm, the gate length is 3μm and the aspect ratio *W*/*L* is 60:3 (calculated according to the method presented in Ref. [5]). LOCOS (Local Oxydation of Silicon) is used to enforce the trench, prevent any interaction of the gate bias on the buried oxides. The use of external body contact suppresses the floating-body effect and bipolar effect, avoids the appearance of lateral leakage current induced by trapping in isolation oxides and LOCOS, and prevents the drain-source breakdown.

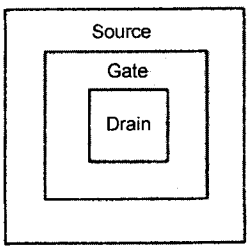

Fig.1 The gate-enclosed layout.

The pre-radiation threshold voltage of front and back gate transistors are given in Table 1.

Table 1 The pre-rad threshold voltage of hardened and control NMOSFET under three bias

	Front gate threshold voltage (V)		Back gate threshold voltage (V)	
	Control	Hardened	Control	Hardened
ON	-0.40	1.60	-1.68	21.1
OFF	-0.22	1.71	-0.25	25.6
PG	-0.25	1.55	-0.85	24.5

Fig.2 shows the equivalent circuit of an SOI NMOS transistor[6]. It consists of a main front channel transistor with top gate, a bipolar transistor with the body being the base (floating or grounded, in our work, it's grounded), and a back channel transistor with back gate. The bipolar transistor is rarely turned on operation at 5V for a 3μm transistor so that the front channel and back channel transistor can be evaluated independently in the partially-depleted SOI transistor structure for V_{DD}=5V.

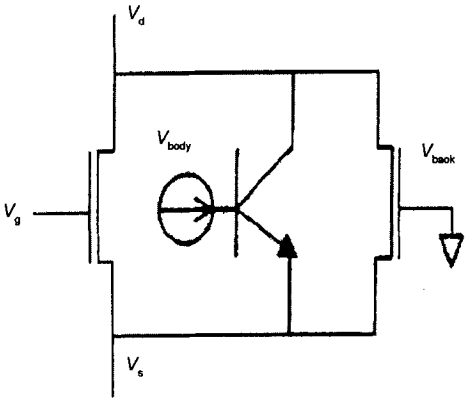

Fig.2 Equivalent circuit of an SOI NMOS transistor (in our device, V_{body}=0V).

Transistors were irradiated with 10keV X-rays generated by ARACOR 4100 Automatic Semiconductor Irradiation System at a dose rate of 27 krad(SiO_2) /min. Three bias conditions under irradiation are given in Table 2, they are on-state, off-state and PG (pass-gate, or transmission-gate) state. *I-V* characteristics of front and back channel transistors (including hardened transistors and control ones) were measured by HP 4155 Semiconductor Parameter

Analyzer, before and after irradiation. Each measurement was ensured to be taken within 20 min after irradiation at each dose. The total dose radiation effects on the individual transistors were characterized by radiation-induced threshold voltage shifts as a function of total dose up to 1.8 Mrad(SiO_2).

Table 2 Bias conditions under irradiation of the PD NMOS/SOI transistors (the supply voltage V_{DD} is 5V for both hardened and control samples)

	Source	Drain	Gate	Body	Substrate
ON	0V	0V	V_{DD}	0V	0V
OFF	0V	V_{DD}	0V	0V	0V
PG	V_{DD}	V_{DD}	0V	0V	0V

3 Results and discussion

3.1 Back gate characteristics

Back gate I_d-V_g characteristic curves at 0, 90, 180, 540, 900 krad (SiO_2) and 1.8 Mrad(SiO_2) under ON, OFF and PG bias are presented in Figs.3, 4 and 5 respectively. Fig.6 shows the threshold voltage shift of the back gate transistor with three bias conditions after irradiation at 90, 180, 540, 900 krad(SiO_2) and 1.8 Mrad(SiO_2) which were extracted from I_d-V_d characteristics at a drain current I_d=10^{-6}A.

Obviously, the hardened sample has less back-gate threshold voltage shift than the control one at any irradiation dose and bias condition. Table 3 indicates the difference in the back-gate threshold voltage shift between hardened and control transistors under three bias conditions, as a function of irradiation dose. The difference in PG bias was the largest one at high irradiation dose. It demonstrates that silicon implantation can effectively harden the transistors below 1.8 Mrad(SiO_2) irradiation at all bias conditions, and prevent them from failure induced by threshold voltage shift of the back gate transistor.

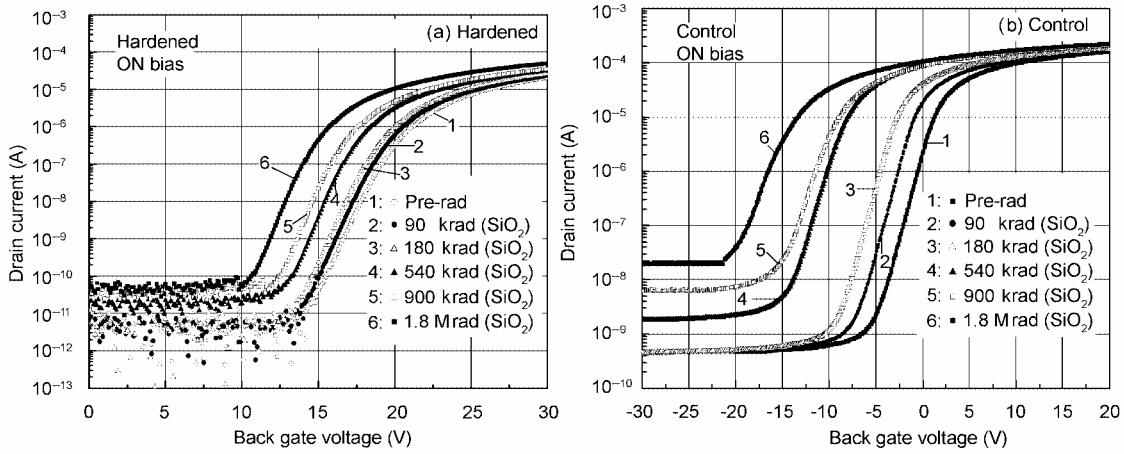

Fig.3 Back gate I_d-V_g characteristic curve at total dose irradiation under ON bias of hardened (a) and control (b) NMOSFET.

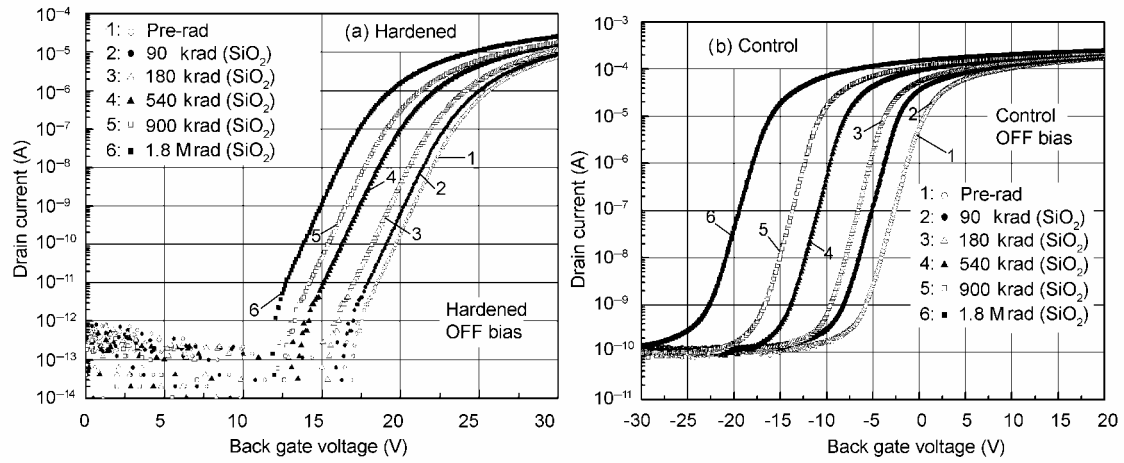

Fig.4 Back gate I_d-V_g characteristic curve at total dose irradiation under OFF bias of hardened (a) and control (b) NMOSFET.

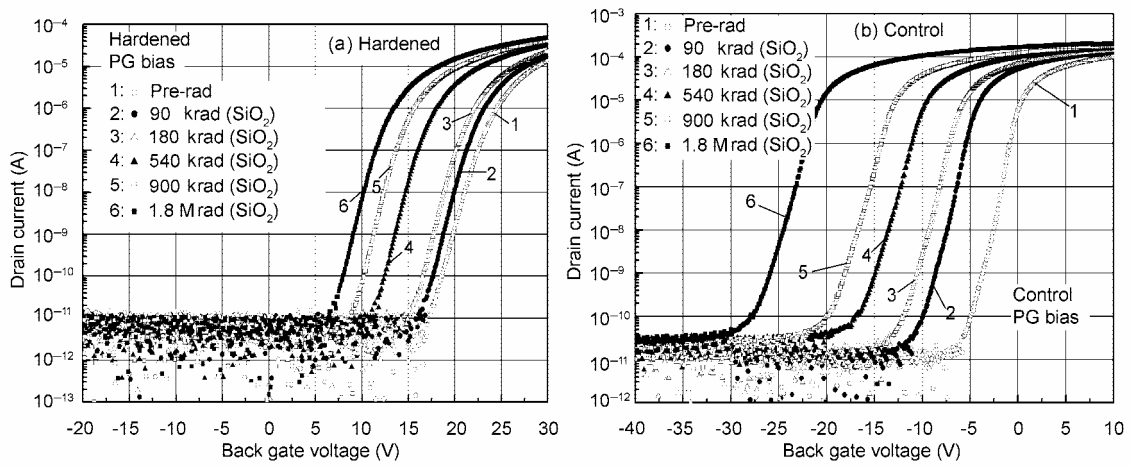

Fig.5 Back gate I_d-V_g characteristic curve at total dose irradiation under PG bias of hardened (a) and control (b) NMOSFET.

It can also be noticed that PG case is the worst case at all irradiation dose. It had been reported[7] that PG is the worst case for the grounded body transistors and OFF is the worst case for the floating body ones. Another research[6] had indicated that the worst-case total dose radiation response of 0.35 μm SOI NMOS body grounded transistors occurs under the pass-gate irradiation bias.

Table 3 The difference in the back-gate threshold voltage shift between hardened and control transistors under three bias conditions, as a function of irradiation dose (V)

Bias	90krad (SiO_2)	180krad (SiO_2)	540krad (SiO_2)	900krad (SiO_2)	1.8Mrad (SiO_2)
ON	1.2	1.8	3.35	3.6	7.55
OFF	2	4.25	4.55	6.7	7.95
PG	3.4	4.0	3.8	4.5	10.2

The edgeless enclosed gate can eliminate the irradiation-induced leakage current as we can see from Figs.3—5 that the drain-to-source current in subthreshold region does not increase significantly after irradiation, especially for the hardened transistors. Concerning the saturation leakage current pre- and post-irradiation (as seen in Figs.3—5), the hardened transistor (OFF and PG biased) is about 10^{-4}—10^{-5} A, and the control one (OFF and PG biased) is about 10^{-3}—10^{-4} A. It demonstrates that one order-of- magnitude reduction in leakage current is due to ion-implantation hardening.

The curves in Fig.6 have been fitted to a recently proposed model[6] describing the back n-channel threshold voltage shift induced by radiation:

$$\Delta V_{\rm th} = -\frac{qN_{\rm ot}}{\kappa\varepsilon_0} t_{\rm BOX}[1-\exp(-\alpha t_{\rm BOX}\frac{\rho D}{\omega N_{\rm ot}})] \qquad (1)$$

where D is the total dose in rad, ρ/ω= 7.6×10^{12} pairs/rad, κ=3.9, ε_0=8.85×10^{-14}F/cm, $t_{\rm BOX}$ is the buried oxide thickness (in this paper, $t_{\rm BOX}$=380nm), $N_{\rm ot}$ is a saturated net positive charge density, and α is the fraction of hole capture. Note that the value of $N_{\rm ot}$ depends on irradiation bias. The net positive charge of the buried oxide at any total dose can be calculated from Eq.(1) as:

$$\Delta Q = -qN_{\rm ot}t_{\rm BOX}[1-\exp(-\alpha t_{\rm BOX}\frac{\rho D}{\omega N_{\rm ot}})] \qquad (2)$$

The values of $N_{\rm ot}$ and α calculated by Origin 7.0 during the fitting of Fig.6 are given in Table 4 below. It is clearly demonstrated that the hardened transistors have smaller saturated net positive charge density $N_{\rm ot}$

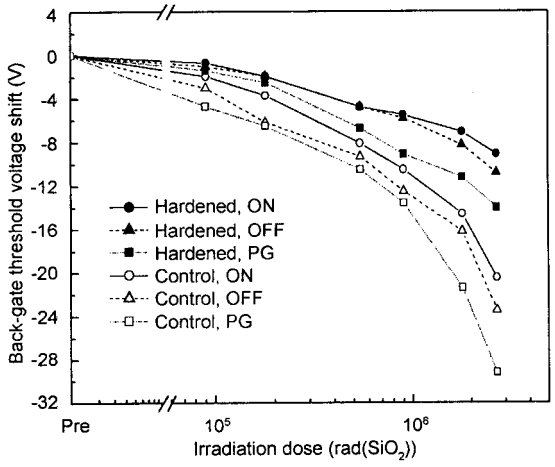

Fig.6 Back-gate threshold voltage shift as a function of total dose for a 3μm gate length NMOS/SOI processed on standard SIMOX with enclosed gate and external body contacts.

and the fraction of hole capture α than their control counterpart for all three bias conditions. The reductions of N_{ot} and α values are definitely attributed to silicon implantation to the BOX and the following annealing. Moreover, PG case has the largest N_{ot} and α values among three bias conditions.

Table 4 The calculated values of N_{ot} and α during the fitting of Fig.6

	ON, hardened	ON, control	OFF, hardened	OFF, control	PG, hardened	PG, control
$N_{ot}(cm^{-3})$	5.04×10^{11}	1.31×10^{12}	6.53×10^{11}	1.34×10^{12}	8.03×10^{11}	1.98×10^{12}
α	3.45×10^{-3}	5.58×10^{-3}	3.31×10^{-3}	6.98×10^{-3}	5.39×10^{-3}	7.43×10^{-3}

3.2 Top gate characteristics

The threshold voltage shift and leakage current of top gate are discussed in the following.

As given in Table 5, at all irradiation dose, the ON case induces the largest top gate threshold voltage shift (extracted from I_d-V_d characteristics at a drain current $I_d=10^{-6}$A) while the PG induces the smallest. The ON case is obviously the worst bias condition for front channel transistor. For example, the top gate threshold voltage shifts of hardened samples at ON, OFF and PG bias are –1.28, –0.22 and –0.15V respectively at 1.8 Mrad (SiO_2). Top gate I_d-V_g characteristic curves at 0, 90, 180, 540, 900 krad (SiO_2) and 1.8 Mrad(SiO_2) under ON bias are particularly presented in Fig.7.

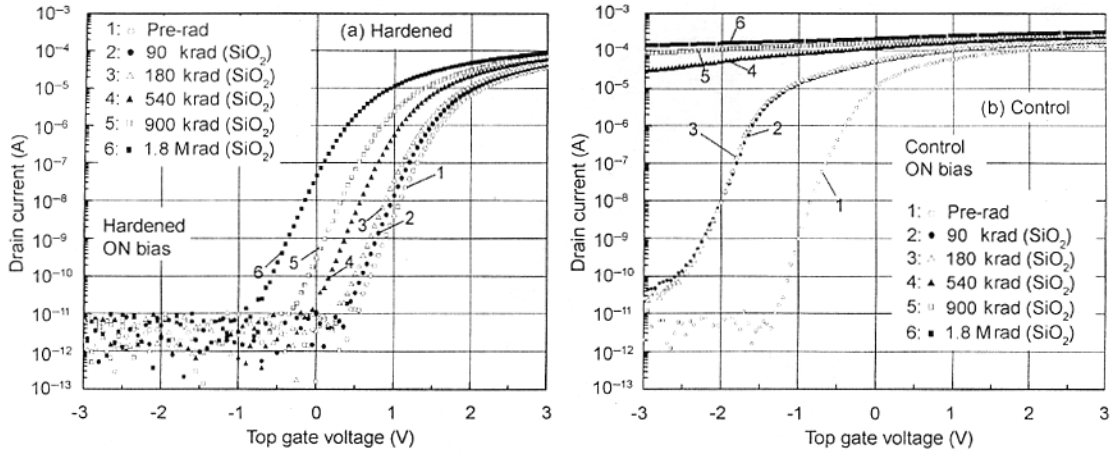

Fig.7 Top gate I_d-V_g characteristic curves at total dose irradiation under ON bias of hardened (a) and control (b) NMOSFET.

Table 5 The top gate threshold voltage shift (V) at various irradiation doses and bias conditions for both hardened and control samples

	90krad (SiO_2)	180krad (SiO_2)	540krad (SiO_2)	900krad (SiO_2)	1.8Mrad (SiO_2)
ON, hardened	–0.2	–0.6	–1.2	–1.25	–1.28
ON, control	0	–2.1	>–3	>–4	>–5
OFF, hardened	–0.05	–0.1	–0.13	–0.19	–0.22
OFF, control	–0.53	–0.73	>–3	>–4	>–5
PG, hardened	0	–0.05	–0.14	–0.17	–0.15
PG, control	–0.3	–1.2	>–3	>–4	>–5

Comparing Fig.7 (a) with Fig.7 (b), the leakage current for hardened transistors in sub-threshold region does not increase apparently, while for control ones, it rapidly increases surpassing over the 10^{-6}A horizontal line, when the irradiation dose rises to 540 krad (SiO_2). It shows that for the hardened transistor, the leakage current in field oxide and back channel is limited to have any evident effect on front channel and for the control transistor, the leakage current in field oxide and back channel is large enough to make front channel leakage current rising sharply in sub-threshold region.

3.3 Discussion

Ion implantation of SOI BOX with silicon to high fluence levels has shown to be an effective method for total-dose hardening of SOI devices [3]. One possible mechanism[4] is that silicon ion implantation creates electron traps with large capture cross sections, that, when filled, compensate radiation-induced trapped positive charge in the BOX and reduce the back-gate threshold voltage shift of transistors fabricated on SOI. It could be attributed to the formation of Si nanocrystals in SiO_2 matrix[8]. Its precursor SiO_x nodules increase in size and eventually go to nanocrystal Si as the implant dose increases and/or annealing temperature and/or annealing time increases. Electron and hole trapping by exposition to VUV has demonstrates that the excess Si creates defects that can capture electrons without an increase in the hole trap density. Four possible structural defects introduced by Si^+ implant have ground and excited energy states that lie within the energy gap of amorphous SiO_2.

Another explanation[4] indicates that positive charge trapping is largely due to proton trapping at network sites having large Si-O-Si bond angles, and implant damage creates such proton traps in the bulk of the oxide so that fewer protons are able to reach the interface, where their effect on flat-band voltage shift would be much greater than in the bulk. Photoluminescence research demonstrates the formation of Si cluster after implantation. UV electron injection has shown that the Si cluster can either trap electrons to become negatively charged or photoemit electrons to become positively charged. It also be shown that the trapping of protons at the clusters is responsible for the reduction in both flat-band voltage shift and interface trap formation during hole injection.

4 Conclusion

In this paper, we have investigated the electrical properties of partly-depleted NMOS body-grounded transistors fabricated on SIMOX with enclosed gate during total-dose irradiation. We have shown that the top and back gate threshold voltage shifts for hardened transistor are much less than the control one as experimentally observed. The leakage current for hardened transistor in sub-threshold region does not increase significantly as control transistor does. It proves that silicon implantation is an effective way to harden SIMOX materials and NMOS transistors fabricated on it. We have also confirmed that PG case is the worst bias for both hardened and control NMOS back gate transistors. The possible mechanisms of hardening by silicon implantation are also discussed.

References

1 Schwank J R, Shaneyfelt M R, Dodd P E *et al*. IEEE Transactions of Nuclear Science, 2000, **47**(6): 2175-2182

2 Schwank J R, Fleetwood D M, Xiong H D *et al*. Microelectronic Engineering, 2004, **72**: 362-366

3 Hughes H, McMarr P. US Patent No.5,795,813

4 Mrstik B J, Hughes H L. IEEE Transactions of Nuclear Science, 2003, **50**(6): 1947-1953

5 Giraldo A, Paccagnella A, Minzoni A. Solid-State Electronics, 2000, **44**: 981-989

6 Liu S T, Balster S, Sinha S *et al*. IEEE Transactions of Nuclear Science, 1999, **46**(6): 1817-1823

7 Ferlet-Cavrois V, Colladant T, Paillet P *et al*. IEEE Transactions of Nuclear Science, 2000, **47**(6): 2183-2188

8 Nicklaw C J, Pagey M P, Pantelides ST *et al*. IEEE Transactions of Nuclear Science, 2000, **47**(6): 2269-2275