Event-driven timing system based on MRF cPCI hardware for HLS-II[*]

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Hefei Light Source (HLS)-II is a vacuum ultraviole (VUV) synchrotron light source. A major upgrade of the light source was finished at the end of 2014. The timing system was rebuilt using compact peripheral component interconnect (cPCI) event-driven hardware to meet synchronization requirements of the machine. In the new system, the cPCI event-driven products manufactured by the micro-research finland (MRF) Oy are employed to achieve about 100 output signals with different interfaces. Device supports and drivers developed for common Experimental Physics and Industrial Control System (EPICS) records are used to access the registers on the timing modules. Five cPCI-bus input/output controllers (IOCs) distributed in different areas of the light source host timing modules for various subsystems. The delay resolution of this system is 9.8 ns for most channels and 9 ps for the channels used for triggering the electron gun and the injection kickers. The measured rms jitter of the output signal is less than 27 ps. Using the bucket chooser, this system enables the HLS-II to fill the storage ring with any designated bunch pattern. Benefitting from this upgrade, brightness and performance of the light source are significantly improved.

Keywords: Timing system, Micro-research finland (MRF), Event-driven, Synchrotron light source

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I. INTRODUCTION

The Hefei Light Source (HLS) at National Synchrotron Radiation Laboratory is a second-generation synchrotron radiation light source, which provides radiations from IR to vacuum ultraviolet (VUV) for various user programs. It is comprised of an 800 MeV linac, an 800 MeV storage ring and a transport line connecting the linac and storage ring. From 2010 to 2014, it was upgraded into HLS-II [1–3] with improved brightness. The timing system was rebuilt to meet the synchronization requirements of the machine. It is designed based upon two considerations: 1) all trigger signals are phase-locked with the RF signal of the storage ring to ensure that an electron bunch from the electron gun can be correctly injected into a specified radio frequency (RF) bucket of the storage ring; and 2) the width, delay and other specifications of the output pulses can be independently adjusted. The design specifications of the HLS-II timing system are listed in Table 1.

TABLE 1. Design specification of the HLS-II timing system

Specifications	E-gun, Kicker	Others
Jitter (rms)	≤ 100 ps	—
Delay resolution	10 ps	10 ns
Maximum delay	≥ 1 s	—
Width resolution	20 ns	—
Maximum pulse width	$\geq 60\,\mu$s	—

The HLS-II timing system provides about 100 output signals to trigger accelerator subsystems, including the electron

gun, solid-state amplifiers, modulators, injection septum and kicker power supplies of the storage ring, etc. In addition, it provides RF and revolution frequency clocks for beam diagnostic stations. The clocks are phase-locked with the storage ring RF system to ensure that the diagnostic devices work properly.

In this paper, an overview on the timing system and its hardware integration is given first. The software development, control function realization, and test results of the system performance are then presented.
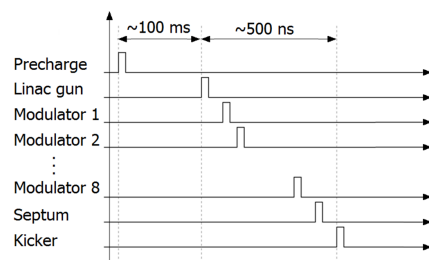

Fig. 1. Timing sequence of the HLS-II. The horizontal axis does not represent the real time scale.

II. SYSTEM OVERVIEW

The HLS-II timing system guides various accelerator components to accelerate and inject electron bunches into designated buckets of the storage ring properly. Figure 1 illustrates the timing sequence of the trigger signals for the accelerator components. The storage ring buckets are defined by the RF system. To inject an electron bunch into a certain bucket, the electron gun is triggered with a proper delay with respect to the RF signal. Then the linac modulators are properly
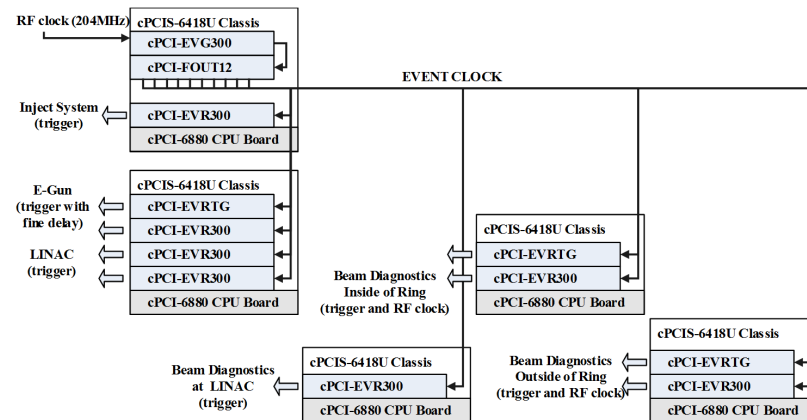
Fig. 2. (Color online) Overview of the HLS-II timing system.

triggered to provide RF power for accelerating the electrons. The injection devices, including the septum and kickers, are energized at the moment when an bunch of electrons arrives, and guide the electrons into the acceptance phase space of the storage ring. The delays of these accelerator units are determined by their locations, and the length of the cable/fibre transferring the timing signals.

As the event-driven timing system developed by the microresearch finland (MRF) Oy is widely used in many accelerator facilities all over the world [4–10], the MRF cPCI-series products were chosen in designing the HLS-II timing system. The software of the HLS-II timing system was developed based upon the Experimental Physics and Industrial Control System (EPICS) [11]. A hardware schematic diagram of the system is shown in Fig. 2. The timing system employs an event generator (EVG) card, cPCI-EVG300 [12], as the master card to generate event codes. The RF signal with a frequency of 204 MHz is used as input signal for the EVG card, and for phased-lock with the RF system. The input signal passes through a divider in the EVG card, and is used as the event clock to generate event codes. The event codes are sent to all event receiver (EVR) cards installed in input/output controllers (IOCs) via a cPCI-FOUT12 fan-out card [13] hosted by the same IOC as the EVG card. Among the EVR cards, cPCI-EVR300 cards are used to generate common trigger signals, while cPCI-EVRTG cards are used to generate trigger signals with fine delay tuning for the electron gun and injection kickers, and to reconstruct the RF and revolution frequency clocks for beam diagnostic stations.

Five IOCs are distributed in different locations to provide trigger signals for nearby systems. Two IOCs are installed in the linac area for the linac related systems. The master IOC holding the cPCI-EVG300 and cPCI-FOUT12 cards is installed beside the RF signal generator of the storage ring. It is also used to provide trigger signal for the injection system. Besides, two IOCs with similar hardware are respectively installed inside and outside of the storage ring, to produce RF and revolution frequency clocks for beam measurement apparatus. Each IOC of the timing system employs a cPCI-6880 CPU board. Compact PCI chassises cPCIS-6418U manufactured by Adlink coporation are adopted to host the CPU board

and MRF timing modules. The IOC software runs under CentOS operating system. All the EPICS drivers, records and operation interfaces are stored in a virtualized server cluster, and shared by timing IOCs through NFS protocol [14].

III. SOFTWARE DEVELOPMENT

A. Device supports and drivers

In EPICS-based control systems, a set of records are used to control and monitor a certain device. These records access the hardware via corresponding device supports and/or drivers. In developing software of the timing system, we used well developed records in the EPICS package, including ai, ao, bi, bo, mbbi and mbbo. Device supports were developed for the records to send/fetch data to/from the timing modules, and drivers were developed for interfacing the device supports and timing modules.

The scheme proposed by Eric Björklund [15] is used for developing drivers of the timing modules. The driver software is developed in a modular structure for high flexibility and extensibility. For example, the driver module *EVG_initialize*(*hdl*,"*evg_dev_name*") and *EVR_initialize*(*hdl*,"*evr_dev_name*") is used to initialize EVG and EVR cards installed in an IOC, respectively, with *hdl* being the handle used for accessing the card by the drviers. The initialization procedures are configured in the start-up script *st.cmd* of each IOC and called during IOC booting up. Other driver modules can be called by device supports with particular arguments to control the parameters of each channel, such as the pulse delay, pulse width, enable switch, polarity switch and trigger event, etc.

The EPICS system selects an appropriate device support for a record according to the record's DTYP field. The DTYP field currently has two options, "MRF EVG" and "MRF EVR" for EVG and EVR cards, respectively.
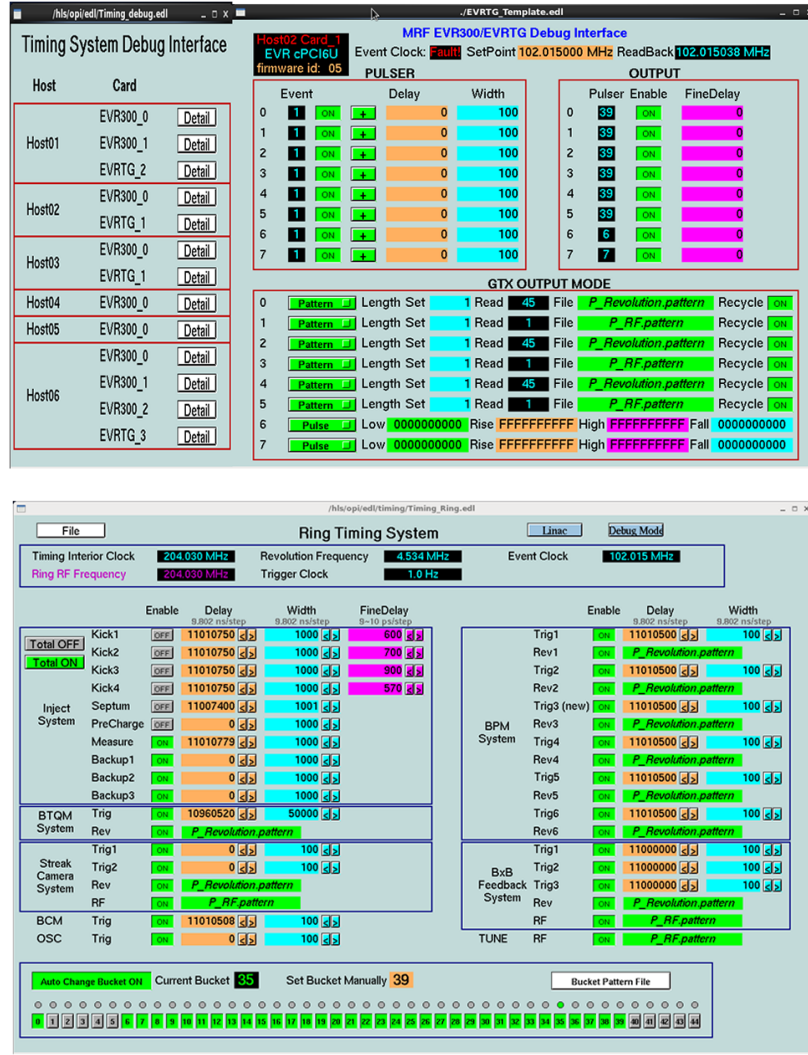
Fig. 3. (Color online) Debug (up) and operational (down) interfaces of the HLS-II timing system.

B. Records for the timing system

In the timing system, two groups of records are used to fulfil different tasks. The first group of records are hardware oriented and used to directly control the timing modules. The other group of records are used to realize various control functions of the timing system.

The hardware oriented records are named using the convention given by *IOC:Card:Chan:Func*. Each of the records is used to control and/or monitor the property *Func* of a channel *Chan* on a timing module *Card* installed in *IOC*. Properties of each channel are controlled by registers on the timing module. The hardware oriented records directly write/read corresponding registers via device driver. The value of field INP/OUT of a read/write record gives the address of the register. Both INP and OUT use the VME address convention, which is expressed as "*#CxSy@para*". In this convention, x and y represent the card and channel numbers, respectively. The optional string in $para$ is used to specify the to-be-

controlled property of the channel, such as delay, width and polarity of the output pulse. Because of the large number of these types of records, we use templates to manage the records. However, the EPICS command *dbLoadTemplate* is inconvenient to be called with arguments. To solve this problem, we develop a number of EPICS commands, such as *dbLoadEVR300* and *dbLoadEVRTG*, to load the record templates during IOC starting up. The arguments are passed to the template loading commands using environment variables as following:

epicsEnvSet("MRF_HOST","Host06")

epicsEnvSet("MRF_CARD","0")

< ${TOP}/iocBoot/${IOC}/dbLoadEVR300

epicsEnvSet("MRF_CARD","1")

< ${TOP}/iocBoot/${IOC}/dbLoadEVR300

epicsEnvSet("MRF_CARD","2")

< ${TOP}/iocBoot/${IOC}/dbLoadEVR300

epicsEnvSet("MRF_CARD","3")

< ${TOP}/iocBoot/${IOC}/dbLoadEVRTG_${MRF_HOST}

For realizing complicated control functions, a set of function oriented records are employed. These records use a different name convention given by *Machine_Device:Function:RecordType*, where *Machine* can be *SR* or *IJ*, representing the storage ring and injector, respectively. *Device* is the subsystem which uses the timing signal, such as the injection kickers, the solid state amplifiers of the linac microwave system, etc. *Function* can be delay, width, switch or other properties of a synchronization pulse. *RecordType* denotes the record type in use, which can be *ai*, *ao*, *bi*, *bo*, etc. The input or output links of these records point to corresponding hardware oriented records.

C.   User Interface

Operator interfaces of the timing system are developed using the Extensible Display Manager (EDM) [16]. According to different purposes, the interfaces are divided into two groups. One is for hardware related records referred as the debug interfaces. This type of interface is used for troubleshooting failures. The other is device-oriented interface used for routine operations. Examples of debug and operation interfaces are shown in Fig. 3.

IV.   BUCKET-BY-BUCKET INJECTION

Bucket-by-bucket injection is essential for stable operation and critical for user programs. To realize this injection scheme, the HLS-II timing system is configured as shown in Fig. 4 to provide synchronization signals with proper delays for various systems. As the timing modules only work with a frequency low than $125\,\mathrm{MHz}$, a frequency divider is used to acquire a $102\,\mathrm{MHz}$ signal from the $204\,\mathrm{MHz}$ input signal. This $102\,\mathrm{MHz}$ signal is used as the clock signals for the delay modules, and used as the input signal of a counter to produce the $1\,\mathrm{Hz}$ injection signal for the bucket chooser which is actually a delay unit. Both the frequency divider and counter are inhabited in the EVG card. The clock and injection signals are also used by various beam diagnostic apparatus to synchronize their measurements. Using pre-programed delays, the bucket chooser produces signals to trigger the electron gun, linac power source system, and the storage ring injection system to aim the electron beam at a designated bucket.
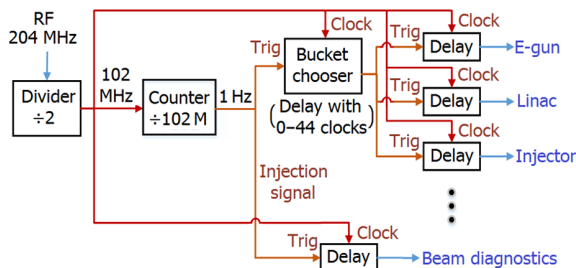

Fig. 4. (Color online) A functional diagram of the timing system.

Since the bucket chooser uses a $102\,\mathrm{MHz}$ signal as its clock, while the storage ring RF signal is $204\,\mathrm{MHz}$, the delay time between two ticks of the bucket chooser equals to 2 bucket length, i.e. the bucket chooser can aim an electron bunch just at every other bucket. However, the harmonic number of the HLS-II storage ring is 45, the bucket-by-bucket injection can be accomplished using proper bucket chooser delays. The number of delay ticks for the nth bucket is given by

$$t_n = n/2, (n = 0, 2, 4, \ldots, 44);$$
$$t_n = 22 + (n + 1)/2, (n = 1, 3, 5, \ldots, 43). \tag{1}$$

This delay arrangement is illustrated in Fig. 5. Each bucket can be enabled/disabled to be filled as shown in the lower part of Fig. 3. The enabled buckets can be automatically iterated or changed manually during injection.
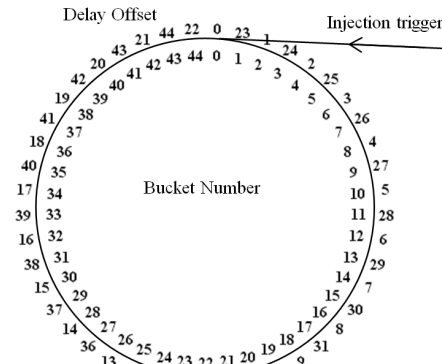

Fig. 5. Bucket-by-bucket injection delay arrangement.

V.   SYSTEM PERFORMANCE TEST

An offline platform (Fig. 6) was setup to test the performance of the timing system. An EVR or EVRTG output signal is connected to a Tektronix DPO5204 oscilloscope, which

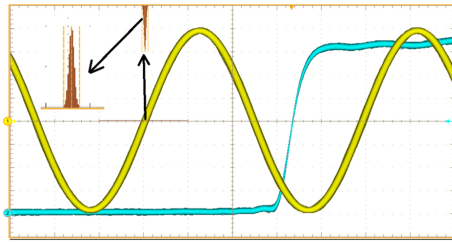Fig. 6. (Color online) Offline test platform of the timing system.

Fig. 7. (Color online) Relative jittering between the EVR output and RF signal.

TABLE 2. Jitter of the timing system in three 24 h-measurements.

Measurements	Pk-to-Pk (ps)	STD (ps)
#1	180.0	26.8
#2	160.0	20.8
#3	180.0	23.0

has a 2 GHz bandwidth and up to 10 GHz sampling rate. The RF signal is connected to another input channel of the oscilloscope. The delay resolution and stability of the timing signal are measured using the test platform. The EVR/EVRTG delay resolution is measured by varying the delay time of an output channel while using the RF signal as the trigger for the oscilloscope. The result shows that the delay resolution of the EVR is 9.8 ns, and the EVRTG is 9 ps. The stability is measured by taking the statistics of the zero voltage posi-

tion of the RF signal while using the EVR output signal as the oscilloscope's trigger, as shown in Fig. 7.

Three measurements were performed consecutively, with the duration of each measurement being about 24 hours. The results show that the relative jittering between the EVR output and the RF signal is close to a normal distribution, with a jitter width of less than 27 ps, and the maximum peak-to-peak value of about 180 ps, as shown in Table 2. These indicate that performance of the timing system meets the design specification. The timing system has performed nicely during one and half years of commissioning and operation of HLS-II.

VI.   CONCLUSION

The HLS-II timing system is developed using the cPCI event-driven products manufactured by the MRF Oy. Common records in the EPICS package are used to realize control functions of the timing system. To effectively control the timing modules, device supports and drivers are developed to manipulate various parameters of the timing modules. The operation interfaces are developed using EDM to fulfil different purposes.

The timing system is capable of bucket-by-bucket injection. By setting a proper delay to the bucket chooser, the storage ring can be filled with any designated bunch pattern. Offline tests and one and half years of commissioning and operation indicate that the timing system meets the requirement of the light source operation.

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