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Experimental study of temperature dependence of single-event upset in SRAMs

Li Cai[1] · Gang Guo[1] · Jian-Cheng Liu[1] · Hui Fan[1] · Shu-Ting Shi[1] · Hui Wang[1] · Gui-Liang Wang[1] · Dong-Jun Shen[1] · Ning HUI[1] · An-Lin He[1]

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Abstract We report on the temperature dependence of single-event upsets in the 215–353 K range in a 4M commercial SRAM manufactured in a 0.15-μm CMOS process, utilizing thin film transistors. The experimental results show that temperature influences the SEU cross section on the rising portion of the cross-sectional curve (such as the chlorine ion incident). SEU cross section increases 257 % when the temperature increases from 215 to 353 K. One of the possible reasons for this is that it is due to the variation in upset voltage induced by changing temperature.

Keywords Cryogenic · Elevated temperature · Heavy ion · Single-event effects · Single-event upset

1 Introduction

There are a lot of energetic particles in the space environments. The single-event effects (SEE) are initiated by a single particle, and interaction with this individual particle can produce many different results in electronic circuits. These results can have different outcomes. Some are nondestructive [e.g., single-event upset (SEU) and single-event transient (SET)], while others can result in permanent damage to electrical devices [such as single-event latchup (SEL) and single-event burnout (SEB)]. Ground-based SEE testing of microelectronic circuits is necessary in order to understand these effects, and the obtained results are used to determine the appropriateness of using such a circuit in a space system either by accepting the consequence of the errors or by mitigating the errors. So far, most of the ground-based SEE tests were carried out at room temperature, but there exists extreme temperature conditions in the space environment. For example, when sunlight hits the moon's surface, the temperature can reach up to 400 K, while the dark side of the moon can have temperatures dipping to 90 K. Therefore, many space missions, such as lunar exploration, are faced with challenges brought by extreme temperatures. It is well known that parameters, which control the electrical behavior of the devices (drift, diffusion, bipolar effects, etc.), are strong functions of operating temperature. As a consequence, we can presume that the SEE response of electronic devices may vary in such a wide temperature range. In this case, we may miss some vital important experimental results if SEE experiments are carried out only at room temperature.

It has been shown that single-event effects (SEU, SEL) are temperature-dependent for some devices [1, 2]. Experiments performed by Copper et al. [3] on Schottky transistor–transistor logic (TTL) devices have shown that susceptibility to latchup may increase with temperature. Johnston et al. [4] reported that the SEL threshold linear energy transfer (LET) of SRAM decreases when the temperature increases, and SEL saturation cross section increases with rising temperature. It also has been demonstrated that the SEU sensitivity increases when the temperature increases for a NMOS-resistant load SRAM [5]. Truyen et al. [6] also studied the temperature dependence of a SEU in an ATMEL 0.18-μm SRAM memory cell, but the results indicate that the SEU sensitivity depends weakly on temperature with a parabolic shape. Recently, both heavy ion experiments and technology computer-aided design (TCAD) simulations show that SET pulse width increases significantly with temperature [7–11].

✉ Gang Guo
ggg@ciae.ac.cn

[1] China Institute of Atomic Energy, Beijing 102413, China

Liu et al. [12] had investigated the temperature dependency of charge sharing in a 130-nm complementary metal oxide semiconductor (CMOS) technology using a TCAD simulation tool. The simulation results show the charge sharing collection increases significantly as temperature rises. From these published experimental and simulation results, it can be seen that the research on the impact of temperature on SEE is continuously developing. Some results show that the influence of temperature on SEE is significant, but others indicate that the temperature dependence of SEE may be ignored.

In this paper, SEU cross sections are measured in the 215–353 K temperature range on a commercial 0.15-μm static random access memory (SRAM), using a sample temperature control and measurement system based on the Beijing HI-13 tandem accelerator SEE test facility. The temperature dependence of the SEU cross section is evaluated. Experimental results will be discussed, and a possible explanation for the test results will be suggested.

2 Experimental description

The device under test (DUT) used in this work is a 4Mbit commercial SRAM fabricated in using the 0.15-μm CMOS process with thin film transistors (TFT). The core SRAM cell is a six-transistor cell with a supply voltage ranging from 2.7 to 3.6 V. Heavy ion experiments were carried out at the Beijing HI-13 tandem accelerator SEE text facility.

Usually, five species of heavy ions are used to irradiate the DUT to get the complete SEU cross-sectional curve, but due to time constraints, we could only select three species of heavy ions (F, Cl, and Cu ions) to depict the trend of the cross-sectional curve. According to the experimental data published in Refs. [13, 14], we found that although the new technology is used in this device, effectively eliminating SEL, it is still very susceptible to SEU, and when compared to a 16M SRAM, which have a similar feature size and structure, SEU was found to occur even when the LET value is as low as 1.73 MeV-cm^2/mg [13]. From Ref. [13], we found that for such large-capacity and small-sized devices, it is usually difficult to measure its saturation cross section, as multiple-bit upset normally occurs. The ion species chosen for the current work and their characteristics are listed in Table 1.

The devices were de-capped prior to the irradiation tests. All tests were performed under normal incidence, writing 1010 into SRAM. No SEL event occurred during these heavy ion tests. In order to obtain high statistical confidence, tests were carried out until at least 100 upsets occured or to a fluence of 10^7 ions/cm^2 for each device. The device was tested two or three times under the same conditions to get the mean value of the SEU cross section.

Heavy ion experiments were carried out at both elevated and cryogenic temperatures. During the elevated temperature test, the device on the test board was heated by a semiconductor heater attached to the back of the chip, and the temperature of the chip's surface was measured and controlled by an infrared radiation thermometer. For the cryogenic test, the device was cooled down by thermal contact with a copper plate to which a liquid nitrogen cavity has been attached, and the temperature measurements were read using a silicon diode sensor mounted on the copper plate. Because the chip is very small, it is too difficult to attach a temperature sensor to the package of the DUT; therefore, we use the temperature measured by the sensor mounted on the copper plate as a representative of the temperature of DUT. Before starting the irradiation experiment, we used two silicon diode sensors to test the temperature difference between the copper plate and the chip's surface. Sensor A was attached to the copper plate, and this sensor was used to control the system temperature. Sensor B was attached to the naked surface of the DUT. The temperature difference between sensor A and sensor B was less than 3 K over the temperature range, down to 180 K. As can be seen from the SEE test results, which will be shown in part 3, the influence caused by this temperature difference is negligible. With the feedback system via the sensors and the PID controller, the system temperature can be maintained to ±1 K of the desired values. More details about this experimental setup will be presented in another paper. The sample temperature measurement and the control system schematics are shown in Fig. 1.

3 Experimental results

As depicted in Fig. 2, the SEU cross section is plotted as a function of LET for the four investigated temperatures. It appears that the temperature dependence of the SEU cross section is not very significant, but we still can see that when a chlorine ion is present, the SEU cross section increases as temperature increases. The SEU cross section increased by 16, 32, and 67 % when the temperature increases from room temperature (300 K) to 318, 333, and 353 K, respectively.

According to the elevated temperature experimental results, the trend of the temperature dependence of the SEU cross section is most obvious when a chlorine ion is present on the DUT. The cryogenic temperature experiment was performed using chlorine ion incidence, and the experimental results are shown in Fig. 3. It shows the influence of temperature on the SEU cross section. We can see that the SEU cross section increases with rising temperature, and the variation in cross section is not induced by error. Cross section increases almost 257 % (from 1.21×10^{-3} to 4.32×10^{-3} cm^2/device) when temperature increases from 215 to 353 K.

Table 1 Parameters of heavy ions used in tests

Ion species	Energy (MeV)	LET (MeV-cm^2/mg)	Range in silicon (μm)
F	110	4.2	82.7
Cl	157	13.2	45.1
Cu	200	32.5	34.5

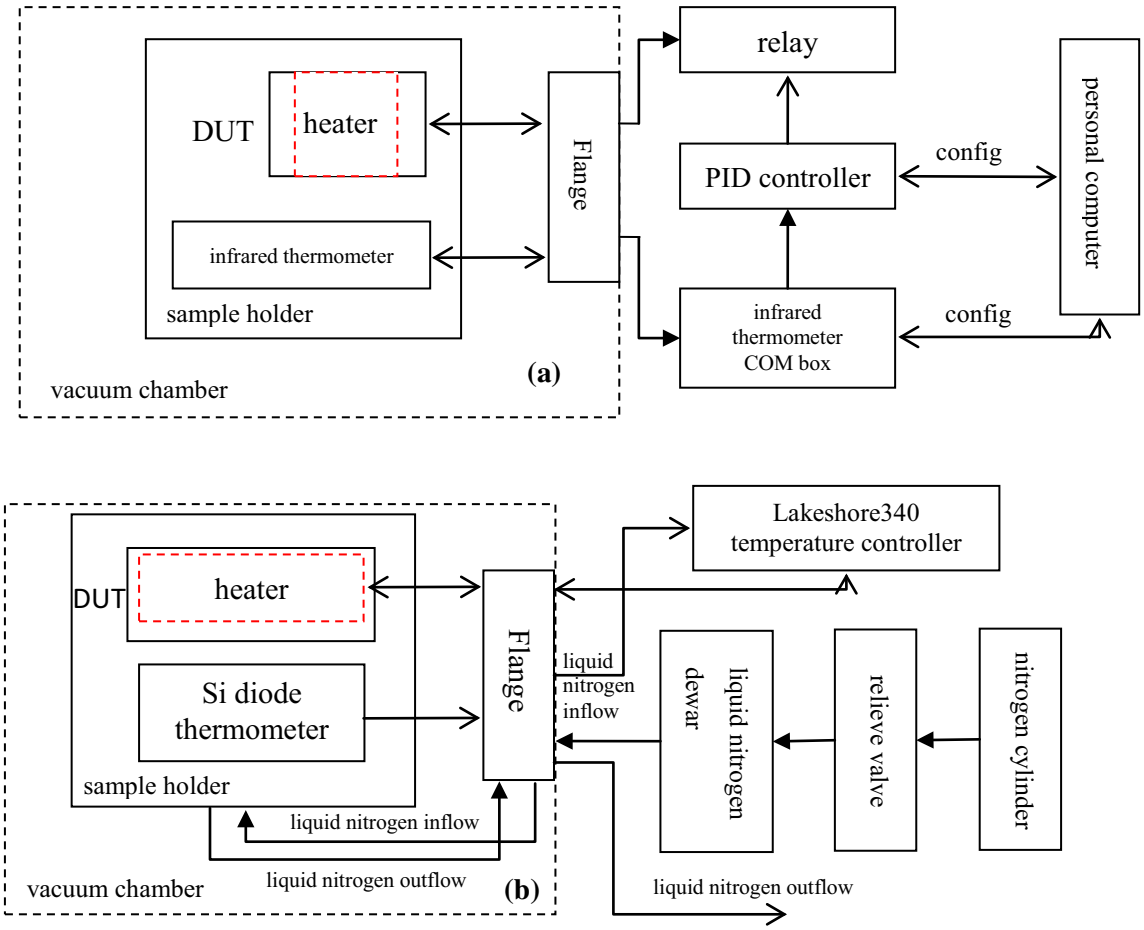

Fig. 1 (Color online) Sample temperature measurement and control system schematics: **a** block diagram of 300–450 K DUT temperature measurement and control system. **b** Block diagram of 90–300 K DUT temperature measurement and control system

4 Discussion

As shown in Fig. 2, on the rising portions of the cross-sectional curves (e.g., around 13 MeV-cm^2/mg for chlorine ion incidence), the SEU cross section obviously increases with temperature, but on the saturation portion of the curve (around 32 MeV-cm^2/mg for copper ion incidence), the SEU cross section almost does not change with temperature; no obvious trend can be observed.

Because the structure of this SRAM is TFT structure, this structure does not have bulk bias, which is similar to the fully depleted SOI device; thus, the effect of bipolar amplification is not considered here [15]. The influence of temperature on the SEU cross section is attributed to a combination of both (a) the temperature effect on SET pulse, and (b) the temperature effect on the electrical characteristics of SRAM.

4.1 Temperature influence on SET

When a heavy ion strikes the most sensitive volume of the memory cell (typically in the "off-state," i.e., during the reverse-biased drain/substrate junction), the charge collected by the junction results in a transient current in the struck transistor. This transient current in a memory cell may or may not produce a SEU, depending on the amount of deposited charge and its time history. Both the transient current peak value and the pulse width are influenced by

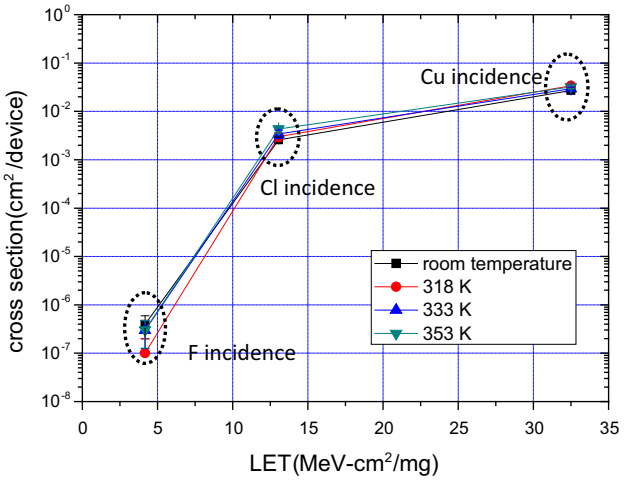

Fig. 2 (Color online) SRAM SEU cross section versus LET for various temperatures above room temperature

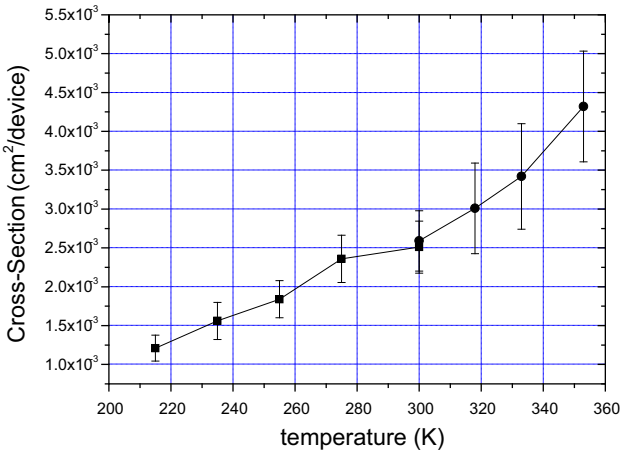

Fig. 3 (Color online) SRAM SEU cross section at different temperatures for 157 MeV Cl ion incidence

temperature. As reported previously [3, 7–11], the transient current peak value decreases as temperature increases, as the pulse width increases with temperature rising. Single-event error rates for microcircuits are a strong function of SET pulse width [16, 17]. Drift, diffusion, and bipolar amplification are the three temperature-dependent factors which affect the ion-induced charge collection in semiconductor devices. The drift component of SET pulse width is typically very short (usual tens of picoseconds), compared to a SET lasting time (hundreds of picoseconds). Its variation with temperature does not impact the SET pulse width significantly. In previous works, it is known that the net effect of temperature's influence on the diffusion current induced by a heavy ion incidence is considered to be small [8], while the increase in bipolar amplification with temperature is a main contributor to the increase in SET pulse width [10]. As stated earlier, for the TFT structure in our study, the bipolar amplification is not taken into account; therefore, the effect of temperature on SET pulse width may not be significant. As a result, the temperature dependence of transient current will not be considered for SEU cross-sectional variation with temperature.

4.2 Temperature influence on the electrical characteristics

It is well known that temperature induces a change in the electrical characteristics of the device. In response to the heavy-ion-induced single-event current transient, there is a voltage transient, which is actually the mechanism that can cause upset in SRAMs. Truyen et al. [6] investigated the DC voltage characteristics for 218, 300, and 418 K temperatures and found that the upset voltage decreases when the temperature increases. According to Ref. [6], there is a linear variation between the upset voltage and the temperature, which can be described using the following equation:

$$V_{\text{upset}}(T) = kT + V_{\text{upset0}}, \quad (1)$$

where T is the device temperature, $k = \mathrm{d}V/\mathrm{d}T$, and V_{upset0} depends on the electrical characteristics of the circuit itself. In Ref. [6], the variation between the upset voltage and the temperature is equal to −0.2 mV/K. The critical charge can be estimated using the following equation:

$$Q_{\text{crit}} = C_{\text{g}} V_{\text{upset}}, \quad (2)$$

where C_{g} is the gate capacitance.

It is very difficult to know the exact value of the gate area and the effective oxide thickness of our device. We estimate the gate capacitance by extracting the area of the gate from the SPICE model and utilizing the effective oxide thickness obtained from the 0.15-μm standard process. The gate capacitance is determined to be ∼1 fF. Utilizing the variation between the upset voltage and the temperature from Ref. [1], the variation between the critical charge and the temperature is equal to -0.2×10^{-3} fC/K. When temperature increases from 215 to 353 K, the critical charge decreased by about 0.0276 fC, which is a relatively small value. However, as the feature size of commercial SRAM has shrunk dramatically, the critical charge for upset has been significantly reduced. For example, according to Ref. [6], the SRAM fabricated in the 0.18-μm process has a critical charge value of about 1 fC. For a device with a smaller feature size, the critical charge will be smaller. Therefore, although the variation in the critical charge induced by temperature is relatively small, it can still lead to the change in cross section.

Following the above discussion, the temperature influence on the SEU cross section is mainly induced by temperature's effect on electrical characteristics. The upset voltage decreases with temperature because the electrical

behavior of the SRAM changes with temperature, resulting in a decrease in critical charge. As mentioned in Sect. 4.2, the value of a reduced critical charge is relatively small. Therefore, we conclude that on the rising portion of cross-sectional curve, the LET value of an ion is not high enough, which can lead to the charge being deposited in a sensitivity volume that is not sufficient at a lower temperature, making the temperature effect more obvious. On the saturation portion of the cross section, the LET value of an ion is high enough, so the charge deposited in the sensitive volume is sufficient to cause an upset no matter what the temperature is. Therefore, the temperature dependence of the upset voltage does not obviously influence cross section.

5 Conclusion

In summary, the influence of temperature on the SEU cross section has been investigated in a 4-Mbit 0.15-μm TFT SRAM. We have shown that at the rising portion of the cross-sectional curve, the SEU cross section increases with temperature. The cross section increases almost 257 % when temperature increases from 215 to 353 K for chlorine ion incidence. At the saturation cross-sectional part, the influence of temperature on the SEU cross section can be ignored. This is because at this part, the LET value of the ion is high enough and the charge deposited in the sensitive volume is sufficient to cause an upset at any temperature. As a consequence, the influence of the variation in upset voltage due to temperature on the SEU cross section is negligible.

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