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A multi-channel real-time digital integrator for magnetic diagnostics in HL-2A tokamak

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Abstract A novel full-digital integrator has been developed for the magnetic diagnostics in HL-2A. Based on the pipeline processing of the field-programmable gate array and high-speed PCI extensions for instrumentation platform, the digital integrator has realized octal-channel 10-kHz real-time integration and data transmission. In order to reduce the integration drift, a 24-bit analog-to-digital converter and simple analog processing circuits are applied for high-precision sampling, while certain correction algorithms are used to minimize the drift. With simple and highly integrated circuits and high-performance digital processor, the digital integrator is of high stability and functional expansibility which greatly simplifies the operation procedure. The digital integrator has been tested in the plasma discharge experiments, and the experimental results have confirmed that the drift performance and accuracy of the digital integrator could fully meet the requirements of HL-2A.

Keywords Digital integrator · Field-programmable gate array · Drift compensation · Real time · Magnetic diagnostics

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1 Introduction

Magnetic diagnostics is a fundamental diagnostics that provides key information about plasma displacement and condition of the tokamak devices [1–3]. The sensors of the HL-2A magnetic diagnostic system, such as inductive loops and Rogowski coils, acquire induced voltage signals when integrators are required to convert the voltages to magnetic fluxes or plasma currents [4]. Accuracy of the integrators is of great impact on quality of the diagnostics.

The magnetic diagnostics system for HL-2A monitors over 400 signals in real time during long-pulse plasma discharges, so the integrator shall be accurate and stable, and convenient to control and maintain. The previous integrator system of HL-2A is based on traditional analog integration circuit, of which the major problem is that the input offset of the operational amplifiers would be integrated and cause integration drift [5]. Reducing the drift needs an extra compensation integrator, with its input being connected to the ground to measure the drift while the output being subtracted from that of the main integrator [6]. The integration drift can be reduced through fine adjustment of the RC-time constant of the compensation integrator of each channel. However, the adjustments are excessively repetitive during longtime experiments since the drifts are unstable due to the low-temperature stability of the analog components, and this kind of integrator performed unstably without further drift compensation methods.

Owing to the limitations of analog integration, integrators using digital techniques gain their popularity [7–12]. The principle of digital integration is to convert the analog signals into discrete digital signals by ADCs and accomplish numerical integration using digital processors and integration algorithms. Yet, most digital integrators require complex analog preprocessing for better performance. In this work, we developed a full-digital integrator based on FPGA and PXI platform [13, 14]. Utilizing ADC and FPGA for digital processing, the HL-2A digital integrator module (HL-2A DIM) was designed, and real-time integration and drift compensation were achieved with simple analog circuit and extensional algorithms. The digital integrator system has been applied to the magnetic diagnostics system of HL-2A, with satisfactory experimental results.

2 Design

Development of the HL-2A DIM is aimed at realizing highly integrated digital integration with high performance for the HL-2A magnetic diagnostics. Specific requirements include (1) high-accuracy integration with low drift; (2) high stability and practicability during longtime operation of the multi-channel system; (3) real-time process and display; and (4) necessary auxiliary functions.

A simple method of digital integration is to connect the magnetic sensors directly to the ADC, from which the digital processor receives converted digital data for integration. Normally, such integration is not accurate because of the input offset from the amplifiers and the ADC. With proper design of the circuit board and the algorithms, however, we can minimize the error and achieve high-accuracy integration.

2.1 Hardware

The architecture diagram of the HL-2A DIM is shown in Fig. 1. It mainly consists of two parts: the high-precision ADC with 24-bit resolution plus the front analog processing circuit, and the high-performance FPGA for onboard processing and PXI interface.

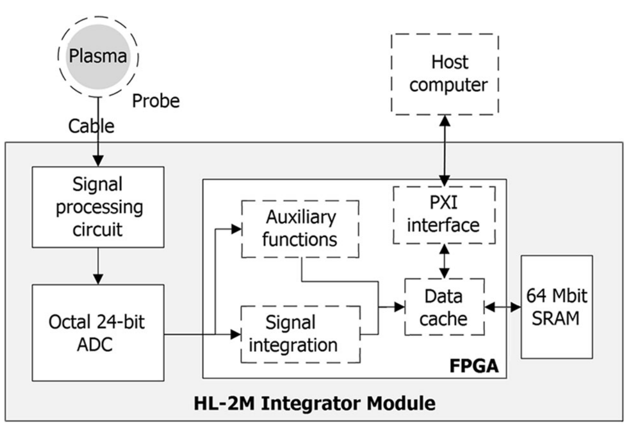

Fig. 1 Architecture diagram of the HL-2A DIM

The magnetic sensors send induced voltages to the HL-2A DIM through cables. The signals are received by the analog processing circuit which drives the ADC while filters the noise and attenuates the signals to extend the dynamic input range. It contains the π-type attenuation, the ADC driving circuit, and the anti-alias filtering. Passive components of high-temperature stability compose the major part of the analog processing circuit. The design ensures that the analog circuit is of high stability and the ADC can work with its best performance.

As a key component of the digital integrator, the ADC affects accuracy of the integrator. So TI ADS1278 is used. It is a fully differential octal-channel 24-bit $\sum$–Δ ADC with sampling rate up to 144 KSPS. Utilizing high-performance digital filters, the ADS1278 is of great DC performance with offset drift down to $0.8\,\mu\mathrm{V}/^{\circ}\mathrm{C}$ and gain drift down to 1.3 $\mathrm{ppm}/^{\circ}\mathrm{C}$. Based on the simple analog driving circuit and the high-performance ADC, the HL-2A DIM has achieved high-precision sampling with low noise.

After reliable digitization, certain algorithms in the Cyclone III FPGA were developed for digital integration and drift compensation. Served as a logic processing unit, the FPGA is programmed to realize digital integration, drift compensation, data transmission interfaces, and auxiliary functions. The integration results from the FPGA are uploaded to the host computer for real-time control and display through the 32-bit PXI backplane bus. An external 64-Mbit SRAM chip is reserved for onboard data cache. The HL-2A DIM is featured by eight single-ended inputs, octal-channel simultaneous sampling at 100 KSPS, and 24-bit resolution. Based on the real-time processing of the FPGA and high-speed PXI backplane bus, real-time integration of 10 kHz per channel can be achieved.

The digital integrator modules are in the form of standard PXI 3U module and installed in the NI PXIe-1085 chassis. The NI PXIe-8135 is a 2.3-GHz, quad-core PXI Express processor as the embedded controller for the operation of PXI platform. It also serves as the host computer of the modules installed in the chassis which stores and displays the real-time waveforms while uploads data to the HL-2A Master Control System (HL-2A MCS) for storage and further analysis through Ethernet network.

2.2 Algorithm

The principle of digital integration is numerical integration which comprises various algorithms for calculating the numerical value of a definite integration. Rectangle integration is a general method. Dividing the entire time interval into a great number of subintervals, one gets the result by adding up the approximate of each subinterval. In the HL-2A DIM, the integration result, S_{FPGA}, is the sum of a sampled datum times the sampling interval Δt.

$$S_{\mathrm{FPGA}} = \int V_{\mathrm{in}} \mathrm{d}t = \sum_{i=0}^{n} V_{\mathrm{in}}[i]\Delta t, \quad (1)$$

where V_{in} is the input signal. But Eq. (1) leads to integration drift due to the input offset, which is expressed as:

$$S_{\mathrm{FPGA}} = \sum_{i=0}^{n} V_{\mathrm{in}}[i]\Delta t = \sum_{i=0}^{n} (V_{\mathrm{sensor}}[i] + V_{\mathrm{offset}}[i])\Delta t, \quad (2)$$

where V_{sensor} is the output of the sensor, and V_{offset} is the input offset. In the magnetic diagnostics of HL-2A, the magnetic sensors are of no complex designs, consisting of simple inductive wires and coils [11]. The sensors themselves do not cause offset, which mainly owes to the integrator circuits. The input offset can be measured since the offset is stable enough to be regarded as a constant in a time period of up to 100 s. The HL-2A DIM measures V_{offset} by starting sampling when the outputs of the sensors are zero and taking average of the sampled data using Eq. (3) (m is the total number of the sampled offset data):

$$V_{\mathrm{offset}} = \frac{1}{m} \sum_{i=0}^{m} V_{\mathrm{in}}[i]. \quad (3)$$

Without any input signals, it can be considered that the sampled data V_{in} equal to V_{offset}. Then, V_{offset} is subtracted from the data sampled during plasma discharge to realize drift compensation. Thus, we have the modified digital integration formula as Eq. (4):

$$S_{\mathrm{FPGA}} = \sum_{i}^{n} (V_{\mathrm{in}}[i] - V_{\mathrm{offset}})\Delta t = \sum_{i}^{n} V_{\mathrm{sensor}}[i]\Delta t. \quad (4)$$

In the HL-2A DIM, the digital integration and drift compensation algorithms are implemented in the FPGA. The sampling rate of the ADC is 100 KSPS, and all the sampled 24-bit data are processed according to Eq. (4) in real time, which is achieved by adopting synchronous parallel pipeline architecture of programming. One of every ten results is uploaded in real time to achieve 10-kHz real-time processing during plasma discharge with the high-speed burst read mode of the PXI bus, which can be expressed as:

$$S_{\mathrm{FPGA}}[i] = \sum_{j=0}^{i\times 10-1} (V_{\mathrm{in}}[j] - V_{\mathrm{offset}})\Delta t, \quad (5)$$

or

$$S_{\mathrm{FPGA}}[i] = S_{\mathrm{FPGA}}[i-1] + \sum_{j=(i-1)\times 10}^{i\times 10-1} (V_{\mathrm{in}}[j] - V_{\mathrm{offset}})\Delta t. \quad (6)$$

2.3 Process

The flowchart of the HL-2A DIM system is shown in Fig. 2. It provides as follows:

(1) Besides digital integration, auxiliary functions are realized by taking advantages of the high-performance and programming flexibility of FPGA, including raw signals display, self-check, and calibration, which is of great convenience to the system maintenance. Specific functions can be selected through the user interface on the host computer based on LabView. For digital integration, the HL-2A MCS or host computer should set basic operation parameters for the integrator, including time division, integration duration, and trigger mode.

In order to start the offset measurement in advance, the HL-2A DIM demands a trigger signal from the HL-2A MCS that arrives earlier than the plasma discharge. The trigger is precisely timed which allows the integrator to

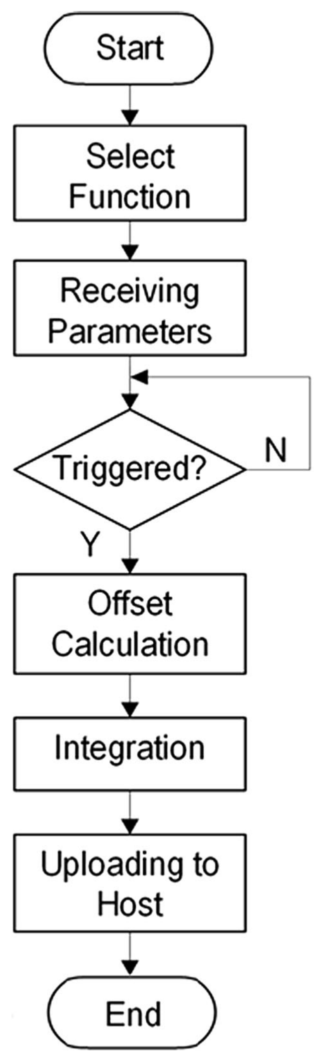

Fig. 2 Flowchart of the HL-2A DIM

start integration at a certain time automatically by setting a proper delay in the FPGA as shown in the sequence diagram of the HL-2A DIM system (Fig. 3). According to practical settings, the offset measurement is started 30 s before the discharge to guarantee that outputs of the magnetic sensors are zero. The offset is premeasured before every experiment; thus, the longtime performance of the HL-2A DIM is highly stable.

(2) After being triggered, the HL-2A DIM starts the offset measurement which lasts 2.5 s. After the delay, the integration begins, and the HL-2A DIM uploads the integration results in real time. As the duration of plasma discharge in HL-2A is less than 10 s, the complete operating time of the HL-2A DIM in one experiment is at most 60 s, during which stability of the offset can be guaranteed. All the above-mentioned time parameters of the HL-2A DIM are user-reconfigurable for practical situations.

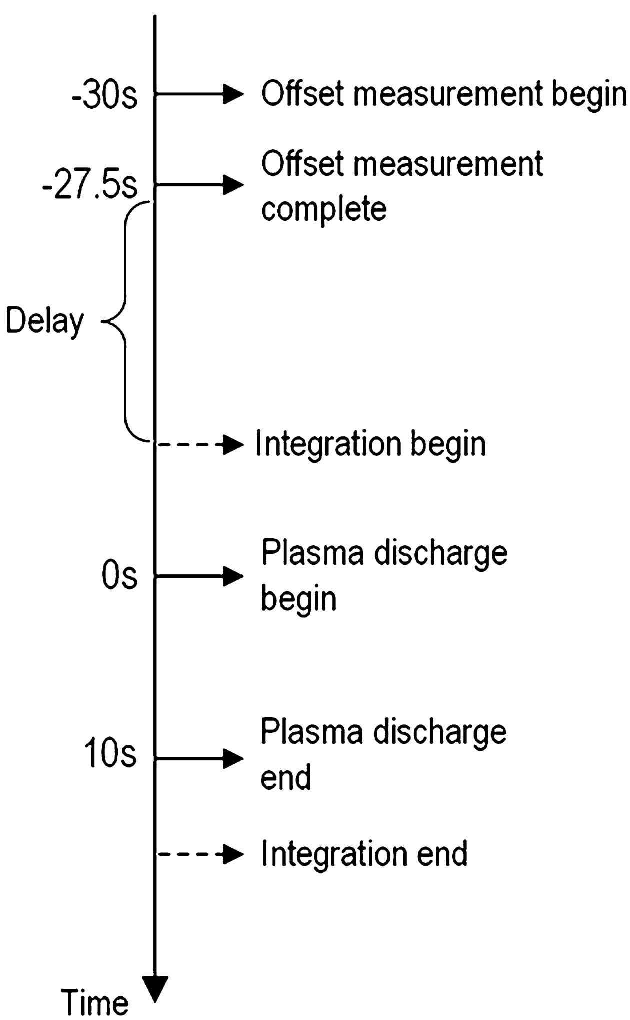

Fig. 3 Sequence diagram of the HL-2A DIM system

3 Performance

In the HL-2A plasma discharge campaign at the Southwestern Institute of Physics, China, in the autumn of 2014, the HL-2A DIM has also been tested in situ. In the experiments, the duration of plasma discharge was about 6 s, and the drift of digital integrator should be better than $50\,\mu\mathrm{Vs/s}$ to meet the demands of present experiments based on the performance of the former integrator system in HL-2A.

3.1 Test experiments

The test experiments were conducted to verify the drift performance of the digital integrators. The HL-2A DIMs were installed in one PXI chassis, and the input connectors were connected to the magnetic sensors with shielded twist-pair cables. Without the plasma, all the sensors were of zero output. Figure 4 shows that drifts of the eight channels of one module were all less than 0.9 mVs in 100 s. Further tests indicate that drift of the HL-2A DIM was $20\,\mu\mathrm{Vs/s}$; thus, drift performance of the digital integrator could fully meet the requirements of HL-2A.

3.2 Application experiments

Several types of signals from different kinds of sensors were applied to test the performance of the digital integrator during plasma discharge. The application experiments were arranged as follows: 30 s before plasma discharge, the HL-2A MCS triggered the offset measurement; 10 s before plasma discharge, the integration started, lasting 40 s to track the real-time integration waveforms in complete plasma discharges. Typical results are as follows.

Saddle loops are inductive wire loops placed around the plasma boundary to determine the plasma displacement [15]. Raw signals from the flux loops are normally of

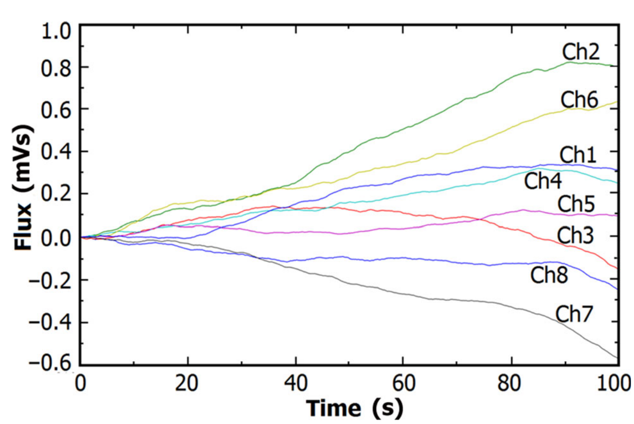

Fig. 4 (Color online) Drifts of eight channels in 100 s

high amplitudes which could reach up to 50 V during plasma disruption. Figure 5 shows the integration waveforms of F_O_d and F_O_u, two saddle loops in contrary directions, in shot 23 323. The total magnetic fluxes detected by the two loops were 3.263 Vs (F_O_d) and 3.365 Vs (F_O_u), which accords well with the results from analog integrators. By measuring the baseline shift before and after plasma discharge, the fluxes caused by the drifts in 20 s are less than 1.8 mVs, which means that the error caused by the drifts is less than $0.0018/3.263 = 0.055$ %.

Poloidal flux loops, or single-turn flux loops, are placed on the toroidal section of the plasma to measure the loop voltages and magnetic fluxes [16]. Signals from the poloidal flux loops are usually weaker than those from the saddle loops. Diag_5_2 is a poloidal flux loop, of which the integration waveform in shot 23 322 is described in Fig. 6a. The drift contributes 0.3–0.5160 Vs flux shift detected in 40 s, and the drift error is less than 0.1 %.

The sensors for plasma current measurement are Rogowski coils placed on the poloidal plane of HL-2A [17]. The plasma current measurement system of HL-2A consists of one main coil and several compensation coils to measure the interferential magnetic fields. Signals from the compensation coils are much weaker after integration and demand highest drift performance of the integrator. The HL-2A DIM has realized longtime integration of the signals from such sensors. Figure 6b shows the real-time integration result of Comp_OH, a compensation coil set to measure the primary current induced by the Ohm field [15]. The drift flux is 0.217 mVs corresponding to the 73.24 mVs total flux shift in 20 s; thus, the drift error is $0.217/73.24 = 0.296$ %.

The results confirm that the digital integrator fits perfectly for the object sensors. In further experiments under multiple conditions, it has maintained its performance without any adjustment or breakdown, while the highly integrated and multi-function integrator modules have

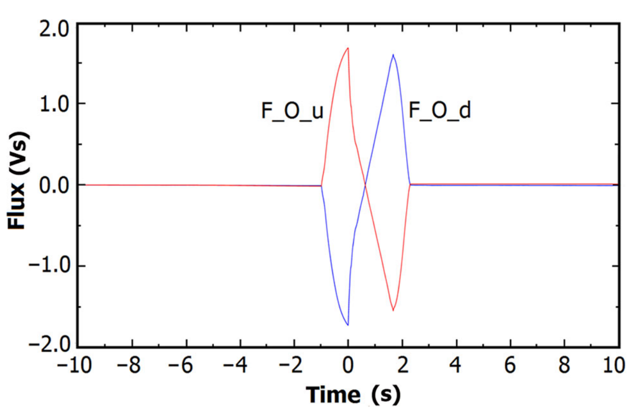

Fig. 5 (Color online) Integration waveforms of F_O_d and F_O_u

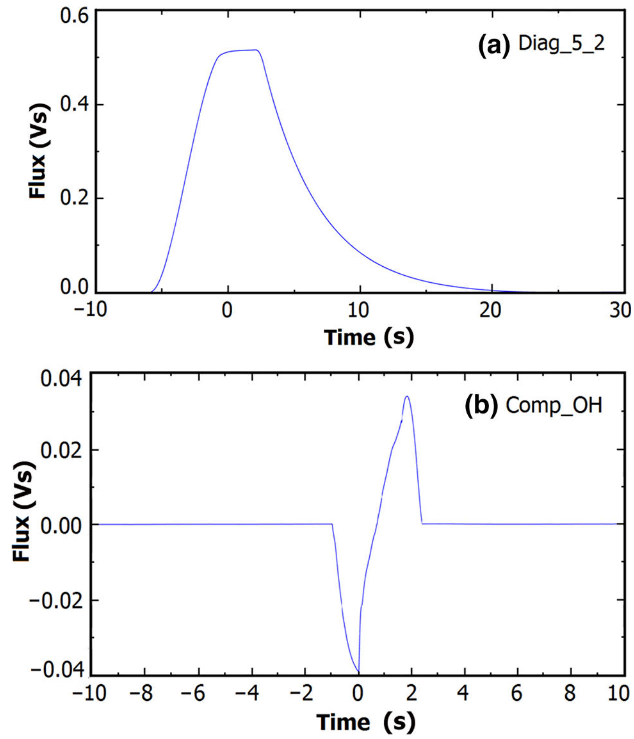

Fig. 6 (Color online) Integration waveform of Diag_5_2 (**a**) and Comp_OH (**b**)

greatly simplified the integrator device and the experiment procedures. The performance and practicability proved that the HL-2A DIM system could meet the demands of present plasma discharge experiments in HL-2A.

4 Conclusion

The HL-2A DIM full-digital integrator has achieved real-time integration of high accuracy along with necessary auxiliary functions based on high-performance ADC and FPGA-based algorithms. It was tested by different types of signals in the HL-2A plasma discharge experiments, and its performances are measured. Integration drift of the digital integrator is just $20\,\mu\text{Vs/s}$, while it was $50\,\mu\text{Vs/s}$ with the analog integrator.

The drift performance of HL-2A DIM is adequate for current HL-2A experiments with discharge duration of less than 10 s. However, as reported recently [8–10], it is close to $0.07\,\mu\text{Vs/s}$ with integrators applied for longtime discharge of more than 1000 s. Also, unlike an analog integrator, which reduces the drift-to-signal ratio by decreasing the RC-time constant, a digital integrator has good drift performance just in applications of small signals such as diamagnetic measurement. Several methods can be considered to improve the drift performance. Further drift compensation methods such as dynamic calibration can be applied. Using an ADC of high resolution and sampling rate may help reducing the input noise and offset. Different integration algorithms like Simpson formula and interpolation method can be applied in FPGA, while the fast Fourier transform might be able to optimize the drift compensation algorithm. On the other hand, the HL-2A DIM system is required to acquire over 400 channels of signals, which puts forward high demands for data transmission and acquisition synchronization. Nevertheless, the system is based on high-performance PXI platform, which can provide not only high-speed data transmission, but also synchronized clock and trigger. Further measurements will test the system performance.

As the first digital integrator operated on HL-2A, the HL-2A DIM has fulfilled its primary goal with great potential, and the design is worthy of further research.

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