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Experimental study on heavy ion single-event effects in flash-based FPGAs

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Abstract With extensive use of flash-based field-programmable gate arrays (FPGAs) in military and aerospace applications, single-event effects (SEEs) of FPGAs induced by radiations have been a major concern. In this paper, we present SEE experimental study of a flash-based FPGA from Microsemi ProASIC3 product family. The relation between the cross section and different linear energy transfer (LET) values for the logic tiles and embedded RAM blocks is obtained. The results show that the sequential logic cross section depends not too much on operating frequency of the device. And the relationship between 0 → 1 upsets (zeros) and 1 → 0 upsets (ones) is different for different kinds of D-flip-flops. The devices are not sensitive to SEL up to a LET of 99.0 MeV cm^2/mg. Post-beam tests show that the programming module is damaged due to the high-LET ions.

Keywords Single-event effects (SEEs) · Flash-based FPGAs · HIRFL · Heavy ion experiments

1 Introduction

Single-event effects (SEEs) induced by heavy ions, alpha particles, protons and neutrons [1] become an issue of increasing concern for CMOS integrated circuits (ICs) [2, 3]. The reliability and availability of electronic devices in radiation environments are being threatened due to SEEs [1]. In the future, as transistor size shrinks and the device voltage descends, developments in advanced technologies have brought about new challenges and opportunities for the electronic devices in spatial radiation environments [4, 5].

In addition, field-programmable gate arrays (FPGAs) have gained an increasing interest and constituted an effective application-specific integrated circuit (ASIC) replacement in military and aerospace applications [6]. Two types of programming technologies, e.g., SRAM and flash cells, are used to implement the FPGA reprogrammable switches [7]. The SRAM-based FPGAs have been widely studied in the past years, and the experimental results have shown that the SRAM-based FPGAs are very sensitive to SEEs [8–10]. The flash-based FPGAs which adopt the floating gate configuration cells provide more robust than the SRAM-based FPGAs with respect to SEEs in the configuration memory [2, 7]. However, a cell of floating gate configuration is also composed of two transistors which are susceptible to SEEs. As a consequence, radiation tolerance of the flash-based FPGAs must be considered for devices to be applied in harsh radiation environments.

Studies in the past years on flash-based FPGAs have shown meaningful SEE results [11–14], and further efforts have been made using different test methods at the Heavy Ion Research Facility in Lanzhou (HIRFL). In this paper, we report the experimental results from the heavy ion tests. The upset cross section for the logic tiles and BRAMs is obtained, and some interesting and meaningful results are presented. In particular, the ratio for 0 → 1 upsets (zeros) and 1 → 0 upsets (ones) for different D-flip-flops (DFFs) is

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different. It is worth mentioning that the phenomenon is of significance for FPGA designers and for their further study on mitigation techniques. Moreover, the frequency dependency of SEU susceptibility is investigated. Single-event latch-up (SEL) characteristics of the DUTs are studied at a higher LET values. In addition, post-beam tests are performed and the corresponding test results are presented.

The paper is organized as follows. Firstly, characteristics of the device under test (DUT) are introduced in Sect. 2, and the experimental setup is described in Sect. 3. Then, the test methods are introduced briefly in Sect. 4. Next, the heavy ion experimental results are presented and discussed in Sect. 5. Finally, some conclusions are drawn in Sect. 6.

2 Device characteristics

In this experiment, a flash-based FPGA from the ProASIC3 product family is selected for the study of SEEs. The architecture overview of the ProASIC3 product family is shown in Fig. 1. The product family is fabricated with a 0.13-μm feature size and a 7-layer metal (6 copper) advanced CMOS process. The product family has up to 10 million system gates, 32 embedded block RAMs (each consisting of 4608 bits), 300 single-ended I/O and 74 differential I/O pairs. And 1 Kbits non-volatile flash ROM and 1 integrated phase-locked loops (PLL) are also included [15]. The FPGA core is composed of a sea of logic tiles, named "VersaTiles," and each logic tile can be configured as a combinatorial module, such as a three-input LUT (look-up Table 1), or configured as sequential modules, including flip-flops and latches with optional enable, clear or preset [16].

The devices A3P250PQ208I from the ProASIC3 product family were irradiated with heavy ions. The devices were de-capped by the use of an acid etching machine. After a sample was processed manually to confirm the area and location of the wafer, the acid etching machine, which can automatically control the proper dosage of the acids and the time, was used to de-cap the DUTs, so that heavy ions could reach the sensitive regions, as shown in Fig. 2.

3 Experimental setup

The SEE test setup is shown schematically in Fig. 3. It is composed of two parts. The main part, consisting of a local computer (PC1), the programmable power (PWR), the device under test (DUT) and the SEE test system (SEETS), is placed in the irradiation room. A LabWindows/CVI program on PC1 is designed to send commands and record experimental data. By sending commands, PC1 can real-timely control and monitor the voltages and currents of the PWR via RS232. When a SEL happens, the PWR can be turned off immediately and the voltages and currents can be recorded timely. Also, PC1 communicates with the SEETS via RS485. The SEETS was developed and verified successfully at the HIRFL [17–19]. The other part is a remote computer (PC2), placed in the control room, linking to PC1 with the remote desktop protocol.

All the tests were performed at the HIRFL, using ^{86}Kr ions at 25 MeV/nucleon of initial energy and ^{209}Bi ions at 9.5 MeV/nucleon of initial energy. Irradiations were carried out in air and at ambient room temperature, with heavy ions passing through a vacuum/air transition foil. The SEE test layout is shown in Fig. 4. For the experiments using

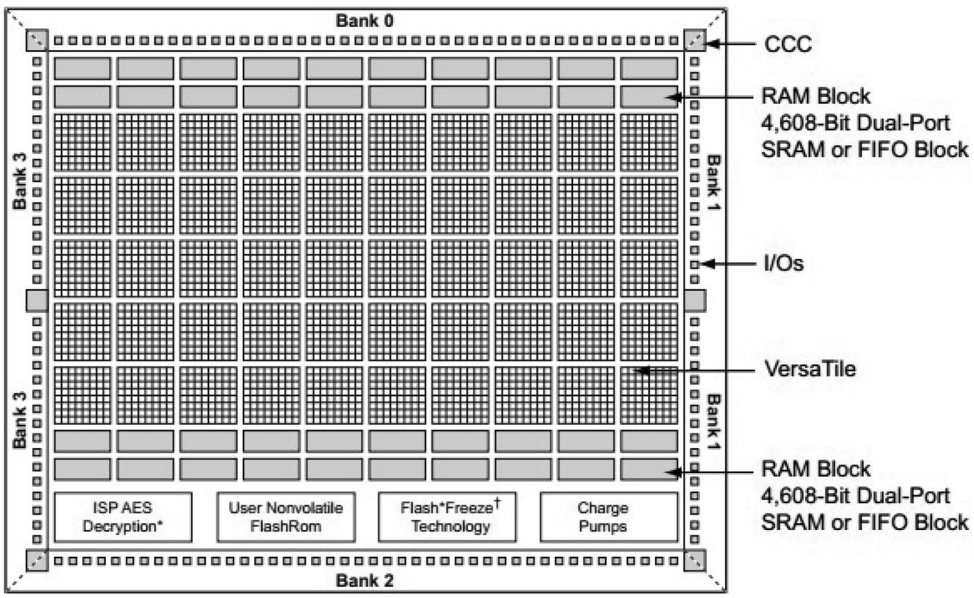

Fig. 1 The architecture overview of the ProASIC3 product family [16]

Table 1 LET values used in the experiments

Ion	Energy (MeV)	LET in silicon (MeV cm^2/mg)	Range in silicon (μm)
^{86}Kr	1783.7	21.11	263.6
^{86}Kr	1153.9	27.22	149.5
^{86}Kr	758.1	32.84	92.4
^{86}Kr	479.8	37.62	58.5
^{209}Bi	682.5	99.0	43.3

Fig. 2 (Color online) The picture of device under test on the daughter board

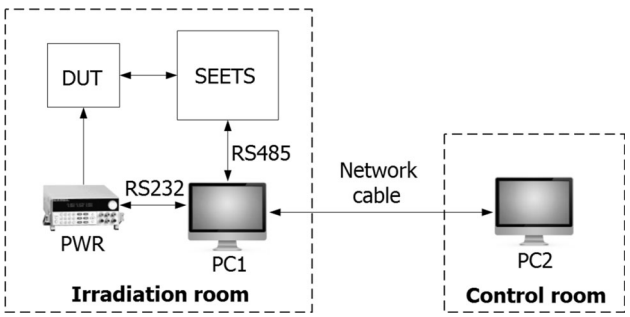

Fig. 3 Block diagram of the SEE test setup

^{86}Kr ions, the LET values of the ions could be adjusted from 21.11 MeV cm^2/mg to 40.62 MeV cm^2/mg with the air thickness of 50 mm by changing the thickness of Al, while using ^{209}Bi ions, the LET values could be adjusted from 97.0 to 99.8 MeV cm^2/mg by changing the air thickness. All the tests were done with nominal voltages of 1.5 V for the core and 3.3 V for the IO. The ion energy, LET and range in silicon are listed in Table 1.

Fig. 4 (Color online) The SEE test layout at the HIRFL

4 Test methods

The test methods have been designed and verified successfully [20]. Figures 5 and 6 illustrate block diagrams of the logic tiles and BRAMs test design. For the logic tiles, the shift register chains (SRC) consist of different reset modes, such as without reset (NORST), synchronous reset (SYNRST), asynchronous reset (ASYNRST) and asynchronous reset synchronous release (ARSRRST). And every reset mode is divided into three groups which include three different input patterns including all "0"s, all "1"s and checkerboard. In every group, there are three SRCs of the same length. The DUT consists of 6144 logic tiles, 6066 of which are used in this design. For the test design of the BRAMs, all the 8 embedded RAM blocks are used and configured to the ratio 512 × 9. And every RAM block can be written into different patterns which include all "0"s, all "1"s and checkerboard.

When the SEUs happen in the DUT, the upset can be detected and captured in time by the error check module (ErrCheck) in the control FPGA (CFPGA). The upset messages which contain the error time, the number and the upset data can be saved in the error fifo module (ErrFifo). For the logic tiles, each SRC corresponds to an ErrFifo, so it is necessary to put every ErrFifo together by means of the circulation check module (CirCheck). The combined SEU

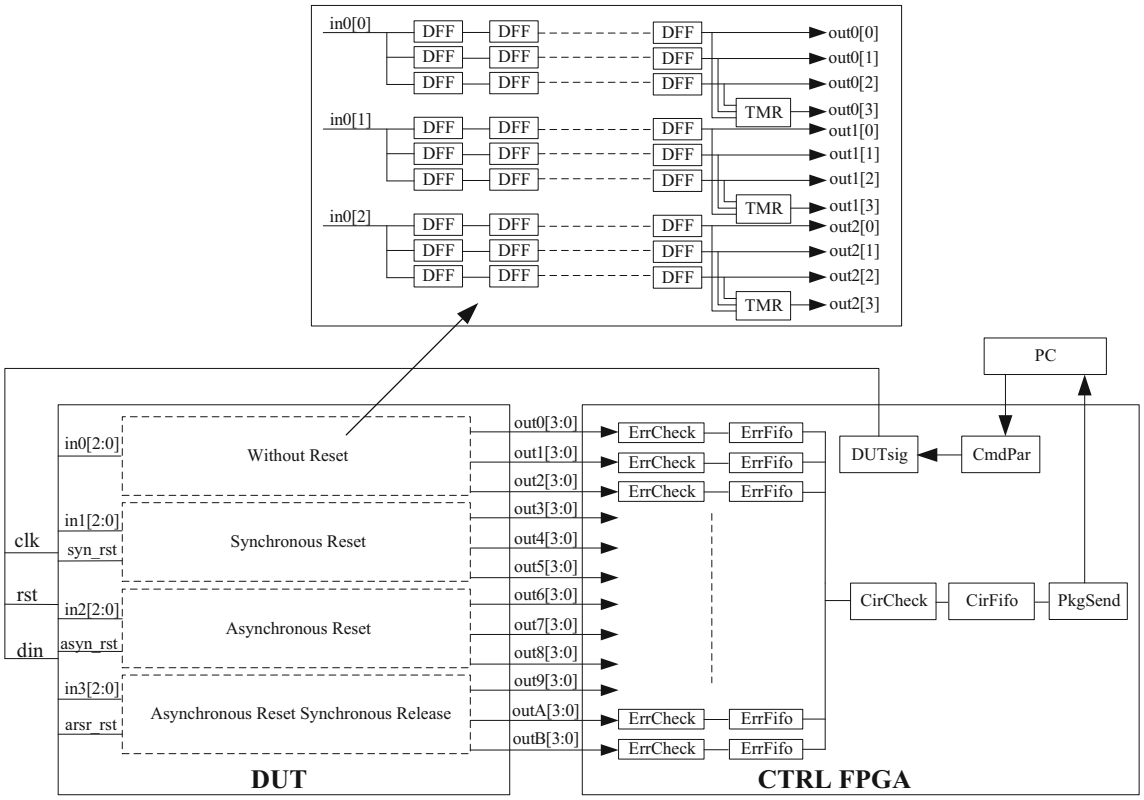

Fig. 5 Block diagram of the logic tiles test design

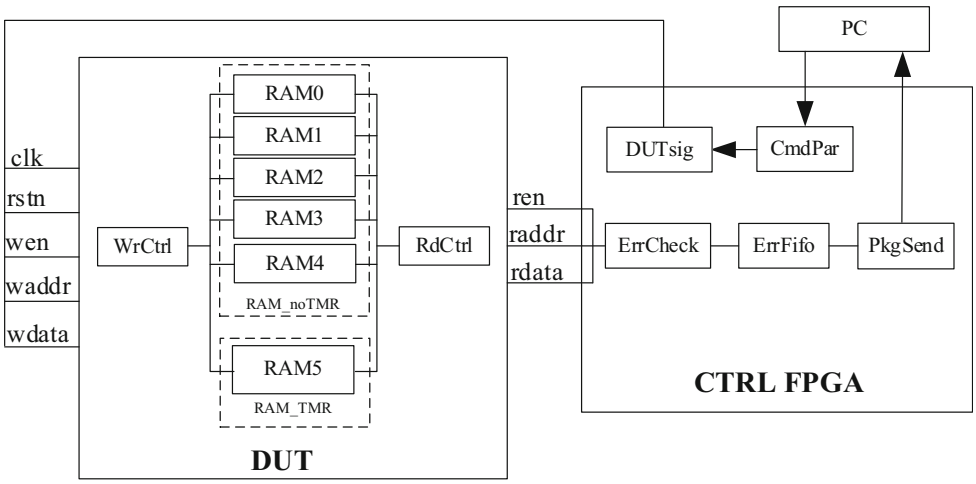

Fig. 6 Block diagram of BRAM test design

messages are stored in the circulation fifo module (CirFifo) and packed to the PC at last. For the BRAMs, it is relatively simple. The upset messages are saved in the ErrFifo and packed to the PC directly.

5 Results and discussion

The experimental results are presented below in the following order. First, cross sections for the logic tiles at different LET values are reported, and the frequency dependency of SEU susceptibility and the ratio of zeros and ones are analyzed. Then, cross sections for the BRAMs at different LET values are presented. Next, the SEL characterization of the device is introduced. Finally, post-beam tests are performed and the experimental phenomena are presented.

5.1 The logic tiles

The experiments of logic tiles were performed at different LETs to obtain the relation between the cross section

and the LETs. The following equation is used to calculate the cross section:

$$\sigma = N_F/(\Phi N_M), \quad (1)$$

where σ is the normalized cross section, N_F is the upset number induced by heavy ions, Φ is fluence of the heavy ions, and N_M is the number of cells [21]. The SEU cross section as function of LET is shown in Fig. 7a.

In order to investigate the frequency dependency of SEU susceptibility, several tests were performed at two LET values and operating frequencies which includes 100, 50, 25 and 12.5 MHz. As shown in Fig. 7b, the error cross section remains almost constant at different frequencies. The test results indicate that the sequential logic cross section depends not too on the device's operating frequency.

Interesting phenomena were discovered in the experiments. Because four types of reset modes are adopted in the design, different DFFs were analyzed to validate the ratio of 0 → 1 upsets (zeros) and 1 → 0 upsets (ones). The test results showed a different relationship between zeros and ones for different reset modes. As shown in Fig. 8, the cross section of zeros is higher than ones for NORST and SYNRST. On the contrary, the cross section of ones is higher than zeros for ASYNRST and ARSRRST.

As described above, each logic tile can be configured as different DFFs. Every logic function is mapped on the logic tile by configuring the floating gate switches [16]. Basic units of the different reset modes in the design are shown in Fig. 9. The D-type flip-flop with active high clock (DFN1) is used in NORST and SYNRST. Both of them indicate the same rule. The D-type flip-flop with active low clear (DFN1C0) is used in ASYNRST. Another D-type flip-flop with active high clear (DFN1C1) is used in ARSRRST. Highlight routing path of the DFN1, DFN1C0 and DFN1C1 functions implemented on the logic tile is illustrated in Fig. 10. Furthermore, the simple schematics of the DFN1, DFN1C0 and DFN1C1 implemented on the logic tile are illustrated in Fig. 11. Except the part of clear function, the remaining function modules are the same. Hence, we can conclude that the difference between ones and zeros is caused due to the distinction of clear function.

5.2 BRAMs

In the experiments, a logical "checkerboard" pattern is adopted to test the BRAMs cross section. Only single-bit upset (SBU) occurred in the experiments. Figure 12 presents the relation between the SEU cross section and the

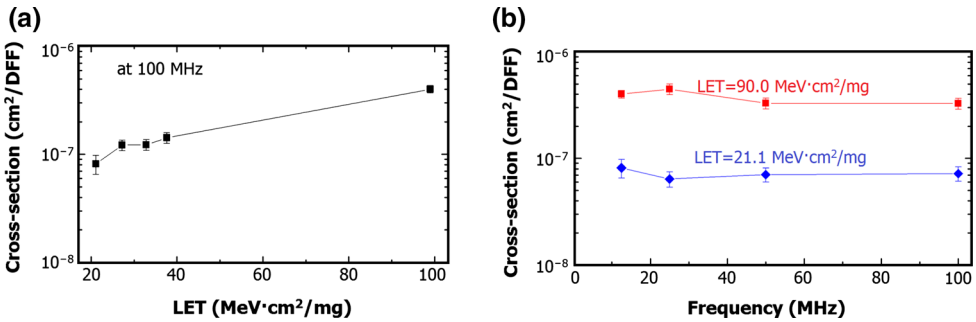

Fig. 7 (Color online) The DFF cross section as function of **a** LETs at 100 MHz and **b** frequency

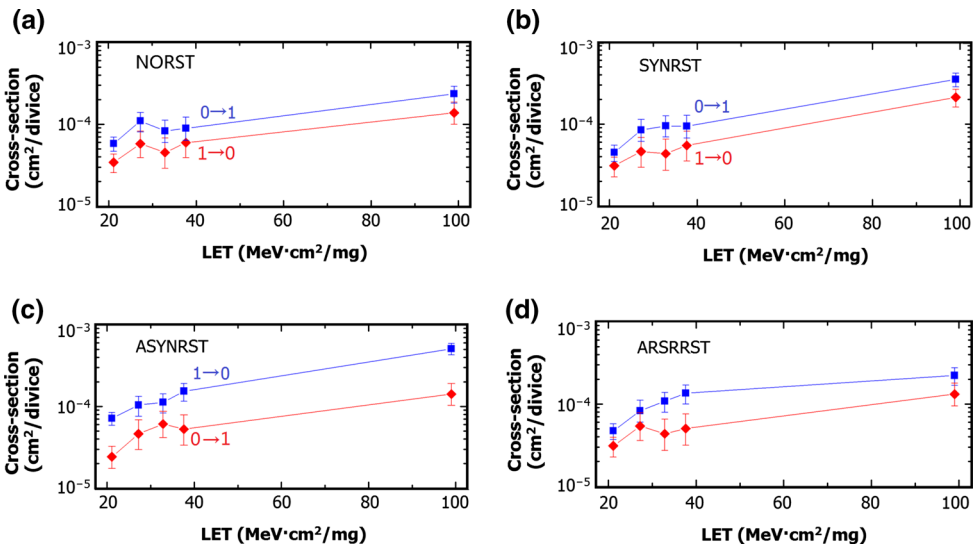

Fig. 8 (Color online) Cross section of different reset modes versus LETs for zeros and ones

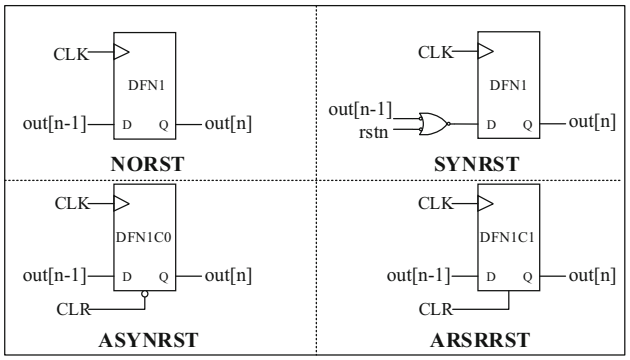

Fig. 9 The basic unit of the different reset modes

LET values. Compared with the test results of the logic tiles, the BRAMs cross section at the same LET value is an order of magnitude lower. As a consequence, the BRAMs are more sensitive to SEEs than the logic tiles.

5.3 Single-event latch-up

Single-event latch-up is a potentially and abnormal high-current state. It may cause permanent damage to the device. High-LET ^{209}Bi ions (up to 99.0 MeV cm^2/mg) were used to investigate the SEL characterization of the device, but no SEL events were observed. The results indicate that the ProASIC3 product family is not sensitive to SEL.

5.4 Post-beam tests

The DUTs can be damaged by heavy ions, so post-beam tests were performed, in which the function, state and reconfiguration of the DUTs were tested under the laboratory conditions after each irradiation experiment. The test results indicate that the function and state of the devices are normal. After ^{86}Kr irradiation, all the DUTs are

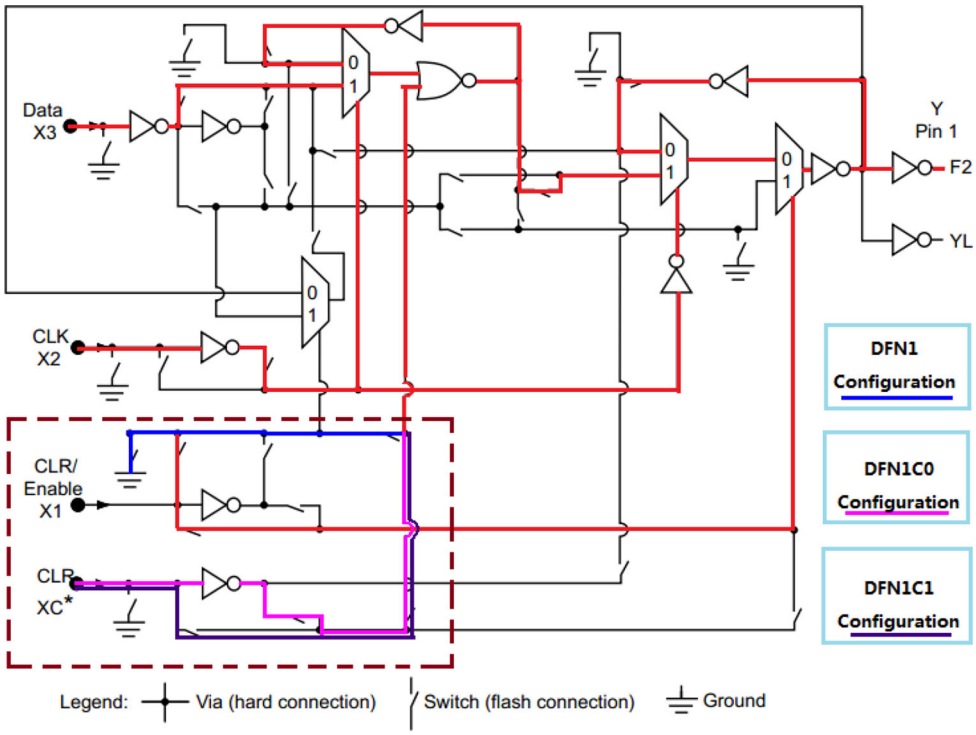

Fig. 10 (Color online) Highlight routing path of the DFN1, DFN1C0 and DFN1C1 functions implemented on the logic tile

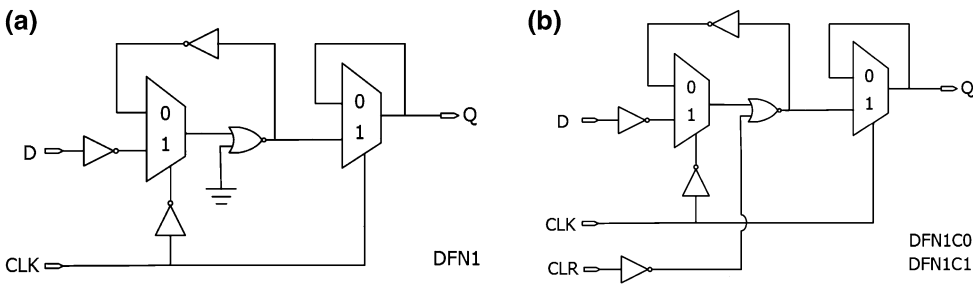

Fig. 11 The simple schematics of the DFN1, DFN1C0 and DFN1C1 implemented on the logic tile

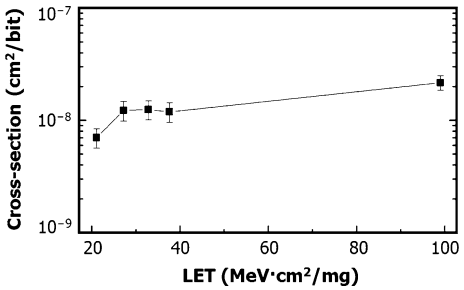

Fig. 12 The BRAMs cross section versus LETs at the checkerboard pattern

Table 2 Total ^{209}Bi ion fluence of the DUTs

Samples	LET in silicon (MeV cm^2/mg)	Total fluence (ions/cm^2)
DUT1	99.0	819,208
DUT2	99.0	374,612

reconfigured successfully, whereas all the DUTs fail reconfiguration after ^{209}Bi irradiation. In the experiments, two chips were tested as follows: DUT1 was used to test the logic tiles, and DUT2 was used to test the BRAMs. DUT2, suffered less total ^{209}Bi ion fluence than DUT1 (Table 2), failed reconfiguration in pose-beam tests. Allen G R and Swift G M [22] did similar post-beam tests at the LETs of 3.07–75.0 MeV cm^2/mg and found no damage to the DUTs. Hence, we infer that the programming module of the DUTs is damaged due to the high-LET ions. Therefore, high attention should be paid to the programming module in its further improvement.

6 Conclusions

The heavy ion irradiation experiments have been carried out at the HIRFL. The experimental results have been obtained about SEE characterization. The relation between the cross section and the LET values for the logic tiles and BRAMs is presented and can provide references for the designer and manufacturer in relevant areas. The experimental results show clearly that the sequential logic cross section depends just a little on operating frequency of the device. The relationship between zeros and ones is different for different kinds of DFFs. The devices are not sensitive to SEL up to a LET of 99.0 MeV cm^2/mg, whereas the programming module is damaged by the high-LET ions, which should be brought to the attention.

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