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Design and implementation of power and phase feedback control system for ICRH on EAST

Zhao Chen[1,2] · Yan-Ping Zhao[1] · Gen Chen[1] · Yan Cheng[1] · Jian-Hua Wang[1,2] · Jia-Hui Zhang[1,2] · Yu-Qing Yang[1,2]

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Abstract Ion cyclotron wave resonance heating (ICRH) is one of the most important auxiliary methods to heat plasma in the Experimental Advanced Superconducting Tokamak (EAST). Several megawatts of power is transmitted through separate coaxial lines and coupled with the plasma through arrays of loop antennas. The parameters of the ICRH system, including the injected power and phasing between antenna straps, are critical to the coupling efficiency of the power as well as the resulting impact on the heating efficiency. In this paper, we present a system for feedback control of the phase between the current straps and the ICRH power on EAST. The feedback control system was tested using both a matched dummy load and a plasma load, and it successfully maintained stable operation in the 2016 EAST campaign. Good control of the injected power and wave phases was achieved during edge-localized mode operation.

Keywords ICRH · Phase · Power · Feedback control system · FPGA

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✉ Zhao Chen
chen207@mail.ustc.edu.cn

1 Institute of Plasma Physics, Chinese Academy of Sciences, Hefei 230031, China

2 University of Science and Technology of China, Hefei 230027, China

1 Introduction

EAST (Experimental Advanced Superconducting Tokamak), a national fusion project in China, is the first tokamak to employ superconducting toroidal and poloidal magnets. The ion cyclotron wave resonance heating (ICRH) system is among the most powerful heating tools and is also used to control the spatial distribution of some important plasma parameters [1, 2]. Theoretical calculations and experimental studies show that the ICRH antenna has a better heating effect and produces relatively few impurities when operated in the dipole phase. In addition, the antenna can drive current by inducing an asymmetric spectrum in the monopole phase [3, 4]. Therefore, measurement and precise control of the antenna phase are of great significance for the study of ion cyclotron heating and current drive. If the phase of the antenna cannot be accurately measured and controlled, it would cause power imbalance between the antenna straps and affect the wave coupling efficiency.

During the EAST 2016 spring campaign, eight 1.5 MW ICRH transmitters were installed to feed two ICRH antennas at frequencies of 35 and 34 MHz, respectively. Four of the transmitters powered the B-port antenna, and the other four powered the I-port antenna; they were distributed as shown in Fig. 1. The phases of the relative generator, ϕ_2, ϕ_3, ϕ_4, ϕ_6, ϕ_7, and ϕ_8, were set such that the inner strap voltage phase differences were $\phi_2 - \phi_1 = \phi_3 - \phi_1 = \phi_4 - \phi_1 = 0$ and $\phi_7 - \phi_5 = \phi_8 - \phi_5 = \phi_7 - \phi_6 = \pi$ [5, 6].

A QNX OS-based phase control system has been implemented in the Lower Hybrid Current Drive (LHCD) system [7, 8]. Time resolution and feedback control take 2 ms. The LHCD phase control system can provide us with

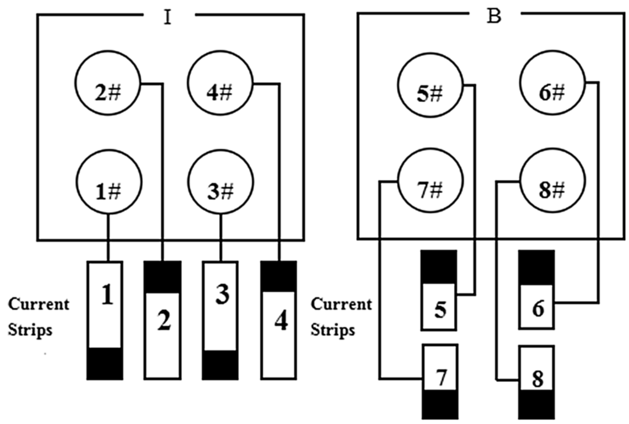

Fig. 1 Distribution of straps on I port and B port of EAST

experience. In previous experiments on the ICRH system, in which we manually set the control signal to adjust the actual injected power and phase to the needed values, the control signals were held constant during a discharge and thus led to random variation of the injected power and phase. Therefore, implementation of a power and phase feedback control system is critically needed for stable ion cyclotron range of frequency (ICRF) operation. Briefly, our main objective in this paper is to establish a real-time data acquisition and feedback control system for the power and phase.

2 System overview

There are eight sets of transmission networks in the EAST ICRH system, each of which includes a radio frequency (RF) transmitter, an impedance-matching network, decouplers, transmission lines, and antennas [9]. The system for feedback control of the power and phase performs an important task and includes phase and power detection modules, an acquisition module, and a feedback control module. The main functions are implemented on two circuit boards based on field-programmable gate arrays (FPGAs). One processor board acquires the phase and power signals. The other control board communicates with the host personal computer (PC) and fulfills the feedback control of the power and phase.

Directional couplers are mounted on the lines near the last-stage amplifiers to measure the peak voltage of the incident wave. The power of the incident wave can be calculated from the peak voltage [10–12]. The phase difference between the current straps is converted into an analog signal by the phase detector and then sent to the data acquisition module through a signal conditioning circuit. The actual values of the phase and power are calculated in the FPGA chip. Another FPGA completes the feedback control algorithm and sends the power and phase data to the host computer through a USB interface for display and storage. The digital control signal is converted into an analog signal by a digital-to-analog converter (DAC) and then sent to the voltage-controlled connectors of the generator. This entire system can perform closed-loop feedback control of the phase and power. A schematic view of the feedback system is provided in Fig. 2.

3 Design of the feedback control system

3.1 Detection of power and phase signals

The amplitude and phase are two of the fundamental properties of the RF wave. The amplitude and phase difference between two RF signals are measured using a peak detector and phase detector, respectively. The RF amplitude is converted into a direct current (DC) signal using a peak-type diode detector and a resistor–capacitor low-pass filter, as shown schematically in Fig. 3. The phase difference between both RF signals is converted into a DC signal through a phase detector, consisting mainly of a digital phase-frequency detector (HMC439). The previous phase detector consisted of two AD8302 gain and phase detector chips. Two AD8302 chips were used because of the limited measuring range (180°); to detect the phase difference in a range of 0°–360°, one phase of the RF signal was shifted by 90°. Additionally, the AD8302 chip exhibited serious nonlinearity at the top and bottom of the characteristic curve, which introduced errors into the measurement result [13, 14]. In contrast, only one HMC439 chip needs to be used in the new phase detector design. The new phase detector has a wider measurement range (up to 720°) and ultralow phase noise. Moreover, it has good linearity, which makes the subsequent data processing more convenient.

The RF signals enter the analog chip (HMC439) through band-pass filters and are converted into two square wave signals corresponding to the phase difference. Then the square wave is converted into a single-ended DC signal by a loop filter. The precision of the phase detector is less than 0.5°. The phase detector has a 720° range and an 8 μs response time. The characteristic curve of the phase detector is shown in Fig. 4.

3.2 Signal conditioning and acquisition

The main function is realized on two circuit boards, the acquisition board and the feedback control board. The acquisition board converts the analog power and phase signals from the power and phase detectors to digital signals. It consists of 24 input channels. Each acquisition

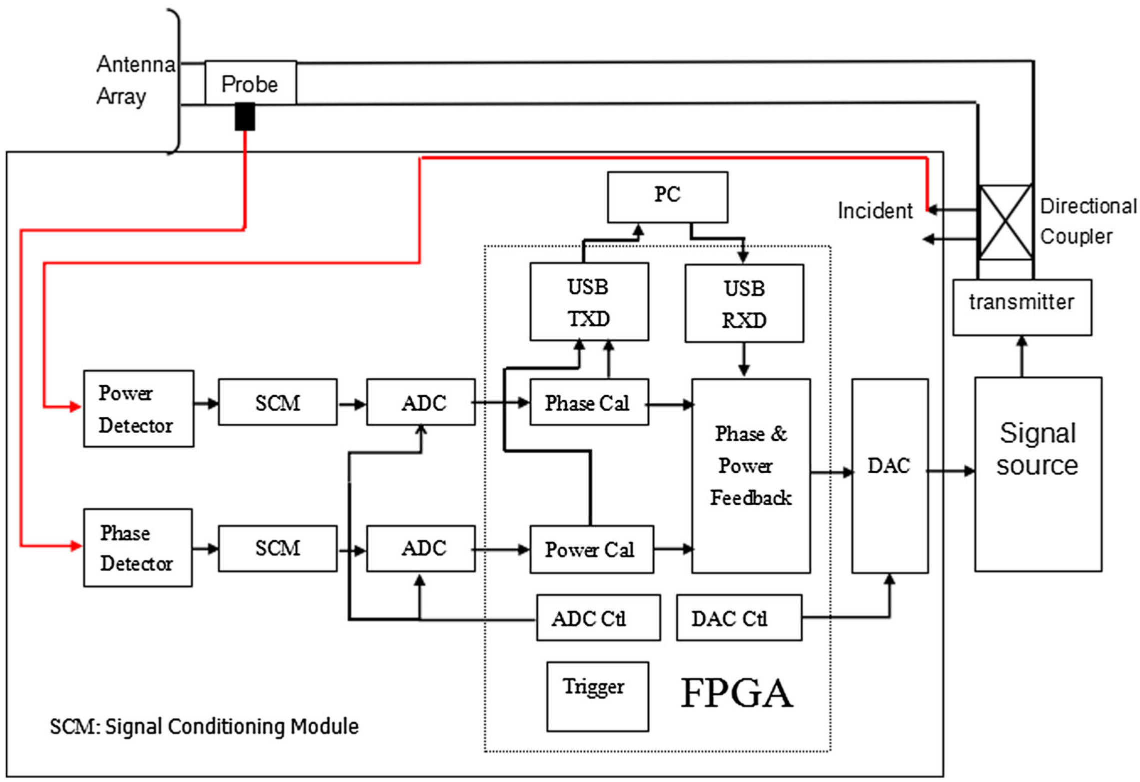

Fig. 2 Overall architecture of the system for feedback control of the power and phase. The functions of the two FPGA chips used in our system are merged into one block enclosed by the dotted line

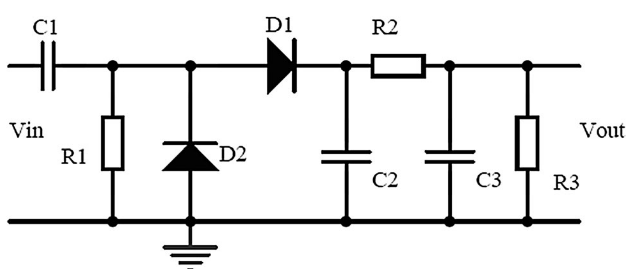

Fig. 3 Schematic of power detector

channel has a second-order low-pass filter. The weak signal is amplified by using an operational amplifier (AD8031), with a bias to adjust the input voltage to the range of the analog-to-digital converter (ADC). Through the filters and amplification stages, the analog signals are digitized by means of low-voltage differential signaling (LVDS) by the ADC (ADS5270) with 12-bit resolution at a 40 MHz sampling rate [15].

The FPGA chip on the acquisition board de-serializes the LVDS inputs from the ADC and calculates the real-time values of the power and phase using cubic curve fitting and linear fitting, respectively. It also controls the time sequence of the ADCs and supplies the clock signal by a phase-locked loop. Finally, the power and phase data are

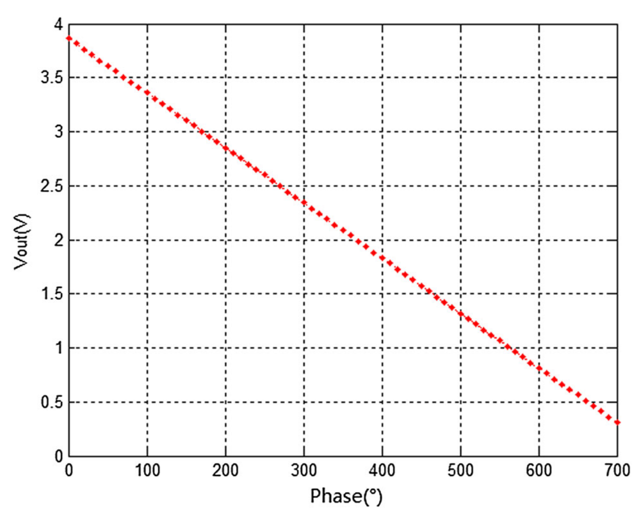

Fig. 4 Output voltage versus phase difference

transmitted to the feedback control board by the serial peripheral interface (SPI).

3.3 Feedback control of power and phase

The feedback control board can complete both down-links and uplinks with the control PC and is responsible for calculating the power and phase feedback control through

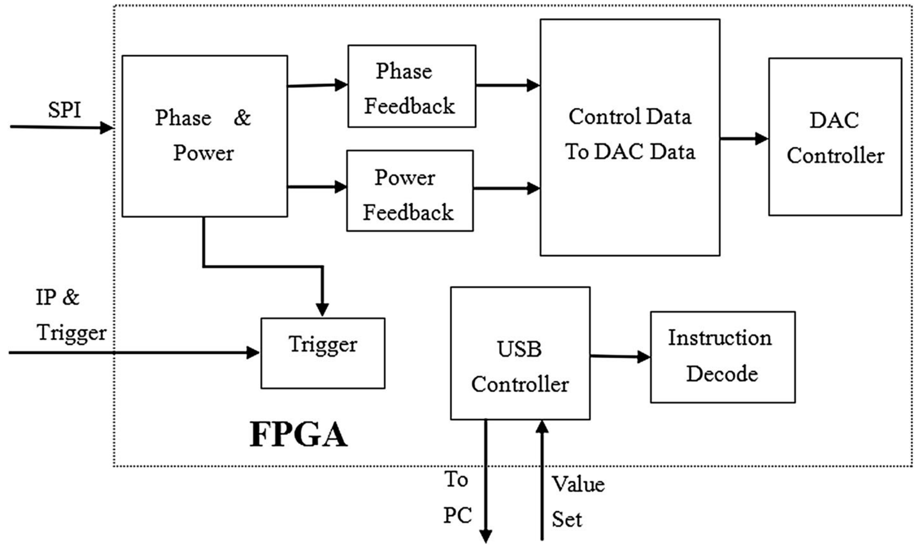

Fig. 5 Block diagram of the feedback control board

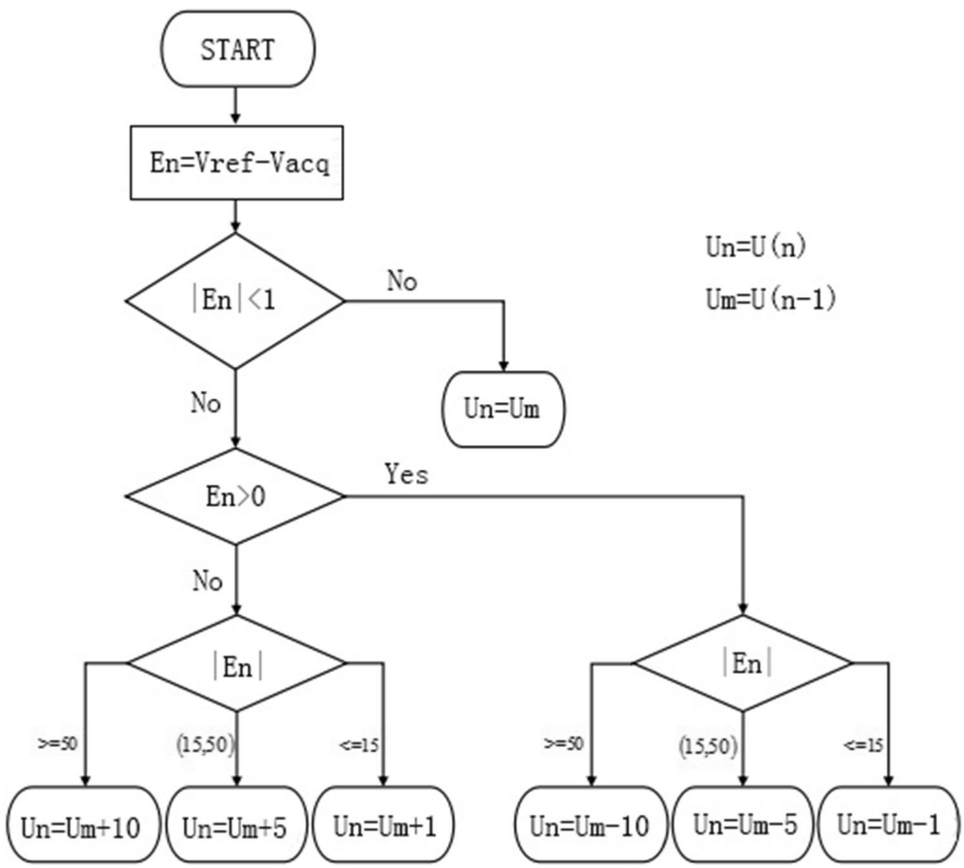

Fig. 6 Program flowchart of power feedback control

an Altera Cyclone IV FPGA. The feedback control data is converted into analog signals by the DAC (TLV5630) with 12-bit resolution at a 1 MHz conversion rate, which serves as input for the phase voltage control port of the signal source and the electronic attenuator, respectively. The process of acquisition and control is triggered on the rising edge of a signal given by the central control room. A USB controller (CY7C68013 USB micro-controller) is installed on the main board to facilitate data transfer between the feedback control board and the host PC. In addition to acquiring the received data on the PC for display and storage, it is used to receive the control parameters that are set by the software on the host computer. The main processor on the feedback control board is also an FPGA chip.

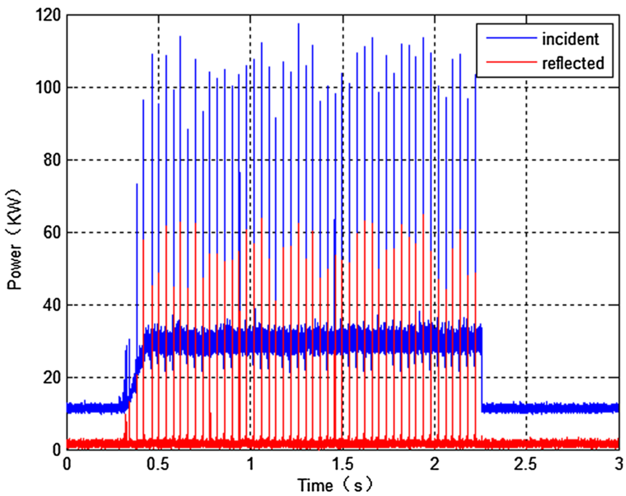

Fig. 7 (Color online) Measured incident power and reflected power. Protection was triggered when the phase of the RF changed very rapidly

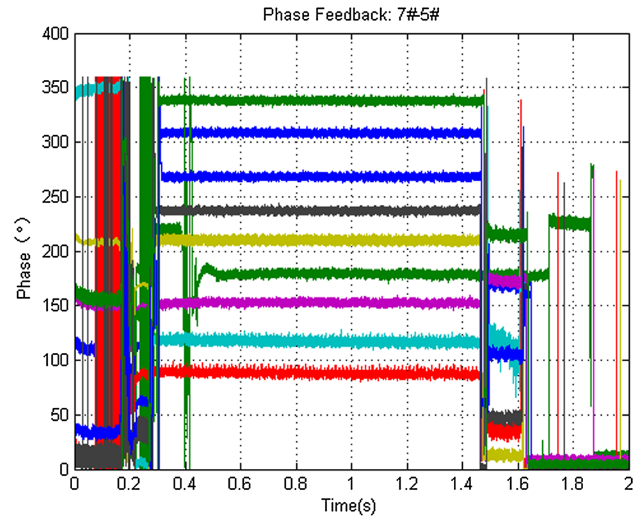

Fig. 9 (Color online) Result of phase feedback control between straps 7 and 5 in 30° steps

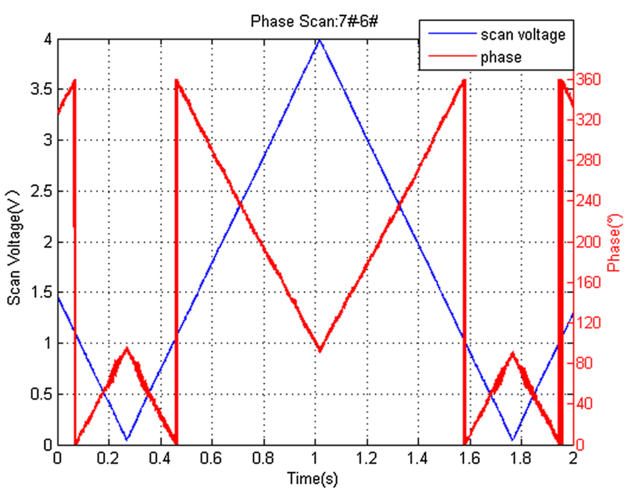

Fig. 8 (Color online) Example of a strap phasing scan on the I-port antenna at constant ICRH power and constant strap amplitude ratio

There are several advantages in using an FPGA, mainly because of its enormous real-time data processing capability. Data can be processed using the embedded digital signal processing blocks available in the FPGA, which can work in parallel to process large amounts of data [16, 17]. A block diagram of the feedback control board is shown in Fig. 5.

Three modes are used to control the power and phase of the ICRH system: scanning mode, fixed mode, and feedback mode. In scanning mode, the phase or power varies from the minimum to the maximum with changes in the control voltage. Thus, we can determine which phase we want to heat the plasma most effectively. The power scanning mode is used only for test purposes; it cannot be used for plasma heating. In fixed mode, the control voltage is a constant, even if the power and phase are unsteady because of plasma impedance variations. Feedback mode is the main working mode for operation; the power and phase values can be controlled as needed even during a fast load vibration discharge.

Because the feedback control algorithms for the power and phase are similar, we talk only about the power control rules, which are basically the same as those for phase control. When the control system works in feedback mode, the power error can be calculated using the reference and sampling values. If the absolute error of the power is less than 1 kW, the output control signal remains unchanged. Otherwise, the feedback control signal can be either increased or decreased, depending on the type of error (increased if it is positive, decreased if it is negative). Six levels of control are possible according to the interval in which the error value lies: below − 50 kW, between − 50 and − 15 kW, between − 15 and 0 kW, between 0 and 15 kW, between 15 and 15 kW, and above 50 kW. Thus, the system not only improves the feedback speed but also reduces the overshoot. One period of feedback control takes less than 20 µs with a 40 MHz sampling bandwidth, 10 Mbps transmission rate of the SPI protocol, and high-speed hardware processing by the FPGAs. A flowchart of the feedback power control program is shown in Fig. 6.

The impedance-matching network and decouplers in the ICRH system are designed for a fixed frequency. A large standing wave ratio will result in automatic protection of the system owing to the impedance mismatch, as shown in Fig. 7. The frequency of the phase modulation signal is the derivative of the displacement with respect to time:

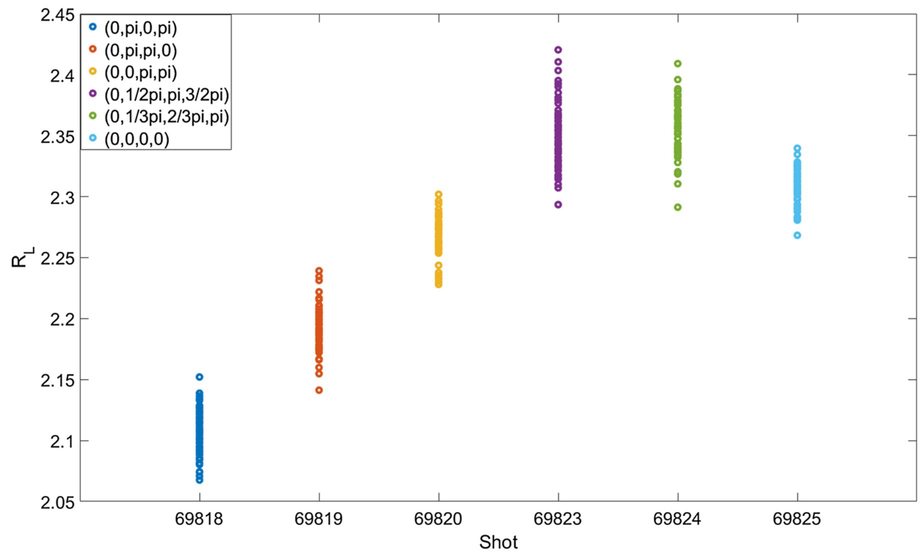

Fig. 10 (Color online) Example of impedance change on strap 1 of the I-port antenna with different phase shifts among straps 1–4. The ICRH power was constant at 1 MW. Note that the impedance became highest during the phase shifts (0, 1/2π, π, 3/2π)

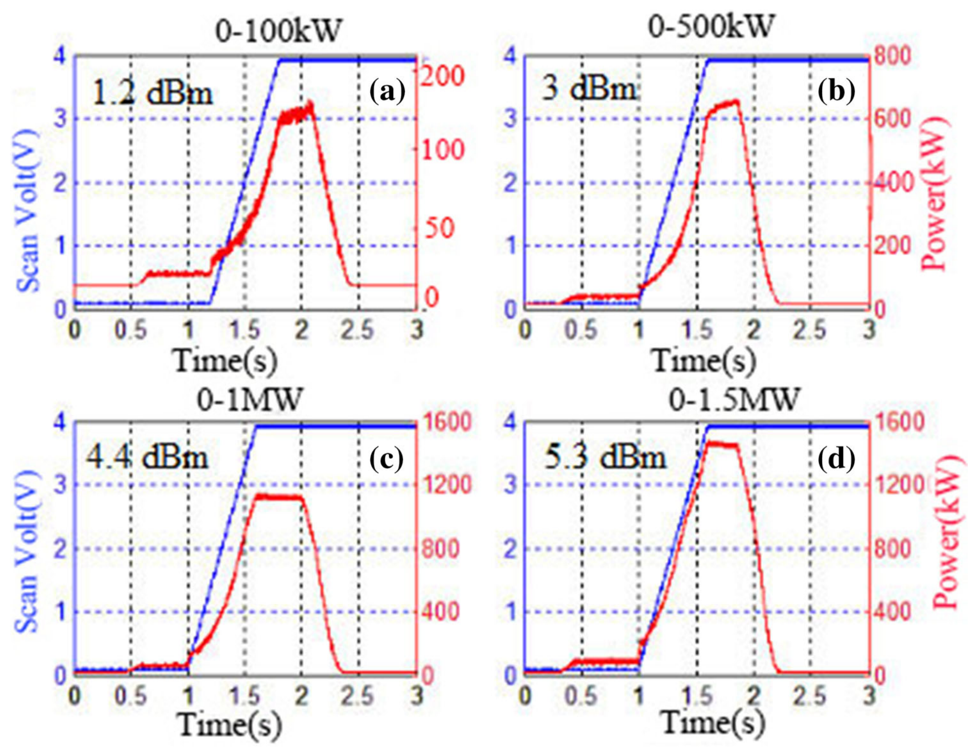

Fig. 11 (Color online) Four typical power curves. Transmitter 8 operated in scanning mode with four subsections

$$\omega(t) = \frac{\mathrm{d}\phi(t)}{\mathrm{d}t} = \omega_c + \Delta\omega, \quad (1)$$

where ω_c is the fixed frequency of the RF signal, and $\Delta\omega$ is the offset frequency caused by the phase change [18]. That is, a large phase change will result in a large change in the frequency. Thus, we restrict the phase change step to 0.1° to avoid frequency variation due to a dramatic change of phase.

4 Experimental results

The power and phase feedback control system was tested using a matched dummy load and was applied to the plasma condition. Figure 8 shows the phase difference between straps 7 and 6 in scanning mode with the matched dummy load. We see that the phase difference changes linearly with the control signal.

As shown in Fig. 9, the phase difference ($\Delta\varphi$) between straps 7 and 5 of the B-port antenna was set in 30° steps.

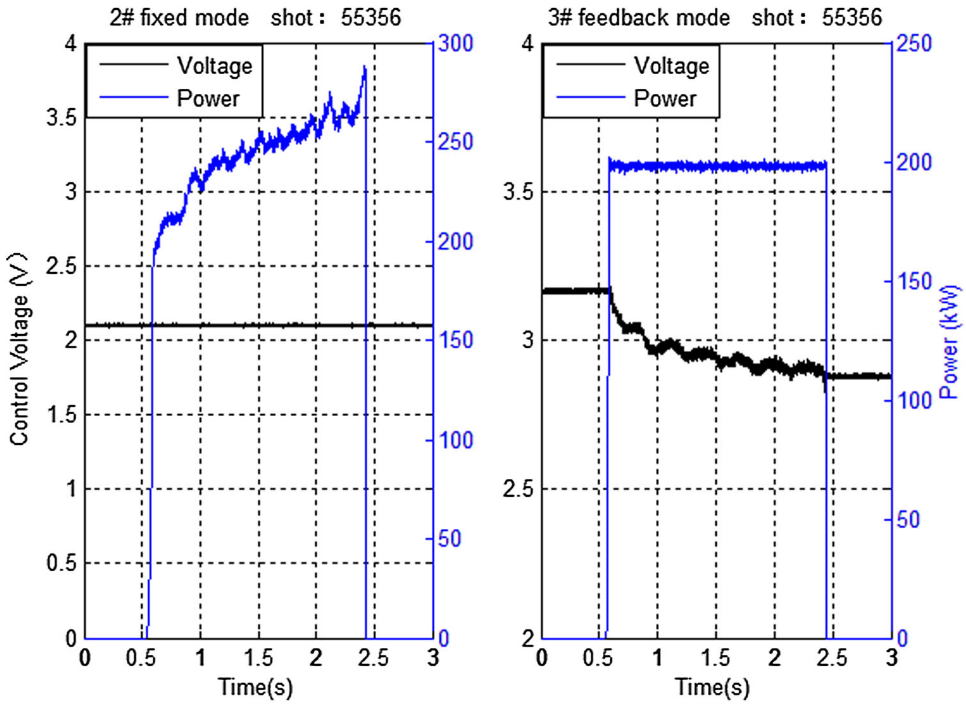

Fig. 12 (Color online) Output power curve when transmitter 3 operated in feedback control mode and transmitter 2 operated in fixed mode in shot 55356 of EAST experiment

The phase error was less than 5° with the application of feedback control mode. Plasma was heated for 1.3 s, and it took another 0.3 s for the ICRF system to receive and react to the information. To ensure the integrity of the data collected, the acquisition always continued for slightly longer than the heating time lap. These delays were responsible for the fluctuations as shown in both sides of Fig. 9.

To investigate the relationship between the coupling coefficient and the antenna phasing, a series of experiments was performed on the I-port antenna. The loading reflection coefficient is

$$\Gamma_L = (Z_L - Z_0)/(Z_L + Z_0), \quad (2)$$

where Γ_L is the reflection coefficient at the antenna, Z_L is the impedance of the transmission line (50 Ω), and Z_0 is the load impedance (less than 10 Ω) [19–21]. Thus, with increasing load impedance, the reflection coefficient decreased, and the coupling efficiency improved.

Figure 10 shows the impedance of the I-port antenna during operation in different phases. The result shows that the I-port antenna has the maximum coupling impedance at the (0, 1/2π, π, 3/2π) phases and thus exhibits the best coupling coefficient.

From the control PC, we can set the RF amplitude of the wave. There are eight electronic attenuators, one for each RF source. The voltage-controlled value of the electronic attenuators can be set between 0 and 4 V. Figure 11 shows the results of power scans for different input values from the control PC. These results can be used to calibrate the voltage. After calibration, the power can be controlled directly from the control PC. Four different values of the RF amplitude were set up for powers in the following intervals: 0–100 kW, 0–500 kW, 0–1 MW, and 0–1.5 MW.

To verify the effectiveness of the feedback controller, transmitters 2 and 3 were set to fixed mode and feedback control mode, respectively. Figure 12 shows typical control curves for shot 55356 with the plasma load. The control voltage of generator 2 was set to a fixed value, and the power exhibited large fluctuations between 200 and 280 kW caused by changes in the plasma load. In contrast, transmitter 3 operated in feedback control mode, and the power was set to 200 kW on the host software. The result shows that the output power remained constant at 200 kW.

5 Conclusion

Feedback control systems for both the power and phase were successfully implemented on the ICRH system of EAST. The system is composed of power and phase detection modules, an acquisition module, and a feedback control module. Phase detectors and power detectors were used to measure the phase difference and RF amplitude, respectively. Real-time calculation and feedback algorithms were executed by FPGA chips. The feedback control system could quickly and accurately control the power and phase at the required set values.

References

1. Y.X. Wan, P.D. Weng, J.G. Li et al., Progress of the EAST Project in China, in the 21st International Atomic Energy Agency (IAEA) Fusion Energy Conference (Oral). Chengdu, China, Oct. 16–21 (2004)
2. A. Messiaen, R. Koch, R.R. Weynants et al., Performance of the ITER ICRH system as expected from TOPICA and ANTITER II modelling. Nucl. Fusion **50**, 02502 (2010). https://doi.org/10.1088/0029-5515/50/2/025026
3. R.H. Goulding, D.J. Hoffman, P.M. Ryan et al., A power compensation system for phased operation of the JET A2 antenna arrays, in the 17th Symposium on Fusion Technology. Rome, Italy, Sep. 14–18 (1992)
4. R.H. Goulding, F.W. Baity, D.J. Hoffman et al., Design and control of phased ICRH antenna arrays, in Symposium on fusion engineering. MA, United States, Oct. 11–15 (1993)
5. Chen Gen, Qin Chengming, Mao Yuzhou et al., Power compensation for ICRF heating in EAST. Plasma Sci. Technol. **18**, 870–874 (2016). https://doi.org/10.1088/1009-0630/18/8/14
6. He Zhongxin, Zhang Xinjun, Zhao Yanping, Results of ICRF heating experiments from the EAST 2010 campaign. Plasma Sci. Technol. **17**, 188–190 (2015). https://doi.org/10.1088/1009-0630/17/3/03
7. Y. Yang, J. Shan, D. Wang et al., The design of LHCD phase control system based on QNX operating system, in Paper presented at the 4th International Conference on Computational Intelligence and Software Engineering, Wuhan, China, Dec. 11–13 (2009)
8. Wikipedia QNX (2017), https://en.wikipedia.org/wiki/QNX. Accessed 27 Feb 2017
9. Yuzhou Mao, Shuai Yuan, Yanping Zhao et al., High power RF transmitters for ICRF applications on EAST. Plasma Sci. Technol. **15**(3), 261–265 (2013). https://doi.org/10.1088/1009-0630/15/3/14
10. J. Ira, Pitel, measuring peak-to-peak output voltage: magnapower electronics shares its method. IEEE Trans. Power Electron. **1**(2), 18–19 (2014). https://doi.org/10.1109/MPEL.2014.2312276
11. Wikipedia, Amplitude (2017), https://en.wikipedia.org/wiki/Amplitude. Accessed 11 Feb 2017
12. R. Ochoukov, V. Bobkov, H. Faugel et al., A new B-dot probe-based diagnostic for amplitude, polarization, and wavenumber measurements of ion cyclotron range-of frequency fields on ASDEX upgrade. Rev. Sci. Instrum. **86**, 115112 (2015). https://doi.org/10.1063/1.4935833
13. L. Yue, L. Dong, The cable phase difference detection of very high frequency (VHF) antenna array based on AD8302, in Paper Presented at the 3rd International Conference on Information Science and Control Engineering, Beijing, China, Jul. 08–10 (2016)
14. Analog Devices, LF-2.7 GHz RF/IF Gain and Phase Detector, http://www.analog.com/media/cn/technical-documentation/data-sheets/AD8302.pdf. Accessed 2 Mar 2017
15. Texas Instruments, 8-Channel, 12-Bit, 40MSPS ADC with Serial LVDS Interface, http://datasheet.octopart.com/ADS5270IPFP-Texas-Instruments-datasheet-142677.pdf. Accessed 28 Feb 2017
16. S.G. Castillo, K.B. Ozanyan, Field-programmable data acquisition and processing channel for optical tomography systems. Rev. Sci. Instrum. **76**, 095109 (2005). https://doi.org/10.1109/TNS.2016.2610142
17. Chun-Fei Hsu, Bore-Kuen Lee, FPGA-based adaptive PID control of a DC motor driver via sliding-mode approach. Expert Syst. Appl. **38**, 11866–11872 (2011). https://doi.org/10.1016/j.eswa.2011.02.185
18. J. Zhao, M. Lu, J. Deng, Foundations of Radio Frequency Circuits, 2nd edn. (Xi'an, Shanxi, 2010), pp. 211–216 (in Chinese)
19. Wikipedia, Transmission line (2017), https://en.wikipedia.org/wiki/Transmission_line. Accessed 9 Feb 2017
20. B.S. Guru, H.R. Hızıroğlu, *Electromagnetic Field Theory Fundamentals*, 2nd edn. (University of Cambridge, Cambridge, 2004), pp. 422–423
21. Chunqi Qian, William W. Brey, Impedance matching with an adjustable segmented transmission line. J. Magn. Reson. **199**, 104–110 (2009). https://doi.org/10.1016/j.jmr.2009.04.005