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Clock synchronization design and evaluation for trigger-less data acquisition system

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Abstract For modern particle physics experiments, trigger-less data acquisition (DAQ) system has been put into practice because of the need of reaction multiplicity and trigger flexibility. In such new DAQ systems, global synchronized clock plays an important role because it affects the granularity of time slice and precision of reference clock. In this paper, a novel synchronized clock distribution method is proposed. With the help of modulation technique, master clock module distributes system clock to each slave module. To synchronize slave clocks, the propagation delay is adjusted and the clock phase is aligned by an FPGA chip automatically. Furthermore, an ADC-based method is proposed to evaluate the performance of multi-module clock synchronization simultaneously. The experiments of a prototype system show that slave clocks can be synchronized less than 100 ps over 150 m range. The proposed method is simple and flexible, and it can be used in trigger-less DAQ system and other applications of clock distribution preciously.

Key words Trigger-less DAQ system, Clock distribution, Synchronization, ADC-based evaluation

1 Introduction

For modern particle physics experiments, trigger-less data acquisition (DAQ) system has been put into practice because of the need of reaction multiplicity and trigger flexibility, for example, in the Compressed Baryonic Matter experiment (CBM)[1].

In traditional particle physics experiments, data acquisition and trigger are designed as two parallel processes. Trigger system produces the first level trigger signal using part of the data from the front-end electronics (FEE). Data acquisition system waits for the trigger signal to determine the data to be buffered or discarded. There is a fixed latency which determines the capacity of the buffer between the Level 1 (L1) trigger signal and the originating event time[2]. To ensure the required speed, the Level 1 trigger is implemented by hardware, which is only appropriate for simple and fixed trigger system.

In the next few years, a main physical target of particle physical experiments is to investigate non-perturbative QCD, such as PANDA experiment[3]. The investigation will be done with a high intensity antiproton beam and hydrogen target at the High Energy Storage Ring. Due to the very high interaction rate and very wide physics objectives with different event selection criteria, it was decided to build a trigger-less data acquisition system, where event selection will be done after event building in programmable computer units[3].

In trigger-less DAQ system, each particle hit is autonomously detected and the measured hit parameters are stored with precise timestamps in large buffer pools. Without any external trigger signal, this is a self-trigger mode. Since dedicated trigger data-paths are avoided, all detectors can contribute to event selection decisions at all levels, yielding the required flexibility to cope with different operation modes[1].

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Only with the development of high speed data transmission, real-time data processing and large capacity data storage etc, can such innovative DAQ system be put into practice. Trigger-less DAQ system, more straightforward and more logical than past, will be the development mainstream in the future. For example, trigger-less DAQ will be used in the LHCb experiment[4] and LHAASO WCDA project[5].

The key technique for trigger-less DAQ is clock generation and distribution with precise frequency and phase. Considering the requirement of particle physics DAQ, precise clock means that the reference clock frequencies and phases are deterministic and stable in a system of 1000 channels or more. The skew and the jitter parameter of less than 100 ps are always necessary. The White Rabbit project[6] proposed by CERN provides a choice for this clock distribution. Aiming to develop a distributed timing and data network capable of synchronizing up to 1000 nodes with accuracy less than 1 ns relative to the timing source, the project shows good ability for clock distributing and synchronizing. However, with the usage of switch network and the introduction of transparent clock concept, the complex structure and protocol restricts its application range[7].

In this paper, a clock synchronization method referred to White Rabbit project is proposed. With the help of modulation technique, master clock module distributes system clock to all slave modules. To synchronize all slave clocks, the propagation delay is adjusted and the clock phase is aligned in FPGA automatically. Traditionally, specified equipments are used to evaluate the system synchronization. But for evaluating a system with thousands of channels and large coverage area, traditional observation can't implement easily in practice. In this paper, an ADC-based method is proposed to evaluate the performance of clock synchronization. Do FFT to ADC-sampled points. According to the initial phase, the reference clock skew of ADCs that is slave one can be acquired.

2 Clock Synchronization Design and Evaluation

In traditional particle physics experiment, events are determined by trigger signal. When trigger signal comes, the data in the buffer considered as one event will be sent to the next level. While no trigger signal, the data in the buffer will be discarded. However, in trigger-less DAQ system, with no trigger signal, the timestamp generated by clock becomes the only benchmark. So how to distribute the synchronous and low-jitter clock to all front-end electronics is the key to trigger-less system.

2.1 Clock Distribution and Synchronization

Clock signal transmission can be divided into two forms, baseband and modulated transmission[8]. The common and the most straightforward method is baseband distribution, which transmits the clock signal using either copper cable or optical fiber. The receiver filters the high frequency noises of the input clock with the help of PLL. This technique can be applied to high frequencies and can achieve very high precision. The drawback is however that the distribution tends to be costly, requiring an extra transmission line. This method is usually applied only in the fast timing, for transmission of the most vital signals[8]. For example, this method is put to use in the TOF clock system for BES III[9]. A phase stabilized optical fiber (PSOF) whose temperature coefficient is 0.4 ppm/°C with the temperature range of 10 to 30℃ is used to transfer the RF clock reference from the BEPCII accelerator to the TOF VME64xP crates[9].

Compared to baseband transmission, modulated transmission is a kind of more efficient transport means. In this way, the data encoded by the clock, as the clock information is transmitted simultaneously with the data, so data and clock can be transmitted through the same cable. In the receiver, at the same time of decoding the transmission data, the clock signal is recovered through the clock data recovery (CDR) technology. In order to use the signal jumping edge to recover the clock, 4B/5B or 8B/10B encode is always brought in. Considering the low cost and easy implementation, this form modulated transmission is widely used.

Figure 1 shows the clock distribution and synchronization scheme based on Serializer/ Deserializer (SerDes) and fiber transmission between master clock module and slave module. System clock is embedded into the data stream in master clock module and sent to the slave module. The clock which

has the same frequency as the transmitter clock is recovered in slave clock module. Then the recovered clock of the slave clock module is fed back to master clock module in the same way. There is a transmission delay, which is not fixed affected by factors such as temperature variation, between the recovered clock of slave module and the transmitter clock. In order to realize the clock skew parameter of less than 100 ps, a method referred to WR project is proposed in the prototype system. IEEE1588[10] is used to figure out the coarse delay, while the fine delay is measured based on the digital Dual Mixer Time Difference (DMTD) technique[11] and FPGA-based TDC in the master clock module. According to the fine delay measurement result transmitted to the slave clock module by fiber transmission, the phase of the clock recovered by the SerDes is shifted to synchronize the transmitter clock in the slave module.

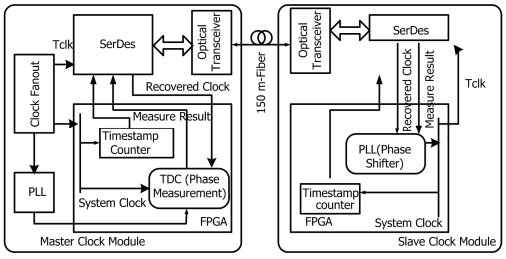

Fig.1 Clock distribution and synchronization scheme.

2.2 Clock Synchronization Evaluation Based on ADC

Since the clocks are synchronous based on the method introduced above, how to evaluate is another key. Because of large coverage area and multi-channels of trigger-less DAQ system, traditional observation using oscilloscope cannot implement easily in practice. In data acquisition system, ADC is used to change analog signal acquired by detectors to digital one. So methods based on ADC to evaluate clock synchronization can implement easily, without extra hardware support. Referred to Ref.[12,13], an ADC-based evaluation method is proposed in this paper.

The synchronized clocks providing reference clock for ADCs are clk1 and clk2 is supported. Using them to sample the same sine signal whose amplitude is A and frequency is f_0, two groups of sampling data $y_1[1{:}N]$ and $y_2[1{:}N]$ can be acquired, in which N is the sampling length.

$$y_1[n]=A\cos(2n\pi f_0T_1+\theta),\ n=1, 2, 3, \ldots, N \quad (1)$$

$$y_2[n]=A\cos(2n\pi f_0T_2+\theta+\Delta\Phi),\ n=1, 2, 3,\ldots, N \quad (2)$$

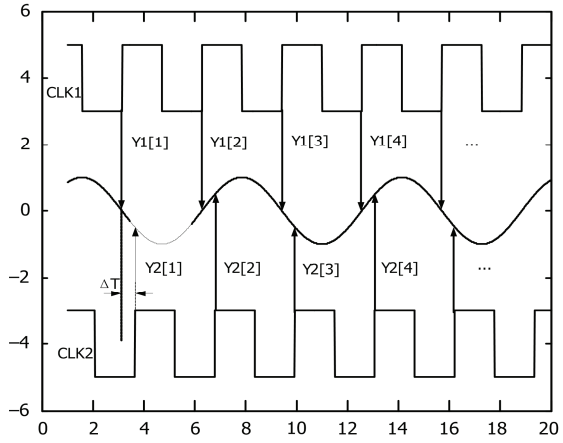

Fig.2 ADC-based sampling diagram.

From Fig.2, the phase difference $\Delta\Phi$ is caused by the clock difference ΔT between clk1 and clk2, so ΔT can be expressed as follows

$$\Delta T = \Delta\Phi/(2\pi f_0) \quad (3)$$

From the analysis above, the key of this test method is to acquire the initial phase of the sampled sine signal from the sampling data. The accuracy of initial phase determines the measurement accuracy

From Ref.[12], the initial phase extraction based on direct DFT has bad estimated accuracy, an improved DFT method called phase difference comparison method is widely used to realize high precision.

Divide the discrete signal $x[n]$ ($x[n]=A\exp[j(2n\pi f_0T_s+\theta_0)]$, $n=1, 2, 3,\ldots, N$) into two parts: $x_1[n]=x[n]$, $x_2[n]=x[n+N/2]$ ($n=1, 2, 3, \ldots, N$). So the initial phase of $x_1[n]$ is θ_0, while of $x_2[n]$ is $\theta_0+N\pi f_0T_s$. Add the same window function to the two signals and do DFT, we can get the formula as follows.

$$X_1(f)=A_1(f)\cdot\exp(j\Phi_1(f))$$

$$X_2(f)=A_1(f)\cdot\exp(j\Phi_1(f))\exp(jN\pi f_0T_s) \quad (4)$$

A_1 and $\Phi_1(f)$ stand for the amplitude and phase at the frequency (f).

$$A_1(f)=A\sin[\pi(f-Nf_0T_s/2)]/\sin[2\pi(f-Nf_0T_s/2)/N] \quad (5)$$

$$\Phi_1(f)=\theta_0+(1-2/N)(Nf_0T_s/2-f)\,\pi \quad (6)$$

From (5), when $f=[Nf_0T_s/2]$, $A_1(f)$ will be the maximum. At this time, the phases for the two DFT sequence are shown as (7) and (8).

$$\Phi_1(f_1)=\theta_0+(1-2/N)(Nf_0T_s/2-f_1)\pi \quad (7)$$

$$\Phi_2(f_2)=\theta_0+N\pi f_0T_s+(1-2/N)(Nf_0T_s/2-f_2)\,\pi \quad (8)$$

f_1 and f_2 correspond the frequency of the DFT spectrum peaks. Define correction coefficient $\delta=\Delta fN/$

f_s ($\Delta f = f_1 - f_0$), for DFT, $-0.5f_s/N < \Delta f < 0.5f_s/N$, we can get the formula (9).

$$\delta_1=(f_1-f_0)N/(2f_s)(-0.5<\delta_1<0.5) \quad (9)$$

Because $x_1[n]$ and $x_2[n]$ are the signals with the same length and frequency, we can get the relationship as follows

$f_2=f_1$, $f_1=k_1f_s/(N/2)=f_0+\delta_1 f_s/(N/2)$ (k_1 is integer, $-0.5<\delta_1<0.5$)

For phase $\Phi_1(f_1)$ and $\Phi_2(f_2)$ are variational with the cycle 2π, support $[\Phi]_{2\pi} \times (-\pi, \pi)$, and $\Phi = 2k\pi + [\Phi]_{2\pi}$ (k is integer), δ_1 can be expressed as follows.

$$[\Phi_2(f_1)-\Phi_1(f_1)]_{2\pi}=[\pi(k_1-\delta_1)f_s/(N/2)N/f_s]_{2\pi}=-2\pi\delta_1 \quad (10)$$

$$\delta_1 = [\Phi_1(f_1) - \Phi_2(f_1)]_{2\pi} / 2\pi \quad (11)$$

From (4) and (8), the value of the initial phase θ_0 can be estimated as follows.

$$\theta_0=\Phi_1(f_1)+\delta_1\pi=\Phi_1(f_1)+0.5[\Phi_1(f_1)-\Phi_2(f_1)]_{2\pi} \quad (12)$$

Do the same operation for discrete signal $y_1[n]$ and $y_2[n]$. Based on phase difference comparison method, initial phase of the two signals can be estimated, from which we can calculate the clock difference between the two clocks.

However, the accuracy of this estimated initial phase is affected by some factors, such as noise of input sine signal and the quantization noise of ADC. Thus the sampled signal can be described as follows.

$$r[n]=x[n]+z[n]n=1,2,3,\ldots,N \quad (13)$$

In the formula, $z[n]$ stands for the noises, including input signal noise, electronics noises, and the quantization noise. Because of the randomness of these noises, the average of $z[n]$ is 0. Supporting the power of $z[n]$ is σ_z^2, the sampling SNR = $10\log(A^2/\sigma_z^2)$. The noises don't satisfy the requirement of Fourier transform. But we can consider the Fourier transform of sampled sequence $z[n]$ as combination of several random variables. So we define the DFT of sequence $z[n]$ in probability sense as follows.

$$Z(f)=c\cdot\exp(j\Phi_z) \ (n = 0, 1, 2,,\ldots, N) \quad (14)$$

The formula (14) is not exact right, which is only right in statistical significance. Because of the randomness, the average of $Z(f)$ is 0 while the variance is $N\sigma_z^2$.

According to Eq.(7) and (8), we can get the phase shown as follows when considering (14).

$$\Phi_{R1}(f_1)=\Phi_1(f_1)-\tan^{-1}[c_1\sin(\Phi_{z1}-\Phi_1(f_1)) /(A_1+c_1\cos(\Phi_{z1} -\Phi_1(f_1)))] \quad (15)$$

Considering $A_1>>c_1$, (15) can be described as (16).

$$\Phi_{R1}(f_1)=\Phi_1(f_1)-c_1\sin(\Phi_{z1}-\Phi_1(f_1))/A_1 \quad (16)$$

For $\mathrm{var}[c_1\sin(\Phi_{z1}-\Phi_1(f_1))]=\mathrm{var}[c_1\cos(\Phi_{z1}-\Phi_1(f_1))]=\mathrm{var}(Z_1(f))/2= N\sigma_z^2/4$, the RMS error of the phase measurement is shown as

$$\sigma_{\Phi 1}=N^{0.5}\sigma_z/(2A_1)\approx N^{0.5}\sigma_z/(2\cdot(N/2)A)= N^{0.5}\sigma_z/NA \quad (17)$$

$\sigma_{\Phi 2}$ are the same as $\sigma_{\Phi 1}$, so the RMS error for the initial phase is

$$\sigma_{\theta 0}=(9/4+1/4)^{0.5}/N^{0.5}\sigma_z/NA=[5/(2N\cdot 10^{(\mathrm{SNR}/10)})]^{0.5} \quad (18)$$

From (18), the RMS error for the initial phase is related to the SNR and sampling length. For the real signal, the RMS error should multiply by $2^{0.5}$.

3 Hardware Design

In order to test the clock synchronization and evaluation methods, a small prototype system which consists of master clock module, slave clock modules and measurement modules is designed. The individual electronics modules are discussed in detail below.

3.1 Master and Slave Clock Module

Master and slave clock module are the basic modules for synchronized clock distribution. Fig.3 shows master and slave clock module diagram, where each master module is responsible for two slave modules.

In master clock module, the system clock 40 MHz generated by clock source module is transmitted to clock fan out module, where they are fanned out to 4 paths: one for the Field Programmable Gate Array (FPGA) as the system clock, another for a PLL to generate a reference clock for DMTD and the others for two SerDes as their Transmission Clocks (TCLK). To maintain the phase synchronization for these fan-out clocks, the three clock paths should be kept in equal length.

Based on modulated transmission method, the system clock can be transmitted to slave module via fibers. In the design, an embedded clock bits SerDes DS92LV16 is chosen, which has a fixed phase relationship between TCLK and recovered clock (RCLK)[14]. With the help of digital DMTD, the clock difference between TCLK and RCLK is zoomed. The resolution of the output phase difference zoomed by digital DMTD is the period of reference clock that is about 25 ns. To measure a time interval about 25ns is easy. An FPGA TDC based on multi-phased clock[15] is

used in our design. The TDC result will be transmitted to slave clock module via fiber transmission. When slave clock module receives the TDC result, the phase shifting operation based on the DCM of Xilinx Virtex -5 FPGA will be initiated. With the help of direct phase-shifting mode of DCM, the phase can be dynamically and repetitively moved forward and backwards by the value of one DCM_TAP which is less than 40 ps[16]. After phase shifter, the shifted clock with the same phase relationship to the system clock in master module is considered as the system clock of slave module (Fig.3).

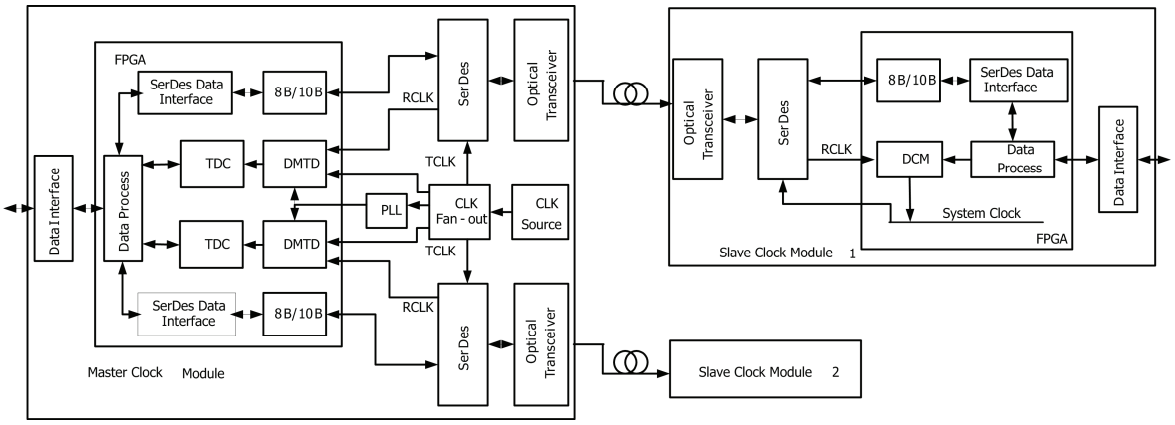

Fig.3 Master and slave clock module diagram.

3.2 Measurement Module

In order to test the clock synchronization performance, measurement module is presented. Because of large coverage area and multi-channels of trigger-less DAQ system, traditional observation using oscilloscope can't implement easily in practice. However, in data acquisition system, ADC is used to change analog signal acquired by detectors to digital one. So methods based on ADC to evaluate clock synchronization can implement easily, without extra hardware support. Known from above, an ADC-based evaluation method has been proposed. So another role of measurement module is to evaluate the ADC-based method.

In this paper, there are three methods to evaluate clock synchronization. The first one is ADC-based evaluation method. This method using ADC to measure clock skew needs to be verified as well. The second one is direct observation using oscilloscope to observe the clock signals directly. This method implements easily in the small prototype system, while hard in practice. However, the measurement phase skew is so small that direct observation will be affected by channel length difference. The third one is indirect observation using DMTD technology to zoom the clock skew that can be observed by oscilloscope with much higher precision. This method implements a litter hard that needs an extra PLL to generate reference clock for DMTD. The latter two methods give a direct proof of clock synchronization, which can be used to evaluate the ADC-based method.

Figure 4 shows the measurement module diagram. Seen from the figure, the slave system clock is divided into three paths: one connecting an SMA test point for direct observation, another linking to DMTD module in FPGA for zooming and the other for PLL reference that provides high precise clock for ADC.

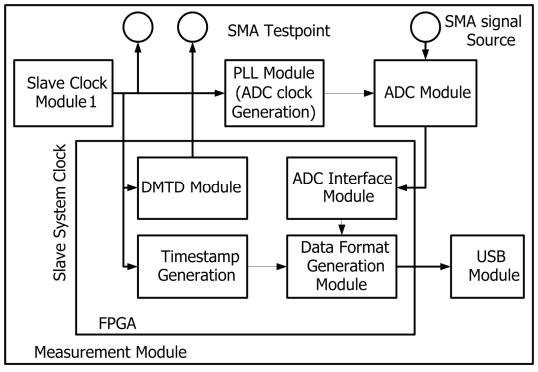

Fig.4 Measurement module diagram.

In order to avoid clock skew brought by PLL for different measurement modules, zero delay PLL is used whose output phase is fixed with input phase. In the direct observation and indirect observation methods, the clock signals of different measurement

modules are observed by oscilloscope via coaxial cables. While in ADC-based method, sine signal generated by signal generator is sampled by ADC via SMA port. In FPGA, timestamp is generated based on the system clock from slave clock module. Data frames generated with sampled data from ADC and precise timestamps are sent to PC to be processed via USB module.

4 Experimental

4.1 Testing Setup

Figures (5) and (6) show the testing setup for evaluating the clock synchronization performance. In the figure, master clock module provides system clock 40 MHz to the system, connecting two slave clock modules via fibers. In order to simulate different transmission delay, two different length fibers 100 m and 200 m are employed. After phase adjustment, the slave clock module outputs the system clock to measurement module. For direct observation and indirect observation methods, the LeCroy oscilloscope Wave Pro 715Zi with 4 channels, 1.5 GHz bandwidth and 20 GS amples per second sampling rate is used to observe the clock skew and jitter. While for ADC-based method, Tektronix AFG3252 is used to provide the 20 MHz sine signal to be sampled by the ADCs, whose sampling clock is 80 MHz and provided by the zero-delay PLL. The sampling results will be sent to PC to be processed further via USB transmission.

4.2 Clock Synchronization Evaluation

There are three methods to evaluate clock synchronization. First, results based on the three methods are measured respectively. Then according to the observation results of oscilloscope, the feasibility of clock synchronization and ADC-based method can be evaluated.

In direct observation method, the difference between the rising edges of slave clocks will indicate the performance of the clock distribution system. Use one channel of the LeCroy oscilloscope Wave Pro 715Zi to observe the master clock as the reference, and another two channels to record slave clocks. To evaluate the method we used, two figures without and with phase adjustment are observed, shown as Figs.(7) and (8). Contrasting the two figures, we can see the synchronization method we used has functioned. Seen from Fig.8, the clock skew between FEE_CLKs is 295.1 ps, while without phase adjustment is 8.334 ns (Fig.7). This result is not exact, which will be discussed in the following.

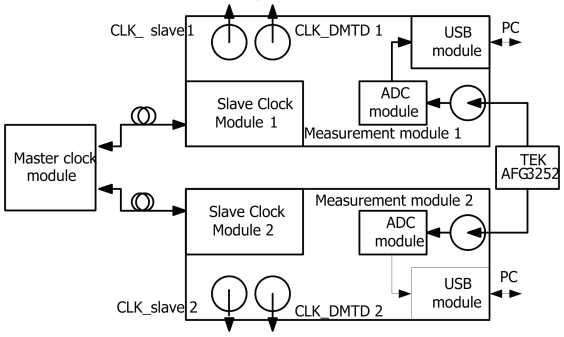

Fig.5 Testing setup scheme.

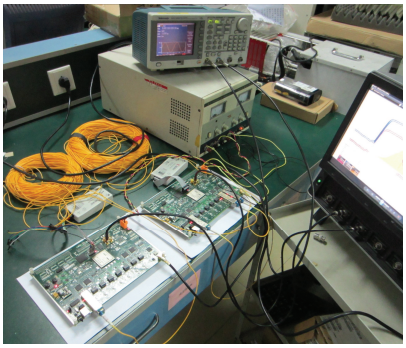

Fig.6 Testing setup for performance evaluation.

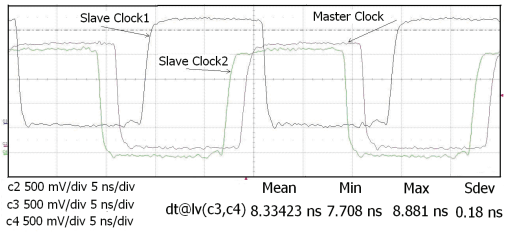

Fig.7 Clock skew without phase adjustment.

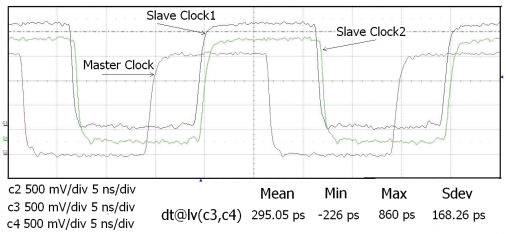

Fig.8 Clock skew with phase adjustment.

In the indirect observation method, the difference between the rising edges of DMTD outputs indicates the time intervals zoomed by real clock skew.

In our design, the amplification factor is 560, which means the observation results 560 times of the real clock skew. On the same observation way as direct method, the results are shown as Fig.9. With phase adjustment, the DMTD output skew is 32.8 ns, 58.6 ps for real-life time difference, less than 100 ps.

In ADC-based evaluation method, two measurement modules sample the sine signal (with frequency of 20MHz) provided by signal source Tektronix AFG3252 at the same time. 8192 points are sampled and divided into two sequences with 4096 points each to do FFT. The results received by PC are processed with the help of Matlab. The initial phase can be achieved shown as Table1. The phase difference of the two sampled signals is 0.0087 (about 0.5°). This means the clock skew of two slave clocks is 69.2 ps.

4.3 Discussion

The results of three methods are 295.1 ps, 58.6 ps and 69.2 ps. But these results may be not very precise. We need further discussion about them.

Direct method result is larger than 100 ps. But considering the effect of the PCB layout and coaxial cable length, that is 2-cm channel length difference will cause 100ps skew difference, this result may not be very precise. But the caused difference is fixed, that can be calibrated. Using the two channels to observe the same clock, we can get the skew difference 237.9 ps shown as Fig.10. After calibration, the direct method result is 57.2 ps. This revised result proves that the clock synchronization method is feasible.

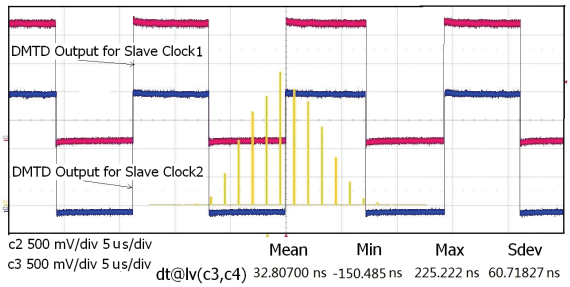

Fig.9 DMTD output with phase adjustment.

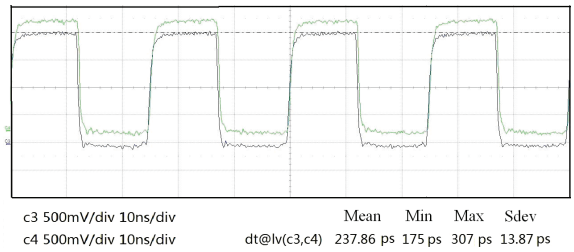

Fig.10 Channel skew difference.

Table 1 Results of ADC-based evaluation method.

Modules	Initial phase1 (first 4096 points)	Initial phase2 (last 4096 points)	Initial phase (8192 points)
Module 1	0.0608	0.1282	0.0271
Module 2	0.0716	0.1433	0.0358

Indirect method employs DMTD to zoom in the clock skew. With the amplification factor 560, the DMTD output will achieve ns range, for example, 32.8 ns as shown in Fig.9. Comparing with it, the effect in direct method can be ignored. Thus indirect method will be precise, as the result 58.6 ps is consistent with the revised result 57.2 ps of direct method. But this method is not easily implemented, for an extra PLL will enlarge the design difficulty.

ADC-based method exhibits good advantage for multi-channel evaluation. From above, we know estimating the initial phase is affected by the SNR and sampling length. In our test, with the help of MATLAB, the SNR of ADC is measured about 60 dB. So the RMS error is about 2.5e-5 for our estimation. That is, the RMS error will bring 0.2 ps clock skew. This result shows that the noises will barely affect the measurement. In order to verify this conclusion, we use MATLAB to simulate this test with the same condition. Generate the tested signal $x[n]=0.5\cos(2n\pi f_0/f_s+\theta_0)$, inside f_0=20 MHz and f_s=80 MHz with sampling length 8192. Add -60dB white noise to $x[n]$, the new signal is $r[n]$. Then do the same operation to $r[n]$ as the ADC-based method. We can get the relationship between estimated initial phase and real initial phase. According to the simulation, we find the effort caused by noises is litter, which proves this method has good performance of noise resistance. However, the ADC-based method result is a litter

larger than others, which may be caused by the two zero-delay PLLs. The devices can't realize accurate zero delay in fact, which can bring a litter skew between two channels. In spite of this flaw, the results satisfy our requirement, which proves that ADC-based evaluation method is feasible.

5 Conclusions

Trigger-less DAQ needs extreme precise global clock. The White Rabbit project proposed by CERN shows good ability for clock distributing and synchronizing, but the complex structure and protocol restricts its application range. In this paper, a novel synchronized clock distribution method is proposed. With the help of modulation technique, master clock module distributes system clock to all slave modules. To synchronize all slave clocks, the propagation delay is adjusted and the clock phase is aligned in FPGA automatically. The experiments of a prototype system show that slave clock skew is less than 100 ps over 150 m range, which proves the feasibility of this clock synchronization method. Furthermore, in order to evaluate the performance of clock synchronization, an ADC-based method is proposed. Compared with the observation results of oscilloscope, this ADC-based evaluation method is feasible and exhibits good advantage for multi-channel evaluation. This method of clock synchronization and evaluation is very simple and flexible, and it can be used in trigger-less DAQ system and other applications of clock distribution preciously.

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