Nuclear Science and Techniques **21** (2010) 366–369

An USB-based time measurement system

QIN Xi[1,2] LIU Shubin[1,2] AN Qi[1,2,*]

[1]*Key Laboratory of Technologies of Particle Detection & Electronics*, *Chinese Academy of Sciences*, *Hefei 230026*, *China*

[2]*Anhui Key Laboratory of Physical Electronics*, *Department of Modern Physics*, *University of Science and technology of China*, *Hefei 230026*, *China*

Abstract In this paper, we report the electronics of a timing measurement system of PTB (portable TDC board), which is a handy tool based on USB interface, customized for high precision time measurements without any crates. The time digitization is based on the High Performance TDC Chip (HPTDC). The real-time compensation for HPTDC outputs and the USB master logic are implemented in an ALTERA's Cyclone FPGA. The architecture design and logic design are described in detail. Test of the system showed a time resolution of 13.3 ps.

Key words HPTDC, USB, Time measurement, High resolution.

1 Introduction

High precision time measurement is of significant importance in particle physics[1]. The HPTDC (High Performance Time to Digital Converter) chip developed at CERN[2] has a time resolution of better than 25 ps[3], and is employed as readout electronics for TOF (Time of Flight) detectors in several particle experiments, such as ALICE[4], STAR[5] and BESIII[6], with high resolution and stable performance.

In some applications, a portable system of fewer channels without a crate is needed for high resolution time measurement. In this paper, we reported the portable TDC board system developed in November 2009.

2 System architecture

Fig.1 shows a schematic diagram of the portable TDC board (PTB) system. The LVDS inputs drive the HPTDC chip, which performs the time-tagging for the signals. An FPGA drives the time values from the HPTDC along with the trigger inputs, and the FPGA and the data acquisition computer is interfaced with a USB controller (CY7C68013).

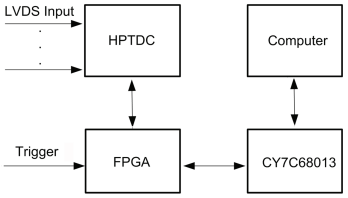

Fig.1 Structure of the PTB system.

2.1 HPTDC

The HPTDC has a high TDC performance designed by the micro electronics group at CERN with a commercial CMOS 0.25-μm technology, and provides a total of 32 time measurement channels for rising and falling edges ("hits") of the input LVDS signals. When the HPTDC receives a "hit", the timing is identified by an 11-bit "coarse time" derived from a coarse counter, and a 5-bit "fine time" is derived from a DLL (Delay Locked Loop) with 32 delay elements, where the rising edge of the clock in the DLL gives an interpolation within the clock cycle. The HPTDC provides the resolution modes of 800, 200, 100 and 25 ps. With the 25 ps mode, only 8 input channels are available. An adjustable RC delay line, spanning the "length" of a DLL delay cell, is optionally used to further increase the time resolution to 25 ps[7]. In our design, the HPTDC chip is used in the very high resolution mode.

Supported by the National Natural Science Foundation of China (Grant No.10775133).

* Corresponding author. *E-mail address:* anqi@ustc.edu.cn

Received date: 2010-05-05

2.2 Logic design in FPGA

The HPTDC chip with a significant non-linearity in the time bins greatly deteriorates the time resolution, and the compensation based on the INL (Integral Non-Linearity) of the chip is necessarily implemented by a LUT (Look-Up Table). As the INL has a repeating pattern at every 1024 bins, a 1024-entry (10-bit depth) LUT is a straightforward choice[8–10]. Because the HPTDC chip may work in the trigger matching mode, the FPGA needs to manage the input trigger signals. Considering the data read out from the TDC in 32 bit data packets and avoiding hit losses, hit rates per channel must be lower than 1MHz when the correlated hits are driven to all 8 channels. Thus the maximum rate of output data for a HPTDC chip is lower than 256 Mb/s. In this design, the FPGA communicates with the USB controller that provides a sufficient data rate up to 480 Mb/s. Fig.2 shows the logic consisting of the trigger logic, LUT, data builder, two 1024×16 FIFOs and USB master logic, which are integrated in a 324-pin ALTERA FPGA EP1C12F324C8.

Configured in trigger matching mode, the trigger logic provides a decision strategy, and drives trigger signal in LVTTL level to HPTDC. The HPTDC configuration is controlled by the FPGA logic using a JTAG port.

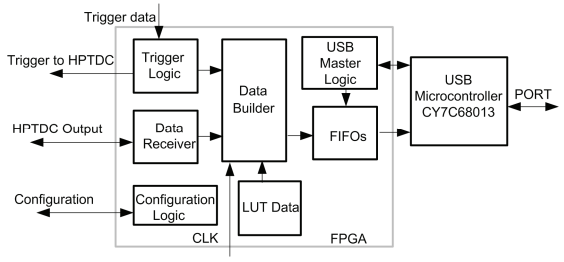

Fig.2 Block diagram of the FPGA logic.

Fig.3 shows the inner logic of data builder providing event-building algorithms for the HPTDC outputs. As the HPTDC output data contain the information of channel and bin, the data builder can locate the corresponding address for the LUT memory, read out the specific compensation data where the raw data from HPTDC are corrected by the compensation algorithm, and the compensated data are pushed into two 16 bit FIFOs.

The USB master logic is responsible for communicating the USB microcontroller with the FPGA, and the software can effectively control the electronics through the USB interface.

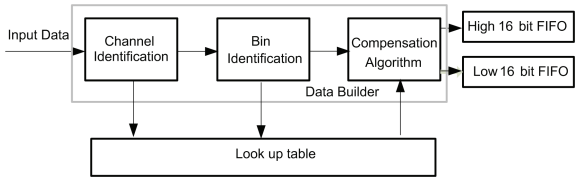

Fig.3 Inner logic of the data builder.

2.3 USB microcontroller

The USB microcontroller, CY7C68013, interfaces the remote computer with the electronics, and acts as a slave FIFO of the FPGA master logic. The USB master logic manages an internal 16-bit wide I/O bus where the USB device is connected, and provides a completely transparent bus mastering and handshaking, thus allowing an easy and straightforward bus to share in both directions.

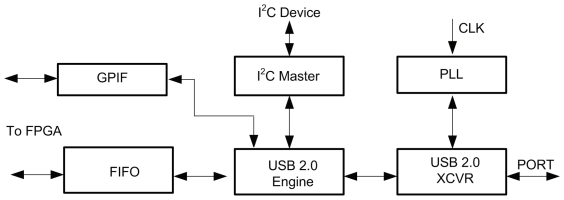

Fig.4 CY7C68013 structure working in slave FIFO mode.

The structure of CY7C68013 structure working in the slave FIFO mode is shown in Fig.4. The chip boots from the I^2C device 24 LC04. The USB2.0 engine is the inner core of the device, and the GPIF module manages the commanding instructions between the USB component and FPGA. A 24-MHz clock is driven to the phase locked loop (PLL) of the chip. With the high speed mode, the clock frequency is doubled to 48 MHz, hence a transmission rate of 480 Mb/s (60 Mbytes/s) of the device.

3 Consideration on the signal integrity

High precision time measurement declares that stringent signal integrity of a circuit may be deteriorated by common-path noise, crosstalk, reflection, ringing, and overshoot, and these give rise to increased measurement error and even wrong results. The PTB system as an 8-layer FR4 printed circuit board is of good signal integrity, with the following design features: (1) large area solid planes

are provided for the ground net to ensure low common-path noise; (2) in order to provide a stable voltage reference and maintain a uniform power distribution voltage on the board, series capacitor arrays are placed between the power terminals and ground planes, hence the low power-to-ground impedance can be ensured; (3) components placing, wiring and resistance matching matching are well considered to minimize signal reflection, overflows and ringing. The PCB Signal Explorer is simulated to obtain good signal integrity, and the system parameters, especially resistance matching, are carefully adjusted before the PCB manufacturing[11].

4 Test results

Fig.5 shows the PTB system. The tests on non-linearity and time resolution were conducted.

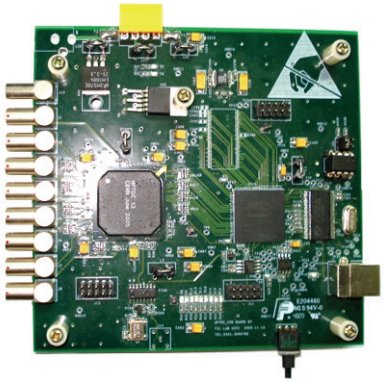

Fig.5 Prototype of PTB system.

4.1 Non-linearity test

The non-linearity of an integrated TDC is often caused by non-ideal topology, non-uniform parasitic reactance, technological spread of the device parameters, and on-chip crosstalk from the logic part of the chip. The DNL (Differential Non-Linearity) is defined as the deviation of output bin size from its ideal LSB (Least Significant Bit), and INL (Integral Non-Linearity), which is a straight line that fits the curve best, is the deviation of the input/output curve from the ideal transfer characteristic.

The non-linearity of the integrated TDC is described by the code-density test method as follows. A large amount of random hits, e.g. a pulse generator with a repetitive frequency quite different from the TDC reference clock, were applied to one TDC channel, and the distribution of measured time stamps were plotted. Any deviation from a flat distribution indicated the amount of the differential non-linearity[8].

Fig.6 shows the DNL and INL curves of one PTB time channel. A simple coarse counter in HPTDC is used to extend the dynamic range to a 25 ns unit, corresponding to 1024 bins, and their pattern repeats at every period of 25 ns. An INL correction table (LUT) can be constructed with only 1024 entries because of the periodic non-linearity over 25 ns, and easily implemented with the FPGA internal memory.

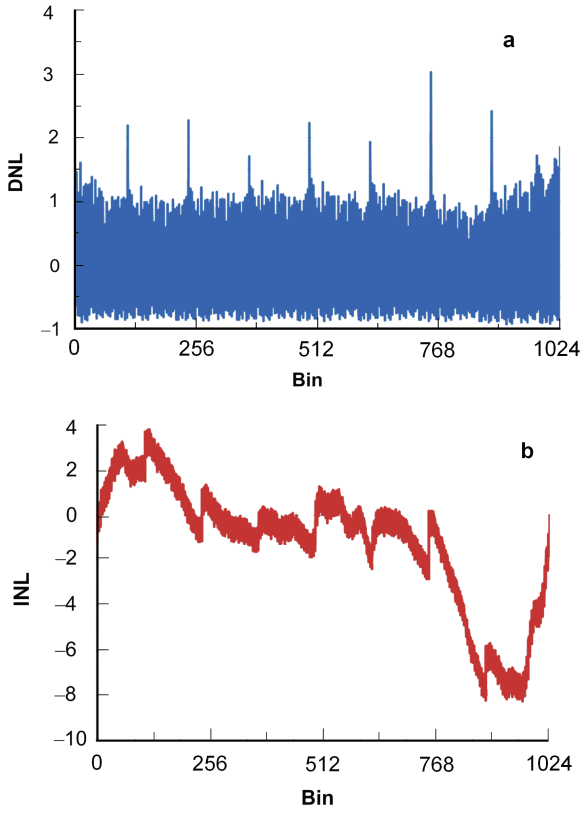

Fig.6 DNL (a) and INL (b) of the HPTDC (Channel 4 of PTB module).

4.2 Time resolution test

The time resolution test was done via the ‘cable delay test’[6,8]. However, an application with a long cable shall result in an attenuation of the input signal, slow the leading edge, and introduce measurement errors. These problems can be overcome by a dual channel arbitrary function generator, AFG3252 manufactured by Tektronix. When Channel A of the generator outputs a pulse, Channel B outputs another pulse, and this allows adjusting the delay between the two pulses and feeding the two outputs to their channels of the

PTB system. As the two pulses are well related with the distribution of the time difference, their RMS (root mean square), divided by the square root of two, is an achievable resolution of single channel for the PTB module.

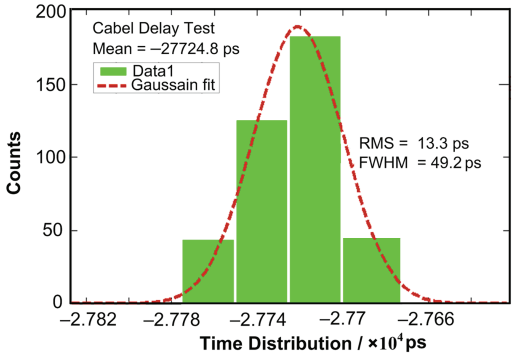

Fig.7 Time resolution of the system.

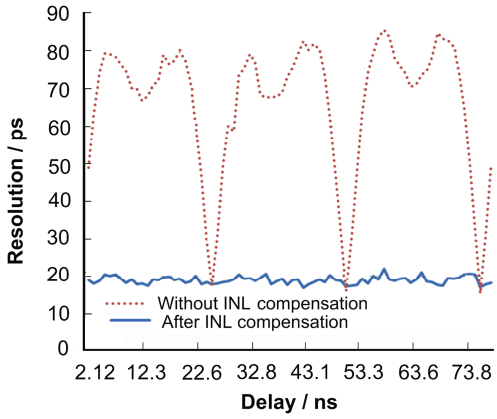

Fig.8 Time resolutions with and without INL compensation.

Once the INL of one HPTDC channel is statistically mapped out, the compensation algorithm is executed in FPGA in real time to minimize the error of time measurement. Fig.7 shows the distribution of one of the time resolution tests after INL compensation, and the 13.3-ps time resolution of a single channel is better than that of 25-ps LSB in HPTDC.

The measured resolution may vary with the time delay of the paired input pulses[12]. Fig.8 shows that the time resolutions for various time delays of 3 to 78 ns greatly enhance after the INL compensation is engaged and periodically repeat at every 25-ns cycle of the 40-MHz clock under the INL pattern of the HPTDC chip. In the whole period, all the compensated RMS values are less than 21 ps.

5 Conclusions

The USB-based time measurement system uses HPTDC as time-tagging, and its data rate is up to 480 Mb/s. Signal integrity in the design is well considered to obtain high resolution of time measurement. When applied in any cases, the system has a better resolution than 21 ps, and the test resolution is 13.3 ps.

Acknowledgments

The authors would like to thank all the FEL collaborators for their support and useful suggestions.

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