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Dose-rate effects of low-dropout voltage regulator at various biases

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Abstract A low-dropout voltage regulator, LM2941, was irradiated by ^{60}Co γ-rays at various dose rates and biases for investigating the total dose and dose rate effects. The radiation responses show that the key electrical parameters, including its output and dropout voltage, and the maximum output current, are sensitive to total dose and dose rates, and are significantly degraded at low dose rate and zero bias. The integrated circuits damage change with the dose rates and biases, and the dose-rate effects are relative to its electric field.

Key words Dose rate effects, ELDRS, Ionizing radiation, LDO voltage regulator.

1 Introduction

Bipolar and linear low-dropout (LDO) voltage regulators, with their merits of low cost, small volume and light weight, are popular in the space applications. Electronic devices under the space ionizing radiation environment suffer from total dose radiation effects that cause performance degradation or even failures. Also, it has been reported widely that bipolar linear circuits, including bipolar voltage regulators, showed dose rate effects[1−10], and for various types of LDO voltage regulators the sensitive parameters changed differently[1−4]. However, fewer reports are available on changes of more than one parameters of an LDO voltage regulator, but performance degradation of an LDO voltage regulator by changing just one parameter in the device hardness assurance testing cannot reflect the device degradation adequately.

The dose-rate effects include the enhanced low-dose-rate sensitivity (ELDRS) and time-dependent effects (TDE)[1,5]. With the ELDRS effect, performance of a device degrades more at low dose rates (LDR) than at high dose rates (HDR) under the same total dose level, and this is a "true" dose-rate effect that cannot be eliminated by the long-term annealing. Therefore, it is worthwhile to study the ELDRS mechanism of an LDO voltage regulator in space, where the dose rates are several orders of magnitude lower than laboratory dose rate.

The TDE difference, under either LDR or HDR, can be eliminated by room-temperature annealing. But the mechanism of the dose rate effects of a bipolar LDO voltage regulator is not well understood. Bipolar integrated circuits (ICs) may exhibit either TDE or ELDRS due to differences in process and structure of the devices[1−6, 11, 12], but fewer devices are reported to exhibit both of the effects.

In this study, dose rate effects of a bipolar LDO voltage regulator (LM2941) under different biases was irradiated at different dose rates in a ^{60}Co γ-ray source. Both TDE and ELDRS in its ICs are observed, suggesting that it may be much difficult to evaluate bipolar devices for a long-term space mission by accelerated ground tests.

2 Experimental

The LM2941 with a band-gap reference (V_{ref}), a bipolar and monolithic and positive LDO voltage regulator, had an adjustable output voltage (V_{out}) of 5−20 V. The dropout voltage (V_{drop}), i.e. the minimum

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voltage between the input (V_{in}) to the regulated output (V_{out}), is 0.5 V at output current (I_{out}) of 1 A[4]. The pulse testing method was used in measuring the electrical parameters so as to limit heating effect on the chip[2]. This was done on an automated testing system of Amida-3001XP from AMIDA technology, INC. The electrical characteristics before and after irradiation, and throughout the annealing procedure, were analyzed, including the conventional line/load regulation, V_{drop}, and maximum I_{out}. The V_{out} of 5 and 15 V were measured by adjusting the external resistor (R_2), as shown in Fig.1.

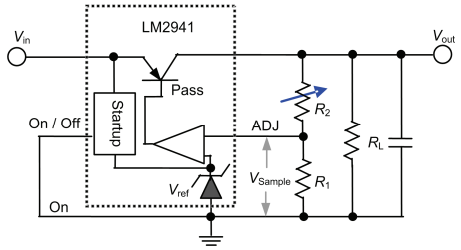

Fig.1 Working bias and test circuit of LDO.

The Chips of LM2941 were irradiated in a ^{60}Co γ-ray source (Xinjiang Technical Institute of Physics and Chemistry), to a total dose of 1000 Gy(Si) at HDR of 0.5 Gy(Si)/s or LDR of 1.0×10^{-4} Gy(Si)/s. Both the dose rates had been calibrated. Post-irradiation annealing the HDR-irradiated chip was conducted, and the annealing time was equal to time of LDR-irradiation time, so as to confirm the time effects of degradation. The parameter measurements were done in either zero biases or working biases (Fig.1). The zero bias was achieved by grounding all the pins related. The working biases was set to the V_{out} =5V by properly configuring the adjustable resistances of R_1 and R_2 with at the input voltage V_{in} =10 V and the load resistance R_L= 200 Ω. The bias conditions were kept during the HDR and LDR irradiation and annealing. The chips were irradiated in a Pb/Al shielding box to minimize dose enhancement.

3 Results and discussion

3.1 The radiation response of sensitive parameters

Fig.2 shows the relative V_{out} response in the LM2941 plotted as function of LDR and HDR total dose, and annealing time. The V_{out} of 15 and 5 V was measured at room temperature by adjusting the R_2. It can be seen that irradiating the chips under working bias at HDR, the irradiation degradation effect is more obviously than irradiating them at LDR, while the low-dose-rate damage is more severe under zero bias. The response of the chips under zero bias at HDR was less than 6% up to 1000 Gy(Si), and almost no change of the response could be observed during the entire period of annealing time, whereas the response of the chips under zero bias at LDR decreased by more than 20% at 800 Gy(Si) . Therefore, the devices exhibit ELDRS under zero bias. Under working bias, the chips irradiated to ≤300 Gy(Si) at HDR and LDR behaved similarly. Above 300 Gy(Si) of the total dose, the response of the chips irradiated at HDR increased with the dose, but decreased at LDR, indicating greater response under HDR irradiation than LDR. However, after the room temperature annealing the chips under working bias at HDR recovered to the same degree of LDR-irradiated chips soon, indicating an obvious TDE. In addition, the V_{out} responses of 5 and 15 V are similar except the last two points at zero bias LDR.

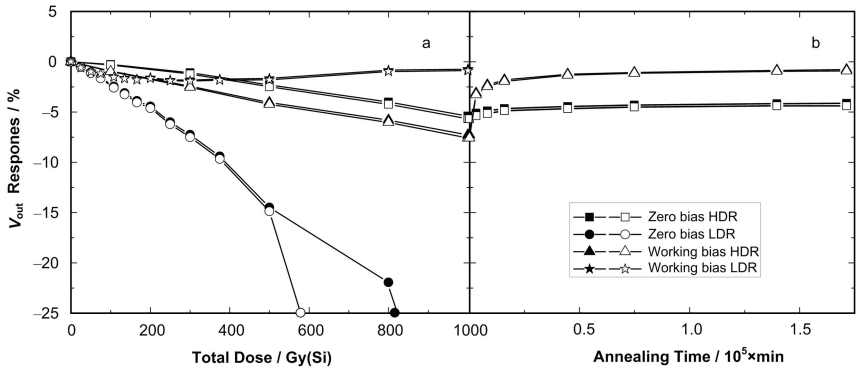

Fig.2 V_{out} vs the total dose (a) and annealing time (b). Solid symbols, I_{out} =50 mA and V_{out}=5 V at V_{in}=10 V (before irradiation). Open symbols, I_{out}=100 mA and V_{out}=15 V at V_{in}= 20 V (before irradiation).

Fig.3 shows that the V_{drop} of the LM2941, another sensitive parameter, has the same dose rate effects at I_{out} = 500 mA. The V_{drop} exhibits ELDRS under zero bias, and TDE under working bias. For the degradation of the maximum output current, the V_{drop} could not be measured after irradiation for some case. And similar behaviors were observed for other key electrical parameters, such as the maximum output current.

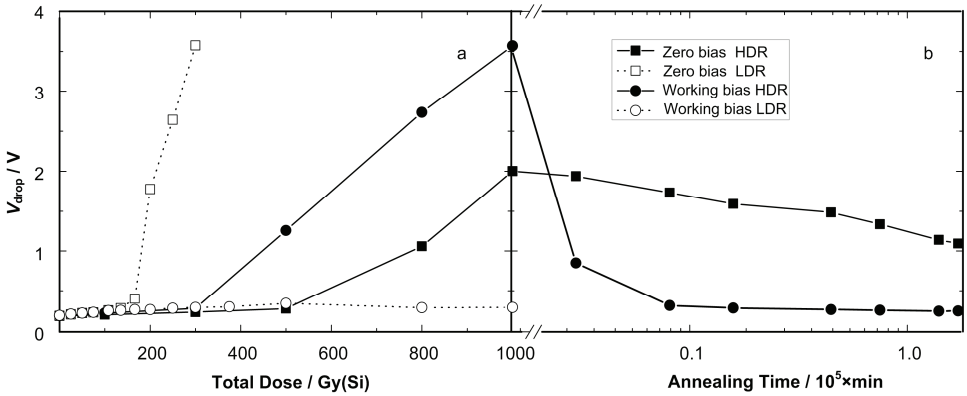

Fig.3 V_{drop} of LM2941 vs total dose (a) and annealing time (b) at I_{out} = 500 mA.

3.2 Explication of the V_{out} response

The LM2941 regulator consists of band gap reference circuit, power output circuit (the pass transistor), and startup circuit. The output voltage V_{out}, which is adjusted by R_1 and R_2 in Fig.1, is decided by Eq.(1). After irradiation, the relative response change (η) of V_{out} is given by Eq.(2).

$$V_{out}=V_{ref}(1+R_2/R_1) \quad (1)$$

$$\eta=(V'_{out}-V_{out})/V_{out}=(V'_{ref}-V_{ref})/V_{ref-} \quad (2)$$

where, V_{ref} is the band gap reference voltage, and the apostrophe denotes the parameters after irradiation.

From Eq.(2), the η of different output voltages may have the same value due to the degradation of the band gap reference, as shown in Fig.2. Under zero bias, however, the output voltage at I_{out} = 100 mA had greater changes at a lower total-dose than that at I_{out} = 50 mA. This kind of inconsistency at LDR may result from the degradation of the maximum output current, which depends on the gain of the pass transistor. Fig.4 shows typical V_{out} response for I_{out} at V_{in} = 25 V measured at LDR under zero bias. Before irradiation, the V_{out} kept constant until I_{out} = 900 mA, but after 1000 Gy(Si) irradiation I_{out} was less than 50 mA. Similar behavior was observed under working bias at HDR irradiation, though the I_{out} could be over 500 mA. After irradiation, the maximum output current kept constant at zero bias HDR or at working bias LDR. Consequently, the I_{out} need to be considered when measuring the V_{out} of LM2941 regulator in its hardness assurance testing.

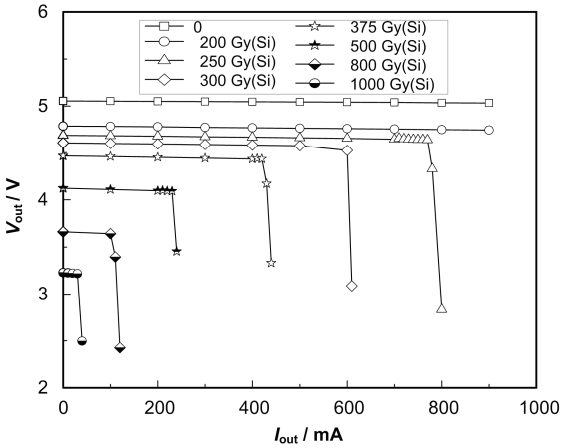

Fig.4 V_{out} vs I_{out} at different total doses of LDR irradiation at V_{in} = 25 V.

Two factors would result in the increase of the dropout voltage V_{drop}. One is the saturation voltage between the collector and emitter of the pass transistor, which causes small increase of V_{drop}. Another is the startup circuit, which may cause large increase of V_{drop}. The output voltage was plotted as a function of the input voltage in Fig.5 for the chips irradiated to different doses under zero bias at low dose rate. We can see that more voltage is needed to start the regulator due to radiation-induced degradation of the

startup circuit. So the large change of the V_{drop} in Fig. 3 may result from the degradation of the start up circuit. It is reported that whatever the degradation of the startup circuit, the maximum output current or V_{ref} is closely related with the radiation-induced gain degradation in the transistors[1−4]. Therefore, dose rate effects are related to degradation of the transistors.

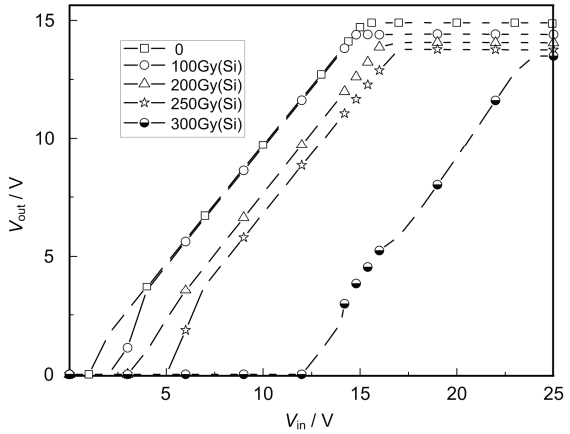

Fig.5 V_{out} *vs* V_{in} at various total dose levels.

3.3 Total ionizing effects

When the bipolar ICs is exposed to ionizing radiations, a great number of electron-hole pairs (e-h) are produced in the screen oxides (SiO_2) on surface of the emitter-base junction[6–9]. The radiation-induced charges increase the base current, and this decreases the current gain. The oxide-trapped charge and interface state are correlated with the radiation-induced defects in the SiO_2, especially near SiO_2-Si interface. After initial e-h recombination, the electrons migrate out of the regions soon, but the holes remain in SiO_2 due to the different mobility. Some holes react with oxygen vacancy to form positive oxide-trapped charges, while others, combining with the H^+ released from the reaction of holes and hydrogen-containing defects, migrate to the Si-SiO_2 interface and react with dangling bonds to create interface state in the interface. Therefore, the base current increases, and the current gain decreases in the transistors, thus degrading the ICs performance. Although both the oxide trapped charge and interface state contribute to the degradation of the devices, their performances are different during the post-irradiation annealing. The oxide-trapped charges can be eliminated by annealing the irradiated chips at room temperature, but the interface state cannot be significantly removed by annealing below 100ºC[10]. From the room temperature annealing in Figs.2(b) and 3(b), the changes are no significant under zero bias, while the degradation rebounds under working bias. It is concluded that the oxide-trapped charges give priority to the damage to the chips under working bias, while the interface state are mainly defects in the chips under zero bias.

It was reported that for thick SiO_2 layers, the dose rate effects change with the biases[6], and we have similar results with the chips under zero and working bias. The electric field maybe increases from zero bias to working bias, thus resulting in the lower e-h initial recombination[12]. Then, the amount of oxide trapped charges increase, and the increased oxide-trapped charges dominating degradation of the chips under working bias, as shown in Figs. (2) and (3).

3.4 Dose rate effects

When the oxide-trapped charges dominant (especially the metastable charges), the device degradation exhibits TDE, or ELDRS otherwise[11]. Under working bias, the oxide-trapped charges dominate the degradation, but the radiation effect can anneal during the long-term LDR irradiation. So the device has less degradation at LDR than HDR, as shown in Figs.(2) and (3).

Under zero bias, less oxide-trapped charges are introduced, so the interface state dominates the degradation of the device. For HDR irradiation, a great number of oxide-trapped charges are produced in the SiO_2 layer at the beginning of the irradiation. The charges generate a strong space field to block the radiation-induced holes and H^+ to reach the Si/SiO_2 interface. Only a few of them can reach the Si/SiO_2 interface to form a few interface states after a long time of irradiation. For LDR irradiation, the rate of electron-hole pair generation is slow, with fewer oxide-trapped charges in the oxide. Thus, the space field is sufficiently weak. On the other hand, the long-term irradiation provide enough time for the holes and H^+ to arrive at the interface, and react with dangling bonds to generate the interface state. Therefore, the LDR irradiated chips have much more interface states than HDR[5–11]. This can explain the ELDRS under zero bias in Fig.(2) and (3).

However, the space charge effects exist under certain conditions[6]. If the time required for holes to transport to the interface (τ_h) is much larger than the time required to build up significant space field in the bulk of the oxide (τ_g), there will be significant space charge effects[6]. As the external electric field increases, the transport time τ_h reduces, while no space charge effects occur when τ_h is smaller than τ_g. This is the reason why we do not consider the space field under working bias.

4 Conclusions

Ionizing irradiations change the V_{out}, V_{drop}, and the maximum output current of the LDO voltage regulator, with the worst effect in the ICs under zero bias at LDR. Under working bias, more device degradation were got at LDR, exhibited ELDRS; while under zero bias, exhibited TDE for the rebound behavior during the annealing following HDR irradiation. The results show that the bias conditions are very important for the LDO voltage regulators in space, and it is necessary to completely evaluate the degradation with different conditions and measure all the key electrical parameters during radiation harden testing.

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