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# Front-end signal analysis of the transverse feedback system for SSRF

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**Abstract** Multi-bunch instabilities degrade beam quality through increased beam emittance, energy spread and even cause beam loss. A feedback system is used to suppress multi-bunch instabilities associated with resistive wall of the beam ducts, cavity-like structures, and trapped ions. A digital TFS (Transverse Feedback System) is in construction at the SSRF (Shanghai Synchrotron Radiation Facility), which is based on the latest generation of FPGA (Field Programmable Gate Array) processor. Before we get such FPGA digital board, investigation and simulation of the front-end were done in the first place. The signal flow was analyzed by SystemView. Construction and optimization of the entire system is our next goal.

Key words TFS, Front end circuits, SystemView, Simulation CLC number TL506

## 1 Introduction

Shanghai Synchrotron Radiation Facility (SSRF) is a 3.5 GeV 3<sup>rd</sup> generation synchrotron light source of high-beam current<sup>[1]</sup>. In its multi-bunch storage ring, vertical instability can be a big problem due to the wall impedance, especially in the sections where narrow-gap insertion devices are installed. To overcome multi-bunch instabilities, a transverse feedback system (TFS) is being developed.

For an acceleration system with N coupled bunches of the beam, their combined behavior can be expressed as a superposition of N normal modes of oscillation, hence N concomitant unstable modes with the system and a need of N parallel narrowband channels to solve the unstable problems. This is not practical, especially for a system of large N, such as SSRF, which will be operated at N=720. Therefore, a time domain bunch-by-bunch transverse feedback system shall be applied to restrain the oscillation of each beam bunch. An all-mode frequency domain system (with uniform gain) is equivalent to a bunch-by-bunch time domain system. The only difference is narrowband *vs*. broadband (all-mode)<sup>[2]</sup>.

# 2 TFS overview

The TFS consists of four main parts:

(1) Wide-band BPM (Beam Position Monitor), which measures the x/y position on bunch-by-bunch basis, but keeps no memory of preceding bunches.

(2) Front-end circuit with bandwidth of 250 MHz, which acts as an analog demultiplexer, extracts the position signal from each bunch, slices every two bunches and converts them into four channels of low frequency signals.

(3) FPGA (Field Programmable Gate Array) signal processor, which has four 12-bit ADCs to sample the four channels of low frequency signals. A 20-tap FIR filter and one turn delay function are implemented inside the FPGA chip, so as to combine and convert the four signal channels into one channel of analog signals by a 500 MS/s DAC.

(4) Vertical/horizontal transverse kickers, which affect corresponding beam bunch with their out-put analog signals amplified by a 150-W amplifier.

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# **3** Signal simulation

First, it is necessary to determine the beaminduced charge on the button electrodes. For relativistic beams, the beam-induced signals can be reduced to a two-dimensional electrostatic problem with the induced charge on the boundary of the electrodes. Therefore, boundary element method<sup>[3-5]</sup> is used to build the BPM output signal.

The signals are processed by SystemView, which provides an environment of comprehensive dynamic analysis for designing and simulating scientific or engineering systems, from analog or digital signal processing, filter design, control systems, and communication systems to general mathematical systems modeling<sup>[6]</sup>.

The beam signals picked up by the BPM are processed into a baseband signal and fed to the digital feedback processor, by which the transverse oscillation signal of each bunch is converted into digital form and filtered by the FIR filters. The kicker is driven by the filtered error signal to damp the bunch motion.

The BPM difference signals are fed to a BPF (Band Pass Filter) of 1.5-GHz center frequency and 250 MHz bandwidth, and are down-conversed to baseband, as seen in Fig.1. The baseband output is split into four channels and delayed to align signals of four consecutive bunches into four parallel signals at a

data rate of 125 MHz. These signals are fed into feedback processor.



**Fig.1** Signal flow of the front-end circuit: signals in 2-ns interval from the 2 button electrodes (a), signals after the BPF with 3-delay lines (b), signals after the mixer (c) and downconversed signals after the 250 MHz LPF (d).

A block diagram of the front-end for SystemVew simulation is given in Fig.2, with four graphic sinks to trace the signal flow in Fig.1.



Fig.2 Functional block diagram of the front-end circuit developed with SystemView.

As shown in Fig.1d, after a 250 MHz LPF (Low Pass Filter), the BPM pulse signals are finally broadened. And transverse oscillation of each bunch can be determined by measuring the peak height of the

output signal. The broadened signals are sent via four channels to the digital processor, where the rising edge of the ADC clock should be set at the peak of the output signal for accurate sampling. Fig.3 shows that the peaks are flattened with the LPF bandwidth of 500 MHz. This is advantageous for AD sampling. The choice of LPF bandwidth is a compromise between maximum flatness of the pulse top and cross-talk between bunches due to long rise/fall times.

Another type of front-end circuit<sup>[7]</sup> is shown in Fig.4 for the principle of the de-multiplexer. The bipolar BPM pulse signal is broaden by a 933-MHz LPF, and mixed with square wave (SW) signal of 125 MHz, one fourth of the RF frequency. The

bipolarpulses mixed with SW at the timing of zero are converted to unipolar pulses, which have low frequency component and are blocked by the LPF, whereas pulses at other time stay in bipolar and pass to the ADC.



Fig.3 Down-conversion signals after the 500-MHz LPF.



Fig.4 The second way of front-end signal processing-jitter effect.

For the two types of front-end circuit, jitter of local oscillator signal from the mixer and the sampling clock of ADC can be a problem to cause reading errors.

For the mixer, the jitter effect is of the second order. The errors can be calculated by Eq. $(1)^{[8]}$ 

$$\sigma_{1} \cong \text{Offset} \times \frac{1}{2} (2\pi \times BW \times \sigma_{\text{ts}})^{2}$$
(1)

where *BW* is the bandwidth of the input signal and  $\sigma_{ts}$ 

is the mixing clock jitter variance.

Assuming *BW*= 1.5GHz,  $\sigma_{ts}$ = 25 ps (the same as the Taiwan Light Source), and the bunch offset =1 mm at the BPM, one has  $\sigma_1$ =27.8 µm.

When *BW*=150 MHz, one has  $\sigma_1$ =23.7 µm For the ADC, the jitter-caused errors is

$$\sigma_2 \cong \text{Offset} \times (2\pi \times BW \times \sigma_{\text{ts}}) \tag{2}$$

 $\sigma_1$  and  $\sigma_2$  are both random errors, plus thermal noise, the total reading error  $\sigma_{\delta}$  is estimated at about 37 µm. The residual motion can be obtained by Eq.(3)

$$\sigma_{\rm x} = \frac{\sqrt{T_0 \tau}}{\tau_{\rm FR}} \sigma_{\delta} = 1.3 \,\mu{\rm m} \tag{3}$$

where  $\tau$  and  $\tau_{FB}$  are total damping time and feedback damping time (we assume  $\tau=\tau_{FB}=1.3$  ms),  $T_0$  is the revolution time, which is 1.44 µs.

## 4 Circuit improvement

Although the above calculations indicate that the minimum reading error requirement of no larger than 10% of the bunch size can be satisfied, improvements of the front-end circuit have been made in laboratory tests.

Whenever the local oscillator frequency is not exactly three times the RF of the storage ring, a low frequency component may be introduced in the pulse mixing. Against such a possibility, the sum signal of four buttons of a BPM is used. It is fed to a network of three delay lines, which have the same structure as the BPF in Fig.2. This provides a local oscillator signal of 3 RF. With such a smart and feasible approach, we do not even need to consider the jitter effect of the mixer, as the local oscillator signal and the beam signals are fully synchronized.

Before the mixer, signal delay was accurately adjusted to make maximum output level after LPF. Figs.5 and 6 show that signals pass through the mixer and LPF from a laboratory test, which indicate that the front-end circuit has achieved its mandate.



Fig.5 Signals after the mixer.



Fig.6 Signals after the 400-MHz LPF.

# 5 Conclusion

The signal's flow of the front-end circuit was analyzed and simulated by a convenient tool SystemView. The effect of clock jitter is also analyzed. An improved circuit is proposed, and it works well in experimental environment. Our next goal is to finish and test the whole TFS system.

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