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A digitalizing board for the prototype array of LHAASO WCDA

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Abstract In this paper, a digitalizing board for readout of PMT signals in the prototype array of WCDA (water Cerenkov detector array) for LHAASO (Large high altitude air shower observatory) is designed. The prototype array is composed of 9 PMTs, including the pulse time and charge measurement from the PMTs, and clock generation and trigger decision. In the digitalizing board, FPGA reconfiguration and data readout *via* VME bus are implemented. Test results show that the performances meet well with the requirements of readout electronics. It has been installed in Yangbajing and tests with the prototype array and DAQ is ongoing.

Key words PMT, Time measurement, Charge measurement, FPGA reconfiguration, VME bus

1 Introduction

A large high altitude air shower observatory (LHAASO) for all sky survey for γ-ray sources is proposed to be built at Yangbajing, Tibet, China[1]. As one of its detector arrays, the water Cerenkov detector array (WCDA) uses 3600 photomultiplier tubes (PMT) to collect the lights generated by charged particles in water. During the pre-research period, a prototype WCDA array consisting of 9 PMTs is being built at Yangbajing to evaluate performances of the detector and electronics[2]. The readout electronics for the prototype array is to digitalize the accurate arrival time of PMT pulse in a wide dynamic range of PMT pulse charge from single photoelectron (S.PE) to 4000 photoelectron. Requirements of the digitalizing board (DB) to readout the nine preamplifiers are as follows.

Time measurement resolution (LSB), <1 ns;
Time measurement precision (RMS), <0.5 ns;
Dynamic range of time measurement, 2 μs;
Multi hit capability, 25 ns;
Charge measurement precision, 10%@S.PE
5%@4000 PE
Trigger readout window, 2 μs.

2 Architecture

Figure 1 shows the scheme of readout electronics system designed for the prototype array. Each coaxial cable of 7-m coming from PMT goes to the preamplifier, and PMT pulses are fed into the DB after amplification. The time and charge measurement of the PMT pulses are processed in DB. The preamplifier has dual gain channels to accommodate large dynamic range of PMT pulses. The charge measurement of PMT_Calib is used for optical calibration. According to signal property, three parts are included in DB: Clock, Analog and Digital. However, the time and charge measurement cross over these parts. Other functions of the DB include mainly the clock generation, on-line reconfiguration of FPGA, Trigger decision and data readout *via* VME bus. Most of the logics are implemented in FPGA, and CPLD controls three parts of functions of the VME interface, local bus between CPLD and FPGA, and configuration of FPGA by means of the serial flash.

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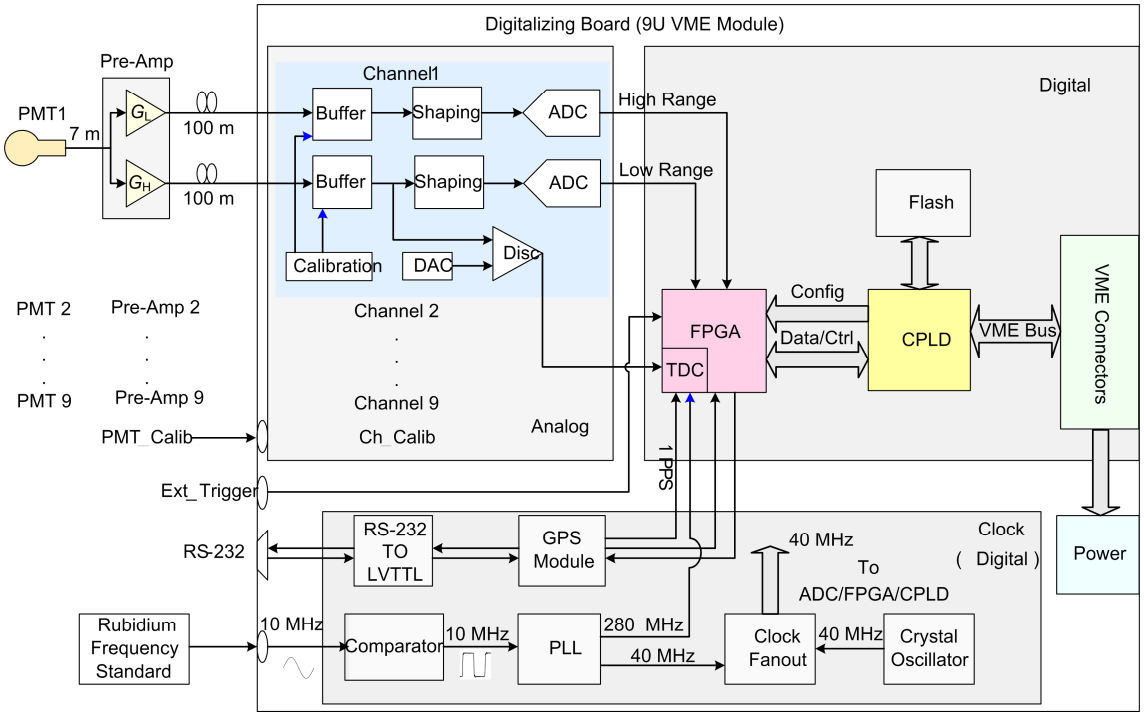

Fig.1 Architecture of the readout electronics for the prototype WCDA array.

2.1 Clock generation

The clock generation uses a high precision rubidium frequency standard as the clock resource. The 10 MHz sine wave coming from the Rb frequency standard is used to synthesize the 40-MHz system clock and 280-MHz sampling clock for the DB. The system clock drives the ADC, FPGA and CPLD, and the sampling clock is used in TDC. For proper working of the PLL (AD9518-3), it must be configured by FPGA, hence the need of a local crystal oscillator before the system clock is available. The scheme of system clock switch is shown in Fig.2.

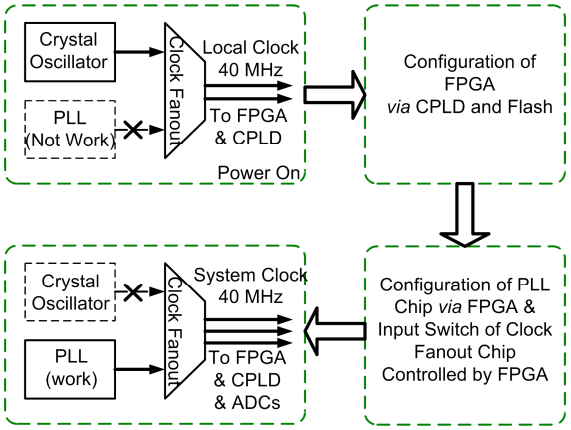

Fig.2 Scheme of system clock switch.

The fan-out chip SY89828L has two input multiplexers and takes four ways of signal as its input. When the DB is powered on, a local clock is fanned out by SY89828 with crystal oscillator as its source. Then FPGA and CPLD are driven by the local clock temporarily. After configuring FPGA and AD9518-3 in sequence, by switching the input of SY89828L from the crystal oscillator to AD9518-3, the system clock is available and fed into FPGA, CPLD and ADCs. The sampling clock works after AD9518-3 is configured.

2.2 Time measurement

In the time measurement, the pulse from the high gain channel of preamplifier is fed into a fast discriminator after transmitted *via* a 100-m high quality coaxial cable. A timing pulse is provided by the fast discriminator when a PMT pulse comes, and its leading edge defines the arrival timing of the PMT pulse. The timing pulse is then sent into the TDC and a time-stamp is produced on detecting its leading edge.

The TDC is implemented in a high performance FPGA, Virtex-4 XC4VLX40-10. Several methods have been used to build TDC in FPGA, such as those based on delay line[3,4] or ring oscillators[5]. Although they are of very high resolution, the TDCs

are not suitable for our design because of their large resource consumption or long dead time.

Sampling the timing pulse with high speed by the flip-flop inside FPGA is another way to build a TDC. By running at a certain clock speed, the output value of the flip-flop can give a time measurement accuracy of the clock period. However, in FPGA, the maximum clock frequency is limited to hundreds of MHz (400 MHz in Virtex-4 XC4VLX40-10)[6], which means that the LSB of TDC is several nanoseconds.

The timing resolution can be further refined using uniformly spaced clock phases. Latching the leading edge of signal to be time stamped with the clock phases allows extracting timing information with sub-clock period accuracy. Quadrature clock can be generated using the Digital Clock Manager (DCM) in FPGA[7]. When the input timing pulse is sampled by the quadrature clock, the results (Q0~Q270) that imply the transition from low to high vary with the location of the pulse (Fig.3). The requirement of the multi-hit capability is 25 ns, so the samples can be pipelined and encoded at the speed of 40 MHz. The 0.893-ns resolution of the TDC's 9 channels is achieved by quadrature sampling the timing pulse at 280 MHz combined with a coarse counter running at the toggle rate of 40 MHz. Using the same method, the best resolution of 0.625 ns is obtained in this FPGA if the quadrature clock is increased to 400 MHz.

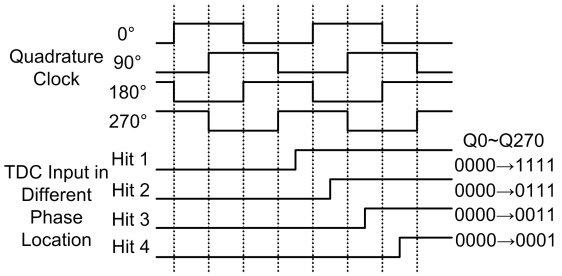

Fig.3 Output bit streams of the quadrature sampling.

The absolute UTC time of an accuracy in second is provided by a GPS module (Motorola M12T) as part of the information of the event. This allows us to correlate observed events with other experiments. The precise one-pulse-per-second (1 pps) of GPS comes once per second with a precision of < 10 ns[8], making it an ideal reset signal of TDC. The dynamic range of TDC is 1 s using 1 pps as its reset signal.

2.3 Charge measurement

For the dynamic range of the charge measurement, the DB circuits are split into the low and high ranges, corresponding to the high and low gain of preamplifier respectively. The PMT used for optical calibration is close to the DB and its dynamic range is small, so one range is enough and no preamplifier is needed. Signals of 19 ways in total shall be measured. The PMT pulse width is very narrow (10–20 ns), if the PMT pulse is sampled directly it is necessary to use a high speed ADCs, which are expensive, and may cause problems of high power consumption and difficulties in saving and processing mass data in time. Thus, the PMT pulse is fed into a Gaussian CR-RC4 shaper circuit followed by an ADC (AD9222) of moderate speed to acquire a series of sufficient samples. The shaper circuit integrates the PMT pulse charge, with an output pulse width of about 300 ns. The pulse peak after the shaping circuit is proportional to the charge of its original pulse coming from PMT[9]. The AD9222, an octal 12-bit 40/50/65 MSPS ADC with serialized LVDS interfaces, is of low cost, low power and small size. In our design (Fig.4), three AD9222 chips digitalize 19 PMT signals after shaper circuit at the speed of 40 MHz. Each data sampled is transformed from serial format to parallel format in FPGA. Once a PMT pulse is detected by TDC in the channel, the data sampled in both ranges are processed to search their peak value in a gate width of 300 ns.

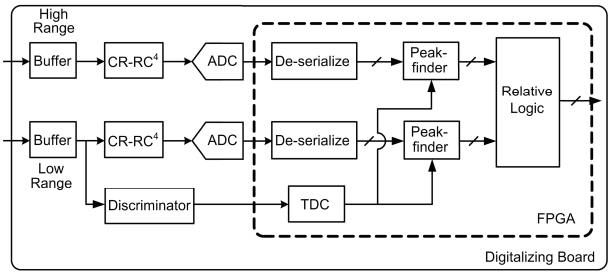

Fig.4 Charge measurement diagram.

2.4 Trigger and dataflow

For in-depth performance check of the prototype array, five trigger modes are designed and implemented in FPGA. Three of the trigger modes are generated based on coincidence of the PMTs, while the external trigger comes from other experiment or detector, and the internal trigger is a period-adjustable pulse produced

by FPGA. The trigger modes can be switched conveniently by the command *via* VME bus. Fig.5 shows the Skeleton dataflow inside FPGA.

When a PMT pulse comes, the charge data is obtained 550 ns later than the time data due to the latency of ADC and the peak finding. The time and charge data are carefully aligned, so as to write them into their dual port Ram (DPRAM) simultaneously. The minimum interval between two triggers is 2 μs, and a second trigger coming in the 2 μs is blocked inside the trigger logic module. The trigger readout window is the same as the minimum interval of triggers, so it is necessary to process the zero compression while writing data into the DPRAM.

A sliding time window provides the start and end addresses of the valid data of a trigger. When a trigger is valid, data inside DPRAMs between the sliding time windows and other information are written into L2 buffers (FIFO_Ch0–9 and FIFO_Misc). The data transfer form L2 buffer to the readout FIFO (L3 buffer) is controlled by the event ctrl module and a token ring. This is designed carefully based on the trigger rate. The minimum and average intervals between triggers are 2 μs and 66.7 μs, respectively. More time margin will be achieved if data of several triggers are piled and transferred to the readout FIFO together. The data in the readout FIFO are sent to CPLD by a local bus and read out by DAQ *via* VME bus. The local bus is only the glue logic between the readout FIFO in FPGA and the VME interface in CPLD, hence no need of memory resource in CPLD. Chain block transfer (CBLT) is supported in VME interface, for future system designs.

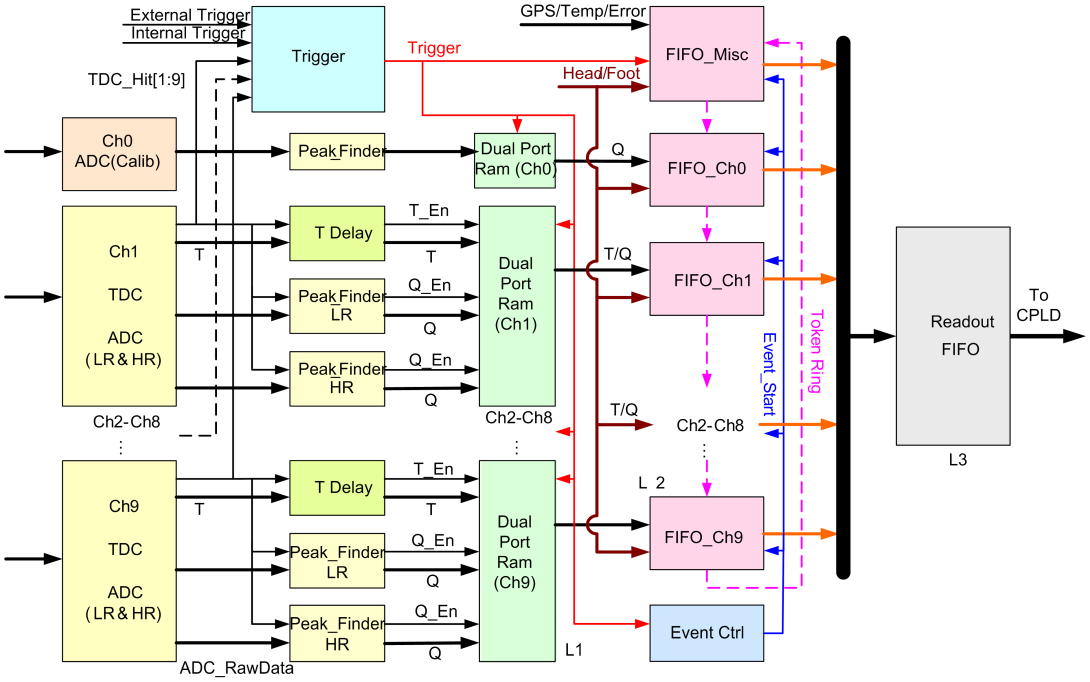

Fig.5 Skeleton dataflow inside FPGA.

2.5 Online configuration of FPGA

The logic in FPGA may need a change in operation, and on-line FPGA configuration provides convenience. Fig.6 shows a scheme of the on-line configuration. CPLD plays an essential role in the process. The VME controller MVME5100 downloads the configuration file through a FTP and writes the file into a non-volatile serial flash *via* the VME bus and CPLD.

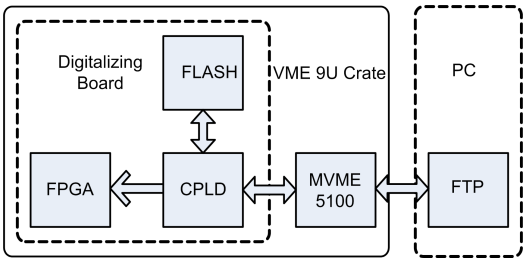

Fig.6 Online reconfiguration of FPGA.

The FPGA has several modes for configuration, and the serial slave mode is chosen[10]. It can be started when the DB is powered up or when CPLD receives a reconfigure command from VME bus or FPGA. During the configuration, CPLD reads content of the flash and put the data and control signals on FPGA's configure ports. The memory size of the serial flash is larger than that of the configuration file, but the exact addresses of the configuration file are not needed. All the data inside the flash can be fed into the FPGA, and FPGA can identify the start and stop positions of the configuration file by the sync and de-sync words inside it. The system of on-line configuration is robust because the VME interface implemented in CPLD remains unchanged after the logic in CPLD is verified in detail. Even if an FPGA does not work properly, a new configuration file can always be burned into FPGA *via* CPLD and VME bus.

3 Test results

Performances of the DB are tested. Combined tests with PMTs and DAQ are performed, too. Fig.7 shows the digitalizing board and one preamplifier, the two curves in the oscilloscope are the PMT pulse before and after shaping circuit.

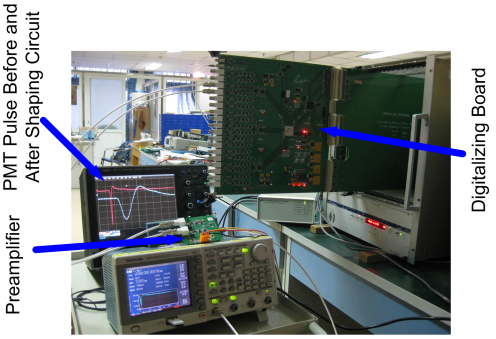

Fig.7 Picture of digitalizing board and preamplifier.

3.1 Time measurement

A Tektronics AFG3252 is used to measure the precision and linearity of TDC circuit. The signal generator, serving as the PMT, sends a pulse into the TDC input. The period jitter of this pulse measured by LeCroy oscilloscope WavePro715z is about 10 ps, which is much less than the LSB of TDC, hence a negligible contribution of the pulse to TDC. A time-stamp is generated when the leading edge of the pulse is detected and all time intervals are obtained by calculating the difference between two consecutive time-stamps.

In Fig.8, the standard deviation (σ) varies with time interval, with the maximum σ of 0.5 LSB or 0.447 ns, and a curve deduced from the ideal condition is plotted[11]. The electronic noise, non-linearity of TDC and metastability introduced by sampling flip-flops increase σ, but in most cases the standard deviations are close to each other. Fig.9 shows the differential non-linearity (DNL) and integral non-linearity (INL) measured by code density test[12], and the maximum DNL and DNL of that channel are < 0.05 LSB. The 9-channel results are listed in Table 1.

The arrival timing difference of 2 PMTs driven by the same laser is measured by DB (Fig.10). The σ of these timing differences is about 2.64 ns, almost 5 times larger than that of the TDC circuit, which means that the contribution of TDC to the precision of the time measurement of PMT pulse is negligible.

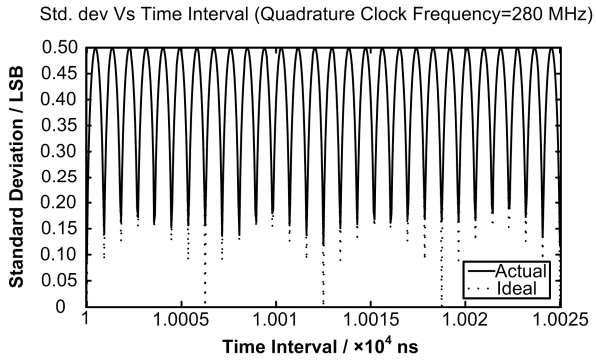

Fig.8 Curve of Standard deviation as a function of the measured time interval, compared with the ideal case.

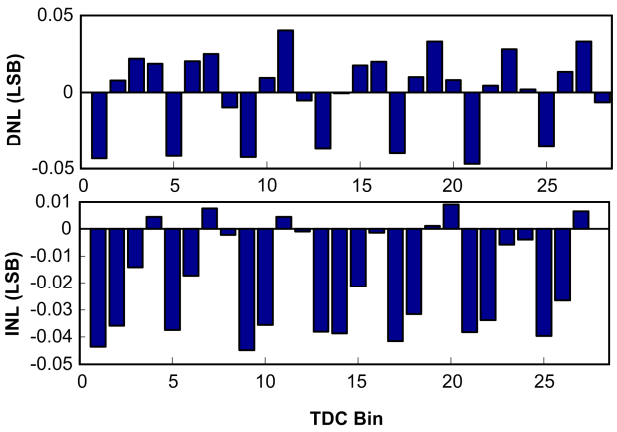

Fig.9 DNL and INL of TDC in channel 3.

Table 1 Maximum DNL, INL and σ of 9 channels

Channels	DNL (LSB)	INL (LSB)	σ (LSB)
1	0.0658	0.0627	0.500
2	0.0472	0.0449	0.500
3	0.0425	0.0415	0.500
4	0.0520	0.0533	0.500
5	0.0428	0.0437	0.500
6	0.0461	0.0495	0.500
7	0.0541	0.0542	0.500
8	0.0346	0.0346	0.500
9	0.0492	0.0549	0.500

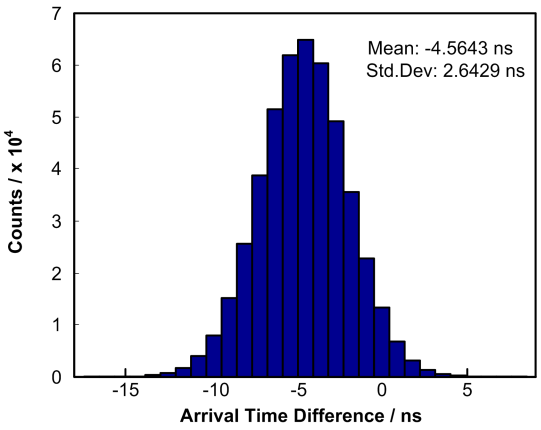

Fig.10 Arrival time difference of two PMTs measured by DB, with preamplifier and 100 meter coaxial cable connected.

3.2 Charge measurement

Electronics performances of the charge measurement are tested by injecting a periodic voltage pulse of variable amplitude into the system of the preamplifier, the 100 m cable and the DB. In each channel, the equivalent charges of these input pulses feeding into low range vary from S.PE to 82 PE, and those of high range change from 80 PE to 4000 PE. Then large amount of peaks are collected to calculate the integral non-linearity and ratios of σ to mean (σ/mean).

Figure 11 shows the test results of one channel, with 100-m coaxial cable attached. The INL of low range and high range are 0.2% and 0.26%, respectively. The ratios in both ranges vary similarly when the charge of the input pulse increases. Intrinsic noise and jitter of the circuit dominate the performance when the input pulse is small, and quantization error of ADC becomes the main factor when the input pulse is large enough.

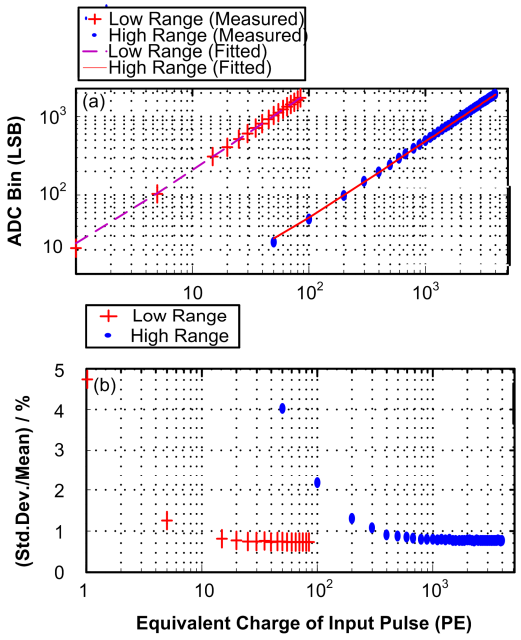

Fig.11 Linearity (a) and σ/mean (b) of Channel 3 in DB, with 100-m coaxial cable attached.

Although adding preamplifiers into the test setups introduces noise and jitter in all the channels, the σ/mean still meet the requirement (Fig.12). Besides, the precision of charge measurement can be refined without changing the structure of the circuit. From Fig.7, the PMT pulse after shaping circuit has two peaks with opposite polarity due to the overshoot of its original pulse. The ADCs are designed to sample both peaks, and only about a half range of the ADC is used for each peak. In our test, only the former peak is measured, so the σ/mean of all channels can be improved by either using the whole range of ADC to measure the former peak or using both peak values as the PMT pulse charge. The capability to measure the S.PE is verified and the single photoelectron spectrum is obtained, as shown in Fig.13.

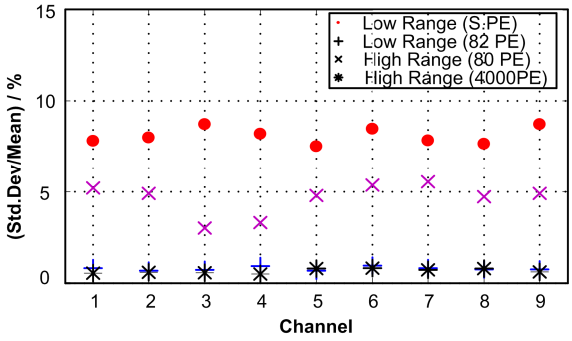

Fig.12 The σ/mean of all channel in DB, with preamplifier and 100m coaxial cable attached.

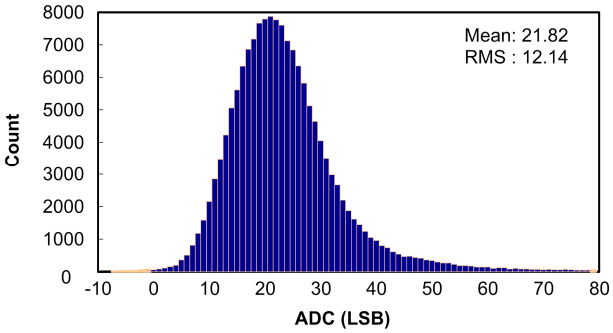

Fig.13 Single photoelectron spectrum measured by DB.

3.3 Other functions

All five trigger models are tested with good results. The data transfer rate of CBLT reaches about 16 MB/s, which is much larger than the actual need. The on-line configuration of FPGA is tested during the running with DAQ. The FPGA is reconfigured when certain amount of data is received, and it has been reconfigured for over 10000 times without any failure.

4 Conclusion

The digitalizing board described in this paper has been designed and tested. TDC with the 0.893-ns resolution is based on the quadrate sampling and implemented in FPGA. The charge measurement obtains the charge of the PMT pulse by means of the shaping circuit and peak finding strategy based on ADC and FPGA. Two ranges are used to achieve large dynamic range of the charge measurement. Test results of the time and charge measurement show that all channels meet the design requirement and can be further refined without changing the circuit's structure. The data transfer rate meets the needs as well. The online configuration of FPGA offers the advantage of flexible firmware upgrade. The whole electronics system including the preamplifiers and the digitalizing board has been installed in Yangbajing and the joint test with the prototype array and the DAQ is ongoing.

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