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LUT-based non-linearity compensation for BES III TOF's time measurement

LIU Shubin[a,b] FENG Changqing[a,b] YAN Han[a,b] AN Qi[a,b,*]

[1] *Key Laboratory of Technologies of Particle Detection & Electronics, Chinese Academy of Sciences,*

[2]*Anhui Key Laboratory of Physical Electronics, Department of Modern Physics, University of Science and technology of China, Hefei 230026 ,China*

Abstract The impact of the integral non-linearity (INL) to the time resolution of HPTDC (High Performance Time to Digital Converter) is presented in this paper. An INL correction method based on look-up table (LUT), is proposed to minimize such INL and improve the time resolution. This scheme is implemented in a single Field Programmable Gate Array (FPGA) device for real-time compensation. The INL characteristic estimation is based on a statistical approach, in which a sufficiently large number of random input signals are measured. The prototype tests show that the deviation for time resolution due to INL can be reduced greatly, from more than 80 ps to less than 20 ps, which can meet the requirement of BES (Beijing Spectrometer) III Time-Of-Flight detector.

Key words INL, Resolution, HPTDC, LUT, Compensation

1 Introduction

The time-of-flight (TOF) detector is a major system for particle identification (PID) in the BES III (Beijing Spectrometer). The detector is composed of the barrel and the end-cap parts. The barrel is of the double layer type, each layer consists of 88 pieces of plastic scintillator bars. The end-caps are of single layer type, with 48 pieces of plastic scintillators at both ends. Particle identification is achieved by measuring the time-of-flight of the high-energy particles generated in the electron-positron collisions. The requirements for the BES III TOF system outlined in 2002 proposal specify a system with <120 ps total resolution, σ_t, that is compact and affordable. This allows particle separation between π and K in the momentum of about 1GeV/c[1]. The TOF readout system is required to handle an amount of 448 PMT outputs with leading time measurement resolution being better than 25 ps.

The BES III TOF electronics performance relies heavily on the HPTDC (High Performance Time to Digital Converter) components specifically designed for the LHC project at CERN, in which they are used to record the time stamp of leading or trailing edge for all the input signals[2]. The HPTDC is fabricated in a 0.25-μm CMOS technology, using a combination of a coarse counter and interpolators. An on-chip PLL (Phase Locked Loop) is used for clock multiplication up to 320 MHz from an external 40 MHz reference, which drives a coarse counter to track the 320 MHz clock periods elapsed since the start of HPTDC. A 32-element Delay Locked Loop (DLL) performs time interpolation down to 98 ps for each bin (LSB). Finally, the finest time interpolation, which is 25 ps for each bin, is achieved by using an on-chip R-C delay line. In addition, it contains more than sufficient buffering capacity to handle BES III data rates.

However, the HPTDC chip exhibits significant non-linearity in the time bins. This is caused by the unequal bin widths in the RC tapped delay lines, unequal bin widths in the DLL, and the coarse clock crosstalk from the logic part to the time measurement part on the same chip. The chip designers suggested that the non-linearity might be due to the power supply

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* Corresponding author. *E-mail address:* anqi@ustc.edu.cn

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and substrate coupling, but efforts made so far in reducing the coupling by changing signal routing and powering scheme have come up with just limited improvements[2]. The tight schedule of BES III did not permit a redesign of the chip, and a flexible alternative approach had to be developed. In BES III TOF readout electronics, in order to achieve the timing resolution claimed by the BES III proposal, a real time correction method, based on look-up table (LUT), was developed to eliminate impact of the HPTDC's inherent INL (integral non-linearity).

2 TDC figures of merit

Similar to ADC (analog-to-digital converter), an ideal TDC can be characterized by LSB (least significant bit) and dynamic range. The LSB specifies the smallest delay that can be discriminated, and the dynamic range corresponding to the largest delay that can be measured[3,4] . Unfortunately, in reality the non-ideality is always present, the non-ideal behavior of the TDC can be characterized by DNL (differential nonlinearity), INL, RMS time resolution, etc.

2.1 Non-linearity and the determination

The non-linearity of an integrated TDC is often caused by non-ideal topology, non-uniform parasitic reactance, and technological spread of parameters of the devices used. DNL is the deviation of output bin size from its ideal LSB value. INL is the deviation of the input/output curve from the ideal transfer characteristic, which is a straight line that fit the curve best. Fig. **1** illustrates the definition of DNL and INL, and we can see that the INL is an integration of DNLs.

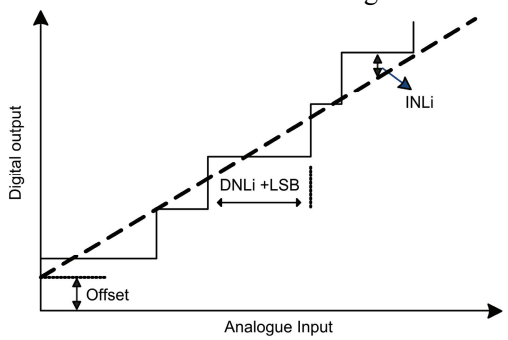

Fig. 1 the definition of INL & DNL.

To determine non-linearity of a TDC, the code-density test method [4,5] is adopted: a large amount of random hits (e.g. from a pulse generator with a repetitive frequency sufficiently different from the TDC reference clock) are applied to one TDC channel, and the distribution of measured time stamps can be plotted. If all TDC bins are uniform, the probability of a pulse arriving in any bin will be the same as that for any other bin, and a histogram of all bins will be flat (except for the statistical variation in the input distribution, which decreases with the number of hits per bin). Any deviation from a flat distribution indicates the amount of "differential" non-linearity.

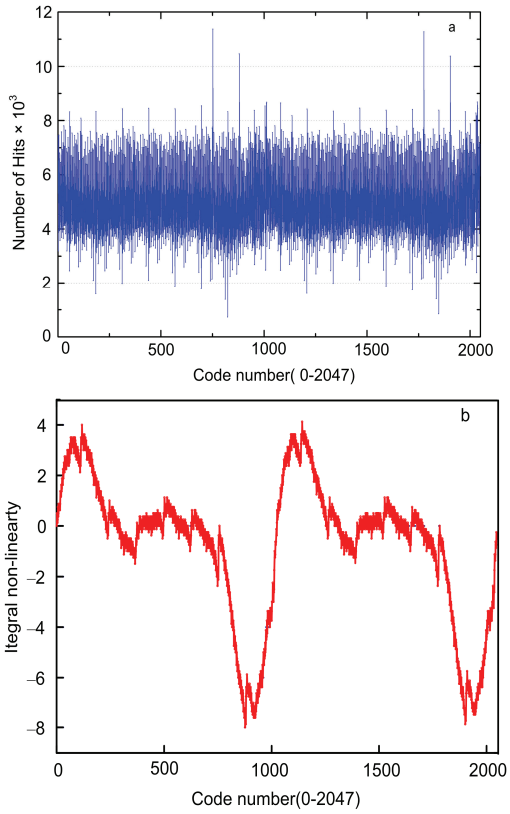

Fig. 2 Test result of code density. (a) Histogram (b) INL .

Fig. **2**a shows the results of a code-density test with 10^7 pulse events acquired from RC and DLL correction values recommended by CERN, plotted for a period of 50 ns (2048 time bins). It is shown that the pattern repeats every 25 ns (1024 bins), as the basic HPTDC architecture is based on a 25-ns unit, using a simple coarse counter to extend the dynamic range[2]. DNL for each bin was extracted from this distribution. And by integrating the DNL derived from the plot, we arrived at an INL shown in Fig. **2**b. The repeating pattern of the non-linearity enables a short way of describing HPTDC's INL characters with only a 1024-entry table (10-bit depth table).

2.2 Resolution and the Determination

The resolution of a TDC is usually definded as a single-shot precision, *i.e.* the standard deviation of the measured data distribution around the mean value when a constant time interval is measured repeatedly.

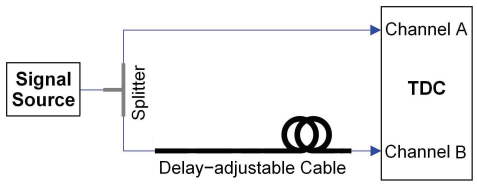

Fig. 3 Schematics for the cable delay test.

To measure the time resolution of HPTDC, the cable delay test approach is used. As shown in Fig. **3**, a pulse generator is employed, and its reference clock is asynchronous to the TDC clock. After the splitter, one output of the pulse generator goes directly to Channel A of the TDC, while the other is fed into Channel B via a delay-adjustable coaxial cable to introduce a delay. The time stamp difference of the pulse pair, and the distribution histogram, can be derived. Given that the individual time stamp difference is constant for all measurements, standard deviation of the measured time difference (RMS_D) shall represent precisely the system resolution, hence a single channel resolution (RMS_S) of $RMS_D/\sqrt{2}$. One of the histogram results for this measurement is shown in Fig. **4**a.

In practical realizations, estimation error of the time measurement is caused not only by clock jitter, ambient temperature variation, and non-ideal (non-uniform) distribution of random pulses, but also by the HPTDC inherent INL, which means the single-shot precision of the HPTDC based on the coarse counter and interpolators is limited by the INL of the interpolators. In Fig. **4**a, the INL spreads the expected time difference peak and affects the time resolution.

3 INL compensation for resolution improvement

It is believed that this problem comes from substrate coupling from the digital logic part on the same chip and it can only be significantly improved by a complete redesign using a more sophisticated digital library with lower substrate coupling[2]. However, an alternative solution had to be found to minimize the impact of HPTDC's INL for the TOF readout electronics. A feasible method is to compensate the INL of HPTDC.

The principle of INL compensation is as follows: a sample that falls in a certain bin of the TDC is corrected by subtracting the INL value of that bin. As shown in Fig. **1**, if the TDC output code of the measured sample is $C(i)_{TDC}$, and the $INL(i)$ of code $C(i)_{TDC}$ is known, then the ideal value of the sample will be denoted by $C(i)_{IDEAL} = C(i)_{TDC} - INL(i)$.

With a code density test prior to the cable delay test, we were able to obtain all the codes' INL value. After the INL compensation, the histogram result is shown in Fig. **4**b, which has an RMS value of about only 16 ps, the improvement is obvious.

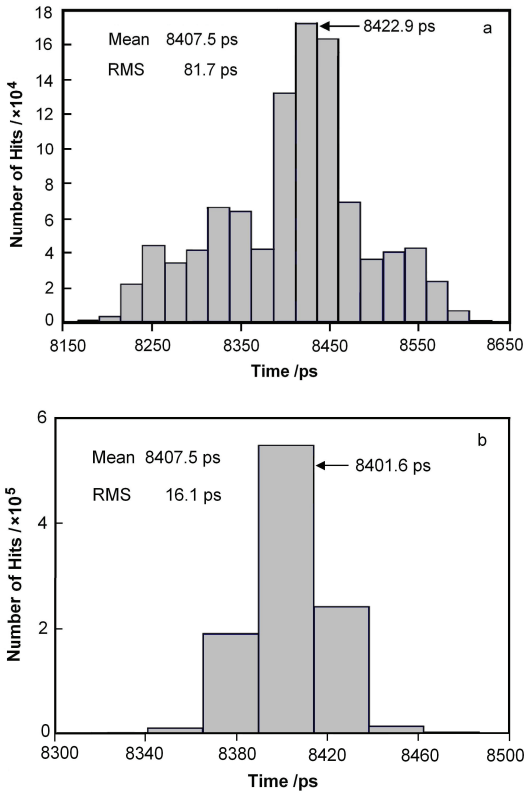

Fig. 4 Cable delay test for HPTDC's resolution. Test result before correction (a), and test result after correction(b).

4 LUT-based INL compensation in BES III TOF FEE

As discussed before, if the INL of the TDC is known in the time interval measurement, the INL can be used for improving the single-shot precision. The INL data is stored in a look-up table (LUT), in which each cell represents the measured INL error for each TDC bin.

Because of the periodic non-linearity over one HPTDC clock period (Fig.2b), the INL values from the plot like Fig. **2**b were used to construct an INL correction table with only 1024 entries in a FPGA (Field Programmable Gate Array), as an array of correcting vectors. The compensation mechanism implemented in the FPGA performed the INL error correction, with $S(i)_{\mathrm{INL}}$ being the interpolator INL values, which was picked from the LUT addressed by the current interpolator values $V(i)_{\mathrm{TDC}}$. Every TDC output was compensated with the formula of $V(i)_{\mathrm{Comp}} = V(i)_{\mathrm{TDC}} - S(i)_{\mathrm{INL}}$. The compensation in the FPGA could release CPU power in the data acquire (DAQ) system from table searching and calculating.

Table1 The test result of HPTDC resolution.

~Cable delay /ns	Resolution before compensation /ps	Resolution after compensation /ps
…	…	…
19	61.6	12.7
21	58.9	14.1
22	54.0	14.8
23	44.4	13.1
24	31.5	15.1
25	16.0	14.9
26	29.7	14.1
27	44.8	13.4
28	53.3	15.6
29	59.6	14.5
30	62.1	15.7
31	60.8	14.2
32	60.6	14.6
33	60.2	15.8
34	55.8	14.4
35	56.0	16.4
36	56.8	15.6
37	54.5	16.8
38	55.8	17.3
39	57.5	16.0
40	57.5	18.3
41	60.0	16.4
42	62.5	17.7
43	64.7	18.1
44	63.0	17.8
…	…	…

A prototype circuit was designed to verify the real-time compensation method. Part of the cable delay test results are shown in Table1, with a series of cable delays ranging over several times of the INL period (25 ns). Since the basic HPTDC architecture is based on a 25 ns unit, using a simple coarse counter to extend the dynamic range[2], its performance repeats with a period of 25 ns. As the signal attenuation due to long cable worsens the resolution, we selected the results with relatively short cables for representative without losing the generality.

From Table 1, most of the resolution data before compensation cannot meet the requirement, with the single-shot precision being worse than 25 ps, but the compensation algorithm in the FPGA improves the resolution to better than 18.3 ps for the worst case.

Fig. **5** shows the testing results, with or without compensation. The mean RMS value of these measurements without compensation is 53.7 ps, while it is 15.5 ps after compensation.

As the crosstalk comes from the 40 MHz clock, which is also the time reference of the HPTDC, the INL has a quasi-static characteristic from channel to channel and from chip to chip. Therefore, it can be compensated for by a simple look up table using the INL bits of the measurements as an entry (1024 entries in HPTDC's very high resolution mode). In others tests, which were operated in STAR[6,7], a performance comparison were done between uniform INL table for all HPTDC chips and a specific INL table for each HPTDC chip, and the time resolution results by the two methods agreed with each other within 10%. Since obtaining an individual INL correction for each chip can be done in parallel, and the INL correction tables are relatively small, we decided to use a specific INL correction for each chip.

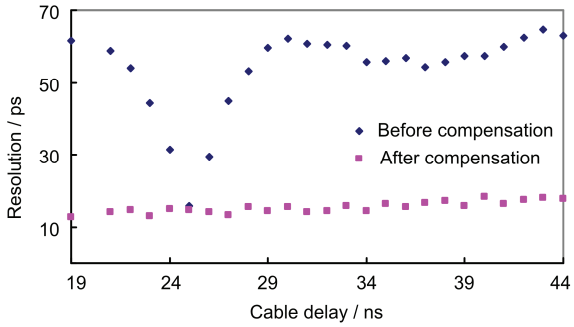

Fig. 5 Resolution *vs* cable delay.

The real-time LUT-base INL compensation algorithm implemented in the FPGA has been employed in the readout electronics modules for BES III TOF detector. A stand-alone cosmic and laser diode (LED) test for the module, cooperating with the realistic scintillator and PMT, has been done in the Institute of High Energy Physics, Chinese Academy of Sciences. The result shows that the whole apparatus achieves the performance that "the intrinsic contribution of readout electronics' time resolution is better than 25 ps, … stable performance with long term working; meet the requirements of BES III TOF detector's readout electronics"[8]. After commissioning, the mass production including 15% spares for the modules has been processed, followed by the burn-in work. The modules installed to the BES III in November, 2007.

5 Conclusion

The time resolution of the HPTDC which is based on a coarse counter and interpolators is limited by the INL of the interpolators. The INL of the interpolators is pre-measured and be stored in a look-up table (LUT) and used as a correction vector in the measurement result calculation to improve the single-shot precision to better than 25 ps.

The commissioned TOF readout electronics modules with the proposed real-time LUT-based INL compensation are assembled to the BES III for in-situ cosmic ray and beam collision test since the end of 2007. The electronics have been reliably operating with the detector since then. The recent results show that the whole TOF detector system provides a barrel time resolution less than 90 ps, which includes the contribution of not only the TOF readout electronics, but also the intrinsic TOF detector time resolution, uncertainties of bunch time and length and extrapolation on MDC track construction etc. [9]

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