Design and test results of a low-noise readout integrated circuit for high-energy particle detectors

ZHANG Mingming CHEN Zhongjian* ZHANG Yacong LU Wengao JI Lijiu

Key Laboratory of Microelectronic Devices and Circuits, Institute of Microelectronics, Peking University, Beijing, 100871, China

Abstract A low-noise readout integrated circuit for high-energy particle detector is presented. The noise of charge sensitive amplifier was suppressed by using single-side amplifier and resistors as source degeneration. Continuous-time semi-Gaussian filter is chosen to avoid switch noise. The peaking time of pulse shaper and the gain can be programmed to satisfy multi-application. The readout integrated circuit has been designed and fabricated using a 0.35 μm double-poly triple-metal CMOS technology. Test results show the functions of the readout integrated circuit are correct. The equivalent noise charge with no detector connected is 500–700 *e* in the typical mode, the gain is tunable within 13–130 mV/fC and the peaking time varies from 0.7 to 1.6 μs, in which the average gain is about 20.5 mV/fC, and the linearity reaches 99.2%.

Key words High-energy particle detectors, Readout circuit, Low noise, ASIC

1 Introduction

High-energy particle detectors are widely used in elementary particle physics experiments, nuclear physics, space applications and medicine[1]. A readout circuit converts charge signals of the detector into voltage signals. As the detector array grows in size, multi-channel Application-specified Integrated Circuit (ASIC) becomes the mainstream implementation of readout circuits.

The output of readout circuit is proportional to the energy deposited in the detector by the impinging particles, but this kind of signal is small, hence the need of minimizing the noise of the readout circuit. The solutions used to include the Bipolar Junction Transistor (BJT) and Junction Field Effect Transistor (JFET) circuits, due to their inherent low noise performance. The CMOS integrated circuit has been gaining attention because of its high density, low cost, and low power consumption [2]. However, noise performance of an MOS transistor is much worse than that of BJT and JFET, and it is a challenge to design low-noise CMOS readout ASIC[3–6].

In this paper, a low-noise CMOS readout ASIC is developed. It consists of a charge sensitive amplifier (CSA), a pulse shaper with adjustable peaking time from 0.7 to 1.6 μs and an output buffer. Many low noise techniques were adopted in designing each block of the circuits to reduce the noise of this readout ASIC. Seven modes with dynamic range and peaking time were designed to meet the needs of applications.

2 Circuit structure

Topology of the readout ASIC is shown in Fig. 1. The circuit contains two input connections at the CSAIN point. The DET connects the detector with the readout ASIC, while V_{test} is used for testing the ASIC. A pulse voltage of V_{test} will be equivalent to a charge pulse generated in the detector. The charges are integrated on the feedback capacitor C_{f}, and the CSA output will rise to a voltage related to C_{f}. The feedback resistor R_{f} is used to discharge C_{f} against saturation of the CSA. The pulse shaper, which is a CR–$(\text{RC})^2$ type filter, shapes and filters the CSA output, so as to suppress the noise and increase the signal-to-noise ratio (SNR). An additional gain is provided by the shaper. One can

Supported by the National Natural Science Foundation of China (No.40704025), and Ye Hongfei for his help with the measurement of the chip.

* Corresponding author. *E-mail address:* chenzj@pku.edu.cn

Received date: 2009-08-24

make a choice of the 16 gains by using a four-bit code under a certain peaking time. The buffer (BUF) was designed for circuit test.

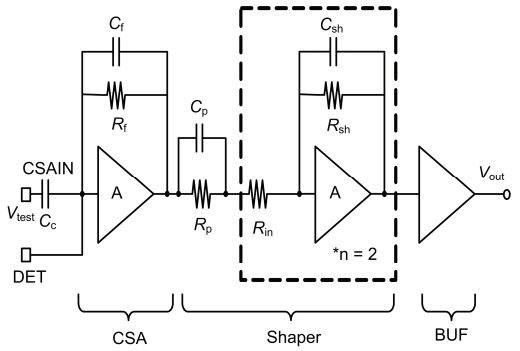

Fig.1 Topology of the readout ASIC.

2.1 Charge sensitive amplifier

Single-ended folded cascade amplifier is usually selected for the CSA because of its higher gain and broader bandwidth. A single-ended amplifier has fewer transistors and causes less noise than a differential amplifier. Fig. 2 shows schematics of the CSA with the bias circuit.

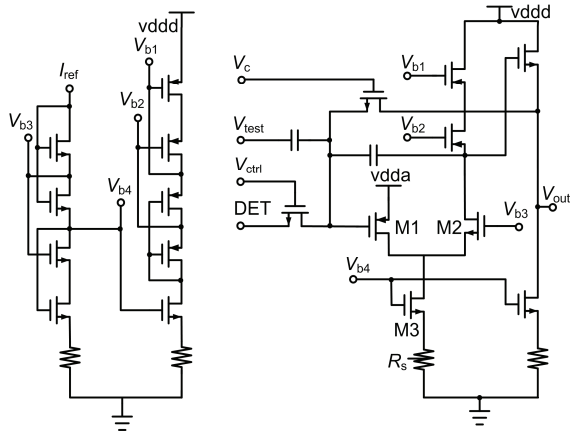

Fig.2 Schematics of the charge sensitive amplifier.

The input charges are accumulated on the feedback capacitor C_f. The CSA output, V_{CSA}, is given by Eq. (1),

$$V_{CSA}(s) = -(Q_{in}/C_f)[1/(s+1/\tau)] \approx -Q_{in}/C_f \qquad (1)$$

where, Q_{in} is the input charge and $\tau = R_f C_f$. The resistor R_f is used to discharge C_f for avoiding the saturation of CSA and supplying a DC path to ground. Without it, the output voltage is directly proportional to input charge and in the inverse ratio of C_f.

The CSA is located at front of the circuit, so the CSA has a great influence on the noise performance[3], and reducing its noise is important. Noise analysis of this circuit indicates that much of noise aroused by M1. A large transconductance of M1 would degrade the input-referred noise voltage [4]. The width, length and bias current of M1 should be optimized. Besides, the noise of other transistors cannot be totally neglected, especially that of the tail circuit source, such as M3, which has lager bias current than M1. We chose PMOS for M1, because NMOS has much more flicker noise than PMOS in CMOS technology. But M3 is NMOS with larger current than M1, so both the flicker noise and thermal noise of M3 are not negligible. To reduce the noise brought by M3, a resistor is used as source degeneration component[5]. In this way, the equivalent transconductance of M3 is reduced, so is the input-referred noise.

Without the resistor, the input-referred noise voltage brought by M3 is given by Eq.(2), which contains both flicker noise and thermal noise.

$$V_{n,3}^2 = \frac{g_{M3}^2}{g_{M1}^2}\left(\underbrace{\frac{8kT}{3g_{M3}}}_{\text{Thermal}} + \underbrace{\frac{K_f}{W_3 L_3 C_{ox} f}}_{\text{Flicker noise}}\right) \qquad (2)$$

where, g_{M1} and g_{M3} are transconductance of M1 and M3 respectively, k=1.38×10^{-23}J/K is the Boltzmann constant, T is absolute temperature, W_3 and L_3 is channel width and length of M3, K_f is flick noise coefficient, C_{OX} is gate oxide capacitance per unit area, and f is frequency.

With the resistor, the input-referred noise voltage brought by M3 and its source resistor R_s can be

$$V_{n,3}^2 = \frac{g_{M3}^2}{g_{M1}^2(1+(g_{M3}+g_{Mb3})R_s)^2} \times \left(\underbrace{\frac{8kT}{3g_{M3}} + 4kTR_s}_{\text{Thermal noise}} + \underbrace{\frac{K_f}{W_3 L_3 C_{ox} f}}_{\text{Flicker noise}}\right) \qquad (3)$$

where, g_{Mb3} is bulk transconductance of M3.

From Eqs.(2) and (3), the flicker noise is reduced by a factor of $[1+(g_{M3} + g_{Mb3})R_s]^2$. The thermal noise is reduced, too. A bigger R_s would be preferred for better noise performance, but it brings larger voltage drop and takes larger area.

2.2 Pulse shaper

Continuous-time filter is chosen to avoid noise brought by switching on and off. Semi-Gaussian shaper is widely used[7–9] as a good compromise among noise performance, counting rate and circuit complexity. The CR–$(RC)^2$ filter reshapes the pulse voltage into a semi-Gaussian shape, to suppress pileup and facilitate pulse height recording, while it filters high frequency and low frequency noise. Besides, the shaper has influence on the noise performance.

Consulting from Fig.1, the transfer function of the shaper from the CSA output to the shaper output is given by

$$H(s)=\frac{1+sC_pR_p}{1+R_p/R_{in}+sC_pR_p}\left(\frac{R_{sh}}{R_{in}(1+sC_{sh}R_{sh})}\right)^2 \quad (4)$$

There is R_{sh} and C_{sh} influencing the time constant. R_p and C_p form a high pass filter to cancel pole caused by R_f and C_f, with $R_pC_p = R_fC_f$. Let $R_pC_p/(1+R_pR_{in}) = R_{sh}C_{sh}$, a peaking time $nR_{sh}C_{sh}$ is achieved. The DC gain of the pulse shaper, which affects the total gain, is expressed as $(R_{sh}/R_{in})^2/(1+R_pR_{in})$. So changing R_{sh} and C_{sh} can change peaking time and DC gain. Fig. 3 shows the first stage of the pulse shaper. To meet the need of applications, the readout IC uses adjustable resistor and capacitor to change the peaking time and DC gain.

3 Test results

The readout ASIC was designed in a 0.35 μm double-poly-triple-metal (DPTM) CMOS and tested on the Verigy 93000 platform. A photomicrograph of the readout ASIC is shown in Fig. 4. A pulse voltage with a repetition period of 20 μs was applied at V_{test} in Fig. 1 to simulate the charge pulse at CSAIN.

3.1 Appropriate discharge time

The input pulse voltage amplitude applied at V_{test} is set as 0.1 V and the gate voltage V_c of the feedback MOS resistor R_f is adjusted to tune the decay time constant of CSA. Fig. 5 shows the output waveform of CSA with different V_c. The decay time increases with decreasing V_c, but the noise decreases with V_c. As a compromise between the discharge time and noise, we chose V_c = 2.25 V for the following test. With this value a suitable leaking time can be achieved.

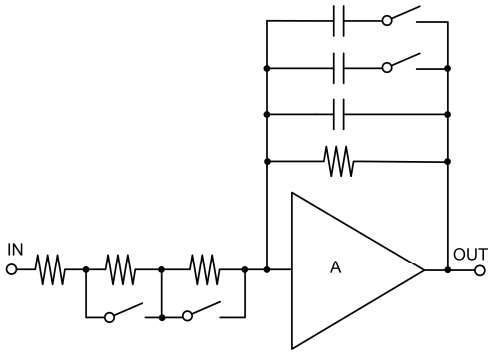

Fig.3 The first stage of pulse shaper.

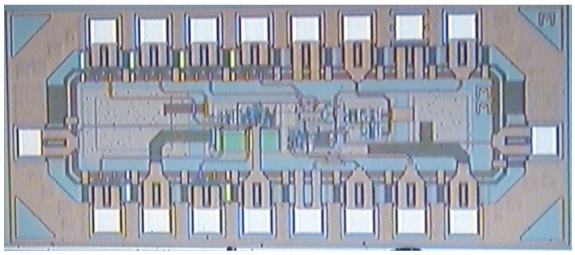

Fig.4 Chip photomicrograph of the readout ASIC.

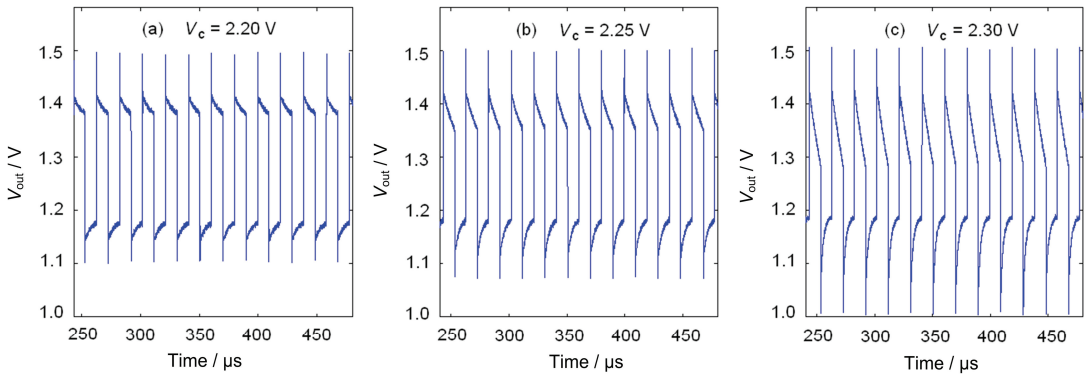

Fig. 5 Output of CSA with different V_c.

3.2 Output of shaper

Output waveform of the shaper at V_c = 2.25 V is shown in Fig. 6. A peaking time of 1μs and 0 dB gains were provided by the pulse shaper. The average gain of the ASIC is about 20.5 mV/fC. For this circuit is designed to deal with current pulse signal flowing from CASIN to ground, only the positive pulse is valid.

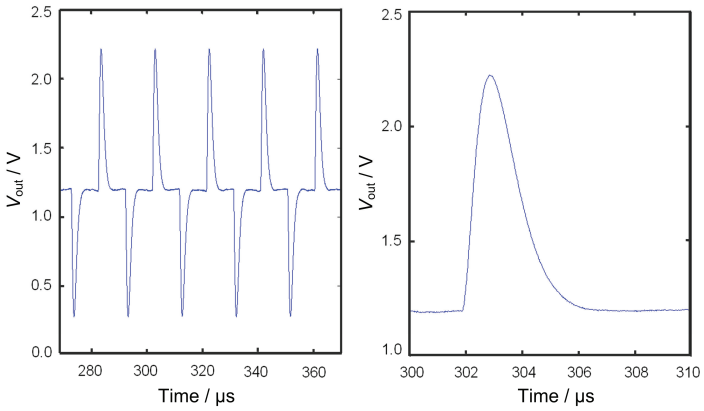

Fig. 6 Output waveform of the pulse shaper.

3.3 Changing gain and peaking time

Changing the switch-control signal can change the capacitor and resistor in the circuit. The dynamic range is 0–90 fC in the typical mode, while in other modes it can be 0–15 fC and 0–150 fC with different gains. The gain is adjustable from 13 to 130 mV/fC and the peaking time varies from 0.7 to 1.6 μs. Table 1 shows the results in seven different modes.

Table 1 The gain and peaking time in different modes.

Modes	1	2	3	4	5	6	7
V_{out}/V_{test}	10.43	16.92	7.75	6.25	15.23	25.32	64.17
Peaking time /μs	1.03	0.60	1.36	1.65	0.95	0.84	0.75
Linearity /%	99.3	99.10	99.20	99.70	99.00	96.70	92.30

3.4 Equivalent Noise Charge

Noise performance is described by equivalent noise charge (ENC), which is the ratio of integrated rms noise at output of the pulse shaper to the signal amplitude due to one electron charge. For testing this circuit, a pulse with 40 periods was injected into the capacitor C_c, where the period was 20 μs. In ideal case, the output waveform has 40 equal peak voltages. The output rms noise was calculated with the standard deviation of a group of output voltage for the same input signal. The ENC was 500–700 *e* in different modes with no detector connected. It should be pointed out that the ENC results included the noise from the test equipment, as shown in Fig.7 which is a two-sided power spectral density. Where the high frequency noises are close to 80 MHz, which is the sample frequency of the test equipment. For this reason, only 40 cycles were recorded. With such a small sampling number, the standard deviation would be larger than the real one. Reducing the sampling frequency at which the waveform is captured can increase the number of cycles saved. However, this will enlarge the sample space. Then, it is difficult to get an exact peak of the shaper output.

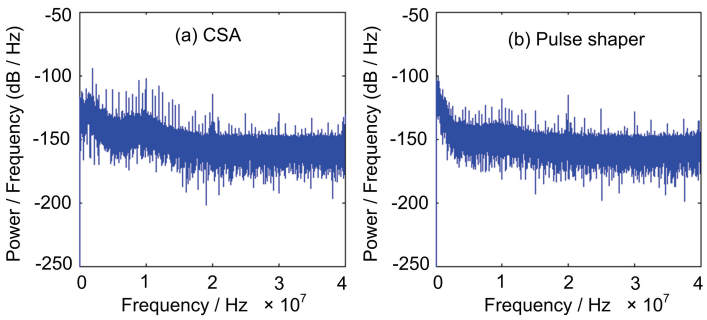

Fig. 7 Noise analysis of the CSA output (a) and the pulse shaper output (b).

3.5 Linearity

Applying different input voltage to obtain the peak output voltages, the linearity can be calculated by[6]:

$$Linearity = (1 - \left|\frac{\max(residual)}{swing(output)}\right|) \times 100\% \quad (5)$$

where, *residual* is the difference between the measured data and the linear fitting result, and *swing* is the output voltage range. The linearity was 99.2% in the typical mode. In other modes, the linearity ranged from 99.1% to 99.7% by changing the capacitor only, whereas by changing the resistor the linearity became worse.

3.6 Performance summary

Performance of the readout ASIC is shown in Table 2.

Table 2 Performance of the readout ASIC.

Size /mm^2	1.7×0.7
Power supply voltage /V	5
Gain / mV·fC^{-1}	13 to 130
Peaking time /μs	0.6–1.6
Equivalent noise charge /*e*	500–700
Linearity /%	99.2

4 Conclusion

Design techniques of a low-noise readout ASIC for high-energy particle detectors is described in detail. The charges released by the detector is converted into a voltage, which is in direct proportion to the input charges, amplified and filtered by following circuits. Then, at the end of the circuit, the output is in direct proportion to the energy the detector detected. Many low noise techniques were used in the design of this ASIC. The readout circuit has been designed in a 0.35 μm DPTM CMOS technology and tested with Verigy 93000. The test results verify the feasibility of this circuit. The readout ASIC can be suitable for many applications.

Refernces

1 Xiao Z, Zou J Q,Zou H, *et al.* J Peking Univer(Natur Sci), 2003, **39(3):** 361–369. (in Chinese)

2 Vandenbussche J, Leyn F,VanderPlas G, *et al*. IEEE Trans Nucl Sci, 1998, 45(4): 2272–2278.

3 Sansen W M C, Zhong Y C. IEEE Trans Circu Syss, 1990, **37(11):** 1375–1382.

4 Adachi S, Nishimura A, Yoshimuta T, *et al.* IEEE Trans Nucl Sci, 2008, **55(6):** 3673–3683.

5 Zhang Y C, Chen Z J,Lu WG, *et al.* ICSICT, 2008, **20–23:** 1717-1720.

6 Zhang Y C, Chen Z J, Lu W G, *et al.* Chin J Semicon, 2007, **28(2):** 182–188.

7 Saghafi S. Adv Optoelectron Lasers, 2005, **5:** 12–17.

8 Pratte J, Junnarkar S, Deptuch G, *et al.* IEEE Trans Nucl Sci, 2008, **55(5):** 2727–2735.

9 Hu Y, Deptuch G, Turchetta R, *et al.* IEEE Trans Circuits Sys, 2001, **48(8):** 1022–1030.