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Clock distribution and local oscillator of a digital low-level radio-frequency board for SSRF

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Abstract In the storage ring RF system of Shanghai Synchrotron Radiation Facility, the clock distribution and the local oscillator are two parts of the digital low level radio frequency hardware board. In this paper, we designed and produced the clock distribution and the local oscillator board using the AD9858 and AD9510 chips. The results show that the phase noise of the local oscillator signal is lower than 100dBc/Hz with 50 kHz offset.

Key words Digital low-level radiofrequency, Clock distribution system, Local oscillator, Digital low-level radiofrequency board

1 Introduction

In the storage ring of a synchrotron radiation facility, the digital low-level radio-frequency (LLRF) system is essential for controlling the radio-frequency system for compensating the loss of beam energy, providing longitudinal bunching voltage, and preventing the electron bunch loss, so as to have a longer lifetime of the beam. An LLRF control system nowadays is a good example of a modern digital implementation of the classic control theory based on analog technology.

The Shanghai Synchrotron Radiation Facility (SSRF), a third generation light source, is built with 499.654 MHz radio-frequency system consisting of the superconducting cavity, klystron and LLRF control system. The LLRF control system for the radio-frequency system of the storage ring consists of circuit boards connected to each other with coaxial cables. This does provide improved reliability and convenience of use, but connecting so many boards of different designs gives rise to a big challenge to build a compact LLRF control system, though this kind of efforts has been succeeded at SNS (Spallation Neutron Source, Oak Ridge National Lab., USA)[4–6] and TESLA (TeV-Energy Superconducting Linear Accelerator, CERN) [7]. In addition, disassembly of the controller is necessary for diagnosis on occurrence of any hardware problem. Also, performance of the system is limited by some of the boards designed long time ago, and our effort to improve the system performance will request a replacement of the old boards, or all the boards. This costs a lot in terms of money and time for a re-design, partly or entirely, if we do not count the difficulties in adding new functions to the system.

In this paper, we report our work progresses in developing an LLRF controller with a new generation of boards. The controller is compact, and has better performance than the one in use at SSRF, in terms of the reliability, stability, scalability and maintainability.

2 Clock distribution and local oscillator in LLRF control system

The SSRF LLRF system, as shown in Fig. 1, is composed of RF front-end, digital processor, clock distribution with local oscillator and RF output.

There are four inputs in the RF front-end system, which are the main signal, cavity forward

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power signal, cavity reflected power signal and cavity signal. The frequency 499.654 MHz of these input signals is too high to input the analog-digital converter (ADC) chip AD6645, which has a max sampling rate of 80 MHz. Therefore, frequency mixers down-convert the RF signals to intermediate frequency (IF) 38.4 MHz with the help of a 461.25 MHz local signal. AD6645 converts the IF signals to digital signals. After processed by algorithm in field programmable gate array (FPGA), the digital signals are converted back to analog signals of 38.4 MHz by digital-analog converter (DAC) chip DAC904. Mixers are needed to up-convert the DAC904 output to RF signal.

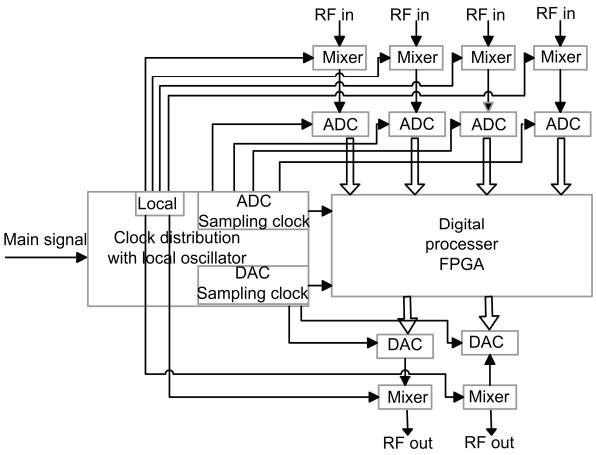

Fig.1 The clock distribution system block diagram. Main signal, RF in, RF out: 499.654 MHz, ADC sampling clock: 30.72 MHz, DAC sampling clock: 122.88 MHz.

The local signal and sampling clock signal is generated in the clock distribution with local oscillator system. The clock distribution system should have a tuning range of frequency and phase so as to compensate the excursion of frequency and phase of the SSRF main signal generator, which may occur as the ambient temperature changes.

The current clock distribution with local oscillator system relies mainly on the AD9858/PCBZ and AD9510-VCO/PCBZ evaluation boards. As commercial off-the-shelf boards, however, they have many specified functions that are not needed in our application. Therefore, we should make an effort to design a new system.

3 Hardware research and development

3.1 Schematic design

The design is based on direct digital synthesizer (DDS) and phase lock loop (PLL) technology.

The DDS is used to generate the 38.4 MHz signal that is necessary for local generating. The AD9858 is a DDS featuring a 10 bit DAC operating up to 1 GS/S. Its main components are a phase accumulator, a phase- to-amplitude conversion (a sine look-up table), and a DAC. The frequency of the output signal is determined by a user-programmed frequency tuning word (*FTW*). The phase accumulator computes a phase address for the look-up table, which provides a corresponding digital value of wave amplitude to the DAC where the number is converted to analog voltage. The *FTW* and reference clock (*REFCLK*) determine the output frequency of the DDS according to Eq.(1).

$$F_0 = \frac{FTW \times REFCLK}{2 \times 2^N} \quad (1)$$

where, $0 \leqslant FTW \leqslant 2^{31}$, N=32, *REFCLK*=499.654 MHz. So, any frequency from 0 to 0.25 Hz of *REFCLK* can be obtained by setting a proper *FTW*.

The PLL is used to compensate the change of frequency and phase of the SSRF main signal generator. AD9510 is a good choice that can realize PLL and generate the clock signals needed by ADC and DAC. Fig. 2 shows the AD9510 block diagram. The AD9510 provides a multi-output clock distribution function along with an on-chip PLL core. The PLL section consists of a programmable reference divider (R), a low noise phase frequency detector (PFD), a precision charge pump (CP), and a programmable feedback divider (N). The PFD compares the frequencies of two signals and produces an error signal which is proportional to the difference between the input frequencies. The error signal is then filtered and used to drive a voltage-controlled oscillator (VCO) or a voltage-controlled crystal oscillator (VCXO). The frequency out from the VCO or VCXO is fed through the N divider back to the system, thus producing a negative feedback loop. If the reference clock drifts, the output error signal will increase, driving the VCO or VCXO frequency in the proper direction, so as to reduce the drift.

Therefore, the output is locked to the reference clock, and clock signals needed by ADC and DAC are generated by adjusting P dividers.

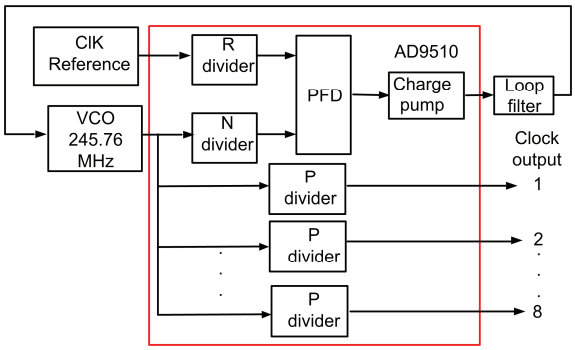

Fig.2 AD9510 block diagram.

The design is shown in Fig.3. The 38.4 MHz signal is generated by adjusting the *FTW* in Eq. (1). The reference clock for AD9510 is to meet the need of a frequency-locked state between the main signal and sampling clock signal of ADC and DAC. It is needed for generating local signal. The clock signals of 30.72 MHz and 122.88 MHz for ADC and DAC are decided by the VCXO and P dividers in Fig.2. The AD9510 and AD9858 are configured by FPGA.

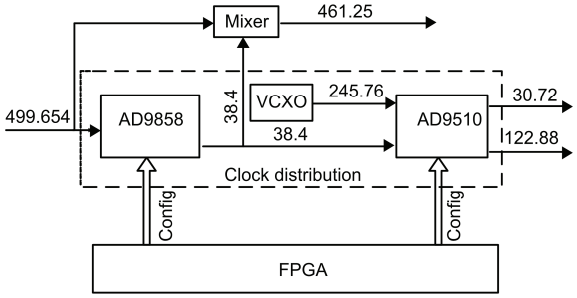

Fig.3 Schematic block diagram. (all units in MHz)

3.2 Hardware board

The board we developed is shown in Fig.4. Zone A consists of an AD9858 and the configuration pins. The output signal is measured by connecting an output Sub-Miniature-A (SMA) connector to an analyzer. The AD9510 with its outputs and configuration pins is in Zone B. As mentioned above, AD9510 has eight differential outputs. Realization of clock PLL needs an external VCXO of 245.76 MHz in Zone C. All the 9858 and 9510 configuration pins are connected to the FPGA directly, so as to be configured online. The power supply pins are in Zone D. The system needs 3 kinds of voltages: AVDD (+3.3 V), DVDD (+3.3 V), and +5 V. The board has rooms for testing functions of the chips.

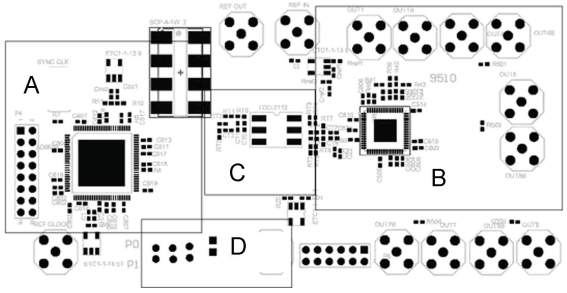

Fig.4 The clock distribution and local oscillator board. A: AD9858; B: AD9510; C: VCXO; D: power.

4 Measurement and results

The clock quality is usually described by jitter or phase-noise. Period jitter (J_{PER}) is the time discrepancy of a measured cycle period from the ideal cycle period. Due to its random nature, this jitter can be measured by peak-to-peak or root of mean square (RMS) using, for example, a common high-precision oscilloscope. The sampling data from the high-speed digital oscilloscopes are processed to estimate the jitter. This provides high-precision results, but it can only be performed with high-end digital oscilloscopes.

The power spectrum density of a clock signal is defined as $S_c(f)$, which can be obtained from the spectrum analyzer. The phase noise (in dBc/Hz) is defined as,

$$L(f-f_c) = 10\log[S_c(f)/S_c(f_c)] \quad (2)$$

However, it is not practical to use a spectrum analyzer and measure $L(f)$, which is usually less than –100 dBc, well exceeding the dynamic range of most spectrum analyzers. Also, f_c can be higher than the input frequency limit of the analyzer. So, a measurement eliminating the spectrum energy at f_c is used instead. The approach is similar to that of demodulating a pass band signal to base band [8].

In a measurement, the carrier power of the phase (frequency) fluctuations of the actual sideband power is of greater interest. The phase noise is characterized by the true meaning of power spectral density—single side band phase noise.

For the phase noise of a specified offset point, the normalized $L(f)$ is given by Eq.(3),

$$L(f) = P_m - P_c - 10\log(1.2B_{nT}) + C \quad (3)$$

where, P_c (dBm) is carrier power, P_m (dBm) is sideband noise power deviating from the carrier frequency(f), B_{nT} is equivalent noise of analysis bandwidth of the spectrum analyzer, and C is 2.5 dB[9].

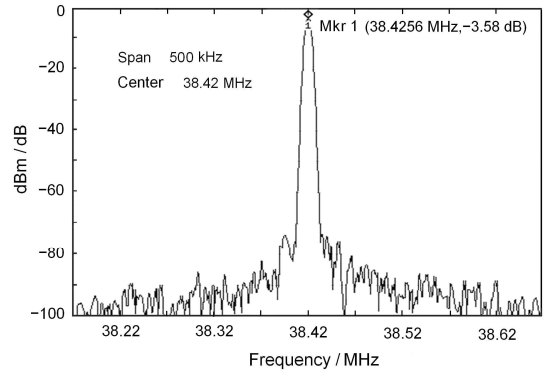

Fig.5 Signal out from AD9858.

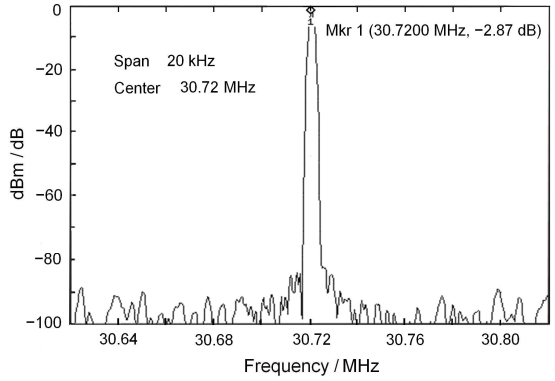

Fig.6 Signal out from AD9510.

We measured the phase noise of the signals generated. Fig.5 shows the 38.4 MHz signal out of D9858 with a 500 kHz span. The phase noise is about –110 dBc/Hz with 50 kHz offset according to Eq. (3). The local signal is a result of mixing the 38.4 MHz and main signal, and performance of the 38.4 MHz signal represents performance of the local signal. Fig.6 shows the 30.72 MHz signal from AD9510 with a 20 kHz span. The quality of sampling clock significantly affects performance of the ADC. Phase noise of the signal is about –115 dBc/Hz, which meets requirement of the ADC.

A frequency tuning range of 10 kHz is obtained between the 38.4 MHz signal and the clock output of AD9510, and the frequency tuning range for the main signal generator (499.654 MHz) is more than 100 kHz according to Eq.(1), which is enough to satisfy the SSRF's frequency changing range (20 kHz) caused by annual temperature variation.

5 Conclusions

The clock distribution and LO board used for improving the SSRF LLRF control system is designed and tested. The performance of LO board satisfies for adjusting a variation range of 20 kHz/year. The phase noise meets the requirement of SSRF. It is an encouragement for the design on the new generation SSRF LLRF control system.

References

1 Zhang T X, Zhao Y B, Yin C K, *et al*. HPLP.B, 2008, **20(6)**:1048–1052. (in Chinese)

2 Wang F, Wang G W. Nucl Tech, 2004, **27(1)**:18–21.

3 Zhao Y B, Yin C K, Zhang T X, *et al*. Chin Phys C 2008, **32 (9)**: 758–760.

4 Doolittle L, LO C C, Monroy M, *et al*. The SNS front end LLRF system. Proceeding of LINAC2002. 373–375.

5 Ma H J, Champion M, Crofford M, *et al*. SNS low-level RF control system: Design and performance. Particle accelerator conference 2005. 16–20 May 2005, 3479–3481.

6 Champion M, Crofford M, Ma H, *et al*. The Spallation neutron source accelerator low level RF control system. Particle accelerator conference 2003. 12–16 May 2003, 3377–3379.

7 Karol P, Krzysztof T P, Wojciech J, *et al*. FPGA-based multichannel optical concentrator SIMCON 4.0 for TESLA cavities LLRF control system. Photonics applications in astronomy, communications, industry, and high-energy physics experiments 2006, proceedings of SPIE, 6347.

8 Maxim Application Note 3359. http://www.maxim-ic.com/an3359

9 Dai W J. The method of phase noise measurement using a spectrum analyzer. Foreign Electron Measure, 2001, **5:** 11–12. (in Chinese)