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A time and charge measurement board for muon tomography of high-Z materials

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Abstract In this paper, a versatile time and charge measurement (MQT) board for muon tomography is described in detail. For time measurement, the general-purpose time-to-digital converter (TDC) chip TDC-GP2 is employed, while for charge measurement, digitization plus numerical integration in field programmable gate array is employed. Electronic tests demonstrate that the total 32 channels of two MQT boards have a time resolution of superior than 100 ps, with excellent linearity for time and charge measurement.

Keywords Time and charge measurement · General-purpose time-to-digital converter (TDC-GP2) · Muon tomography

1 Introduction

When muon passes through a material, multiple small-angle Coulomb scattering happens and the accumulated scattering angle can be obtained when muon penetrates the material [1, 2]. By measuring the scattering angle, one is able to detect and image an object containing high-Z materials. Given that the scattering angle is of the order of $\sim$10 milliradian, a position-sensitive detector is required [3]. So a muon tomography prototype based on drift chamber detector is proposed [4, 5], and read-out electronics for time measurement needs to be developed.

The time and charge measurement are implemented with a 16-channel time and charge measurement (MQT) board based on Versa Module Eurocard (VME) crate. The overall time resolution should be 1 ns to meet the requirement of 50-μm position resolution. Therefore, the time resolution of MQT board should be <100 ps, which will have a negligible contribution to the overall time resolution.

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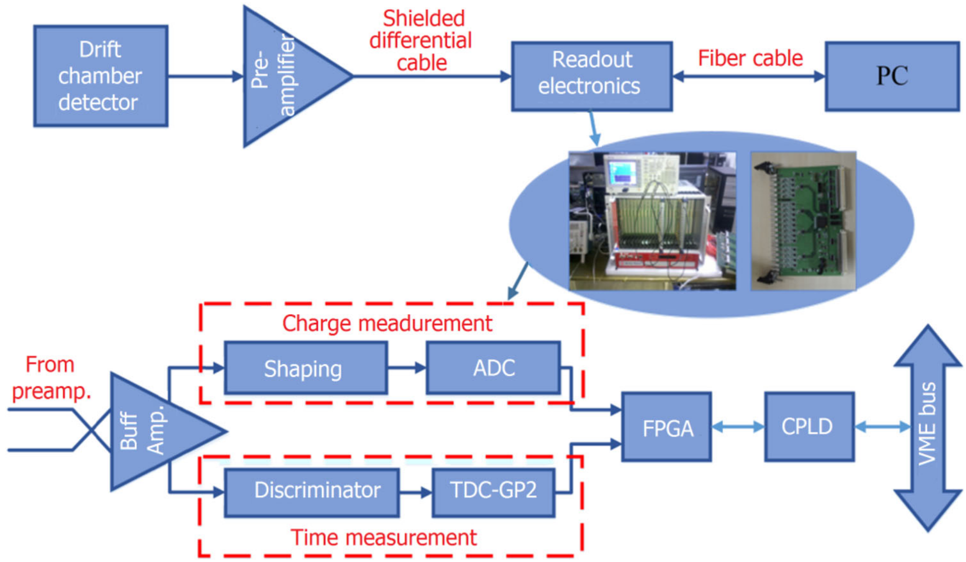
2 Time and charge measurement board

As described above, the MQT board is responsible for time and charge measurement [6]. Differential signal containing time and charge information from preamplifier is distributed into two signals for time and charge measurement, respectively. In the charge measurement part, the signal is processed by a shaping circuit and sent to ADC for digitization. Then, numerical integration is implemented in FPGA to calculate signal area, which is proportional to the signal charge. In the time measurement part, the signal is processed by a discriminating circuit and then sent to TDC-GP2 to measure the time interval. The measurement results are also sent to FPGA for further processing. The time and charge results are packed and then sent to complex programmable logic device (CPLD), which is responsible for communication between FPGA and VME bus. Figure 1 shows schematically the electronics system, and the middle part is MQT board and VME crate. Each MQT board

Fig. 1 Schematic diagram of the MQT board



contains eight TDC chips, four ADC chips, one FPGA and one CPLD and is responsible for 16-channel time and charge measurement board.

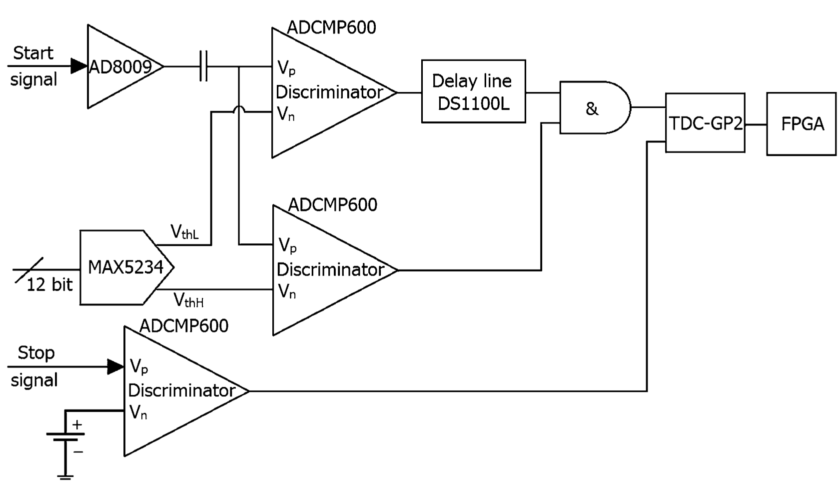
2.1 Time measurement

Analog signals are converted into digital signals with timing discriminator for time measurement. To reduce design complexity, the leading edge timing discriminator is employed [7–9]. The time measurement part is shown schematically in Fig. 2. An input start signal passes through two discriminators of different thresholds to a coincidence gate, which is linked by a delay line to the discriminator with low threshold. Then, the start and stop signals pass through the TDC-GP2 chip to the FPGA. TDC-GP2 is a general-purpose TDC chip suitable for cost-sensitive applications. Its measurement ranges from 3.5 ns to 1.8 µs or from 500 ns to 4 ms [10, 11]. We use the 3.5–1800 ns range with the typical resolution of 50 ps [12].

2.2 Charge measurement

Charge measurement of preamplifier output signal is equivalent to amplitude or area measurement of the signal [13]. The charge measurement circuit is shown in Fig. 3. The pole-zero cancellation network acted as a differentiator attenuates low frequencies, and the two-stage RC filter acted as an integrator attenuates high frequencies. The adjustable resistor in the pole-zero cancellation circuit should be adjusted to an optimal value to minimize undershoot [14]. The time constant is 0.1 µs to generate a semi-Gaussian signal of 1 µs pulse width at 0.1% of the pulse amplitude. The shaped signal is then passed through a full differential amplifier to ADC for digitization. Digital

Fig. 2 Block diagram of time measurement



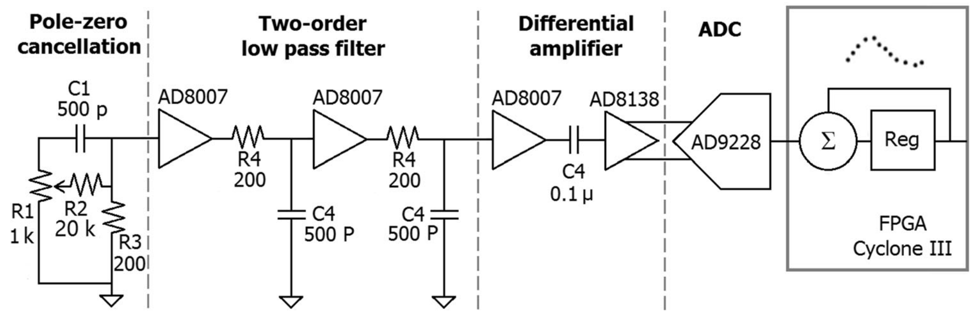


Fig. 3 Schematic diagram of charge measurement

data are sent to FPGA for numerical integration, each time about 40 points are accumulated [15].

3 Results and discussion

To examine the performance of the MQT board, electronic tests were performed. A Tektronix dual-channel arbitrary signal generator AFG3252 was employed, with one channel outputting a pulse as the start signal, and another outputting a customized signal as stop signal in similar shape to the preamplifier output signal. The phase between outputs of the two channels could be finely regulated.

3.1 Time measurement test

The resolution and integral nonlinearity (INL) of time measurement were tested. For time resolution test, multiple measurements were taken for a specific delay, and the standard deviation of the multiple results was the time measurement resolution. From Fig. 4a showing the typical counts histogram at a specific delay, the corresponding resolution was 67.7 ps at 502.8-ns delay, while from Fig. 4b, resolutions of all 32 channels of two MQT boards are <100 ps. As a calibration was conducted following the time measurement each time in TDC-GP2, the tested resolution is relatively stable with variation of temperature and supply voltage.

The time measured at different delays from 0 to 500 ns is shown in Fig. 5a. The INL was calculated at 0.095%, and the linear fitting equation of $T = 0.9975D + 3.6479$ was obtained, where D is the delay and T is measured time. As slope and intercept of each fitting line for every channel are different, a linearity correction was implemented with this equation [16]. Figure 5b shows that all 32 channels of the two MQT boards have excellent linearity for time measurement.

3.2 Charge measurement test

As the detector and preamplifier were not completed, an equivalent INL test was conducted. A customized signal in similar shape to the preamplifier output was used as the input, and the signal amplitude was proportional to the charge. The measured pulse areas at different input signal amplitudes from 50 to 500 mV are shown in Fig. 6a, and from a linear fitting of the data, the INL was calculated at 0.08%, indicating excellent linearity of the charge measurement. In fact, the INLs of all 32 channels are <0.15%, as shown in Fig. 6b. As resolution and range of charge measurement were designed to be 15 and 1800 fc, respectively, a 12-bit ADC AD9228 was employed, and the effective number of bits (ENOB) of each channel was >9, which meets the requirement. In fact, the charge information is also useful for correction of leading edge timing discrimination.

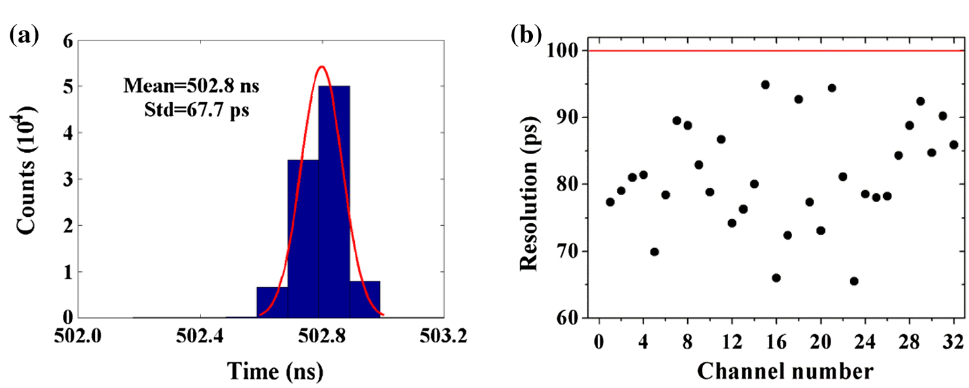


Fig. 4 **a** Typical counts histogram at a specific delay; **b** time resolutions of all 32 channels of two MQT boards

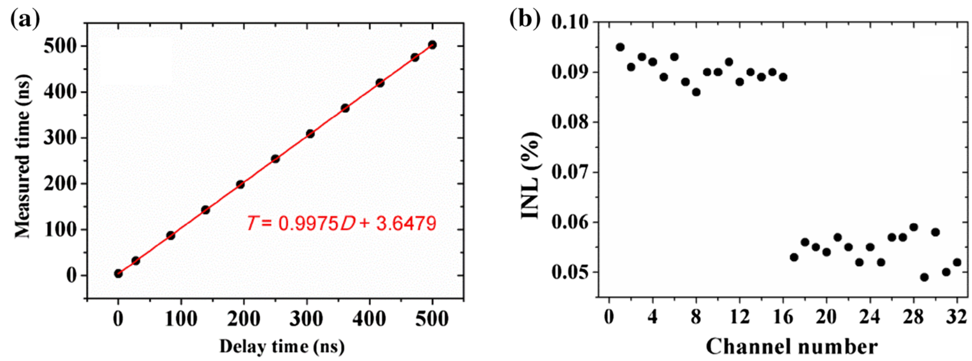


Fig. 5 Linearity between delay and measured time (**a**) and the time measurement INLs of all 32 channels of the two MQT boards (**b**)

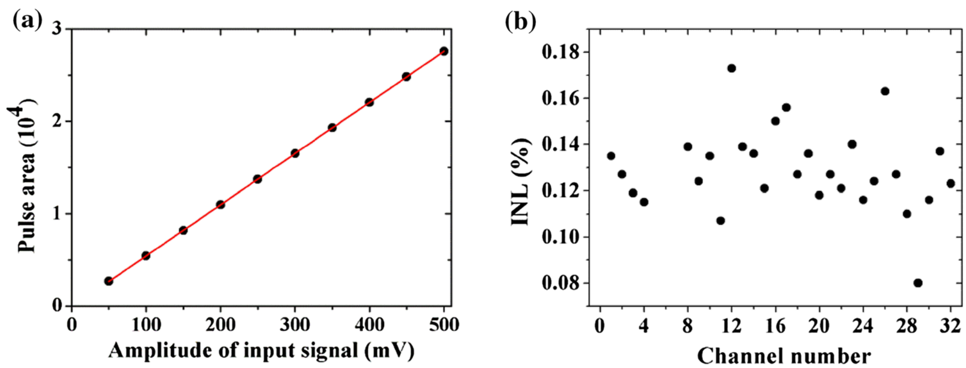


Fig. 6 Linearity of the charge measurement data (**a**) and the charge measurement INLs of all 32 channels of the two MQT boards (**b**)

4 Conclusion

A time and charge measurement board has been developed for the drift chamber-based muon tomography. The general-purpose TDC chip TDC-GP2 is employed for time measurement of drift chamber detector. Test results show that all the 32 channels of two MQT boards have a time resolution of <100 ps, with excellent linearity for the time and charge measurement. Joint tests with drift chamber and preamplifier will be carried out. And the charge information will be used for correcting leading edge timing discriminator, which will minimize the timing walk. After the joint tests, we will consider developing stand-alone readout electronics suitable for field applications.

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