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A novel single event upset reversal in 40-nm bulk CMOS 6 T SRAM cells*

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In advanced technologies, single event upset reversal (SEUR) due to charge sharing can make the upset state of SRAM cells recover to their initial state, which can reduce the soft error for SRAMs in radiation environments. By using the full 3D TCAD simulations, this paper presents a new kind of SEUR triggered by the charge collection of the Off-PMOS and the delayed charge collection of the On-NMOS in commercial 40-nm 6 T SRAM cells. The simulation results show that the proposed SEUR can not occur at normal incidence, but can present easily at angular incidence. It is also found that the width of SET induced by this SEUR remains the same after linear energy transfer (LET) increases to a certain value. In addition, through analyzing the effect of the spacing, the adjacent transistors, the drain area, and some other dependent parameters on this new kind of SEUR, some methods are proposed to strengthen the recovery ability of SRAM cells.

Keywords: Radiation environment, 6 T SRAM cell, Charge collection, Charge sharing, Single event upset reversal (SEUR), Single event transient (SET)

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I. INTRODUCTION

Single event effects (SEEs) seriously break the normal functions of integrated circuits (ICs), which work in radiation environments [1]. As a kind of SEEs, single event upset (SEU) makes the predominant contribution to the soft error of static random access memories (SRAMs) [2–4]. Thus, many researchers have paid significant attention to SEU in order to produce hardened designs and reduce the soft error rate (SER) for SRAMs. With greater packing density at advanced technology nodes, the charge sharing among sensitive devices makes the SRAM cells more sensitive [5]. For example, the charge sharing makes existed hardened designs, such as triple-modular redundancy (TMR) and dual interlocked cells (DICE), vulnerable to upsets in advanced technologies [6, 7].

But there are also some favorable effects of charge sharing on the radiation sensitivity of SRAM cells. A great many of the experiment results illuminated that SER may be largely overestimated if the charge sharing based on placement is not considered in advanced technologies [8–10]. Lee *et al*. found that the negative charge collected by the On-transistor can restrain the upsets happening on the output node in an inverter [11]. Using this restraining mechanism, DICE are improved to restrain multi-cell upsets (MCUs). Ahlbin *et al*. observed "Pulse Quenching" in logic circuits for the first time, which is induced by charge sharing and can decrease the pulse width of a single event transient (SET) [12]. In 90-nm SRAM cells, Black *et al*. advocated the similar phenomenon that SEU can be recovered due to the well-collapse-source-injection mechanism [13]. In 40-nm triple-well SRAMs, Chatterjee *et al*. showed that the charge collection of both the adjacent NMOSs in cross-coupled inverters can trigger the recovery of SEU at high linear energy transfers (LETs), and they named this new beneficial mechanism "SEU reversal (SEUR)" [14]. A similar work was carried out by Qin *et al*. in 90-nm SRAMs, where SEUR induced by charge sharing between the two adjacent PMOSs has been studied [15]. In the process of SEUR, one of the devices in the OFF state collects charges induced by striking particles and trigger an upset, then the adjacent device's state changes to OFF due to upset and also collects charges and makes the SRAM cell recover to the initial state. Thus, SEUR is based on charge sharing between adjacent devices. However, little attention is paid to the effect of charge sharing between the adjacent PMOS and NMOS in SRAM cells in previous research.

This paper focuses on a novel SEUR, which depends on the charge collection of the Off-PMOS and the delayed charge collection of the On-NMOS, and studies it in a single commercial 40-nm 6T SRAM cell using full 3D TCAD simulation. We term this SEUR as $\mathrm{SEUR_{PN}}$ to distinguish it from other existing SEURs. Like other studied SEURs, $\mathrm{SEUR_{PN}}$ is also based on the charge sharing which exists between Off-PMOS and On-NMOS. It is found that $\mathrm{SEUR_{PN}}$ can not occur when the radiation particles perpendicularly hit the devices, but can appear in angular incidence. The reason is analyzed in depth. We also confirmed that after $\mathrm{SEUR_{PN}}$ occurs at high LETs, the width of SET due to $\mathrm{SEUR_{PN}}$ remains the same, even with increasing LET. Lastly, the dependent parameters of $\mathrm{SEUR_{PN}}$ are studied.

II. GENERATION MECHANISM OF $\mathrm{SEUR_{PN}}$

A. Simulation setup

The schematic of a single commercial 6T SRAM cell used in this paper is shown in Fig. 1(a). It consists of 2 cross-coupled inverters and 2 access pass-gate transistors. All the 6 transistors are modeled in a 3D TCAD block, as illustrated in Fig. 1(b). The size of the 3D TCAD block is 5 μm × 5 μm × 5 μm, and the size of each transistor and lay-

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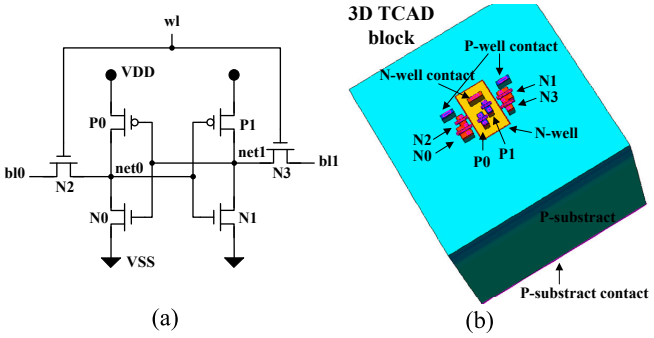

Fig. 1. (Color online) (a) Schematic illustration and (b) 3D TCAD block consisting of 6 device models for the single commercial 6 T SRAM cell used in our simulation.

out details are extracted by the Memory Compiler, based on a commercial 40-nm bulk CMOS technology. The doping profiles of the 3D device models used in this paper consulted Ref. [16], and they have also been calibrated to the DC and AC electrical characteristics of the process development kit (PDK) supplied by the foundry. The I-V characteristics of the 3D device models and the SPICE models can be well matched. The charge deposited by the incident heavy ion is modeled using a Gaussian radial profile with a characteristic $1/e$ radius of $0.05\,\mu$m and a Gaussian temporal profile with a characteristic decay time of 0.5 ps. The other physical models adopt the default setup in Sentaurus TCAD.

For all simulations, we assumed that the storage states of net0 and net1 are low and high, respectively. Thus, at the beginning of the simulation, P0 and N1 are off and P1 and N0 are on. To cause the SRAM cell to be in a retention state, both N2 and N3 must be in the Off-state during the whole simulation process. Under these conditions, the OFF drains of P0 and N1 are the most sensitive regions in our simulation. Since the main factor of $\mathrm{SEUR_{PN}}$ occurrence is that the Off-PMOS collects enough deposited charge to trigger the first upset, the center of P0's drain is chosen as the particle hit location in all the simulations. However, the center of the PMOS drain is not the only hit location that can trigger $\mathrm{SEUR_{PN}}$. As long as the hit location can cause NMOS to collect enough deposited charges to trigger the second upset after Off-PMOS triggers the first upset, it induces $\mathrm{SEUR_{PN}}$.

B. Absence of $\mathrm{SEUR_{PN}}$ in normal incidence

First, we explored whether $\mathrm{SEUR_{PN}}$ can occur at a perpendicular hit, which is commonly adopted in particle striking simulations. Since SEUR significantly depends on LET values in the former studies, different LET values are adopted in the simulation. SEU obviously occurs in all simulations, as shown in Fig. 2(a), but there is no SEUR observed on net0. In Fig. 2(b), SEU on net1 trends to recover after about 15 ps, but it still returns to the upset state at the end. This indicates that the delayed charge collection of P1 due to charge sharing makes net1 enter a metastable state, and then net1 returns to low again after the charge collection is over.

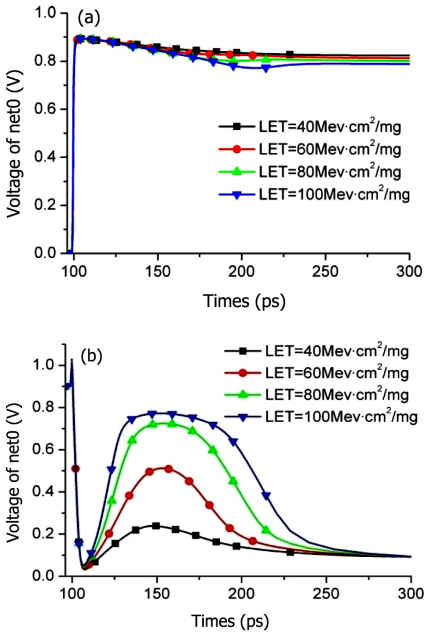

Fig. 2. (Color online) Voltages pulses of (a) net0 and (b) net1 at normal incidence with different LET values.

C. Presence of $\mathrm{SEUR_{PN}}$ at angular incidence

The normal incidence of particle striking is an exceptive case for ICs in radiation environments, while the angular incidence is more frequent. Compared to the normal incidence, the angular incidence enlarges the scope of deposited charges and increases the charge collection of the adjacent devices. Based on these points, $\mathrm{SEUR_{PN}}$ may occur more easily if the incident angle leans to N0. The angles of particle striking used in the simulation are illustrated in Fig. 3(a), and the simulation results obtained with a LET of $40\,\mathrm{MeV\,cm^2/mg}$ are shown in Fig. 3(b). One can see that the upset state of net0 recovers to the initial state when the incident angles are larger than $30°$. Both the width and magnitude of SET due to $\mathrm{SEUR_{PN}}$ reduce with increased incident angles, while the incident angle is no less than $45°$. But SET magnitude becomes much smaller (with the peak value of 0.48 V) at an incident angle of $75°$. It is demonstrated that $\mathrm{SEUR_{PN}}$ happens at incident angles of $45°$ and $60°$, but the state recovery of net0 at an incident angle of $75°$ is not related to $\mathrm{SEUR_{PN}}$. Furthermore, the current transients of net0 in the same simulations are given in Fig. 3(c). There are two peaks in the current transient of net0. The first current peak is caused by the charge collection of P0, while the second one is due to the delayed charge collection of N0. With the incident angle increasing, the first current peak goes down because of the charge collection reduction of P0. Contrarily, the second current peak goes up because of the larger charge deposited under N0.

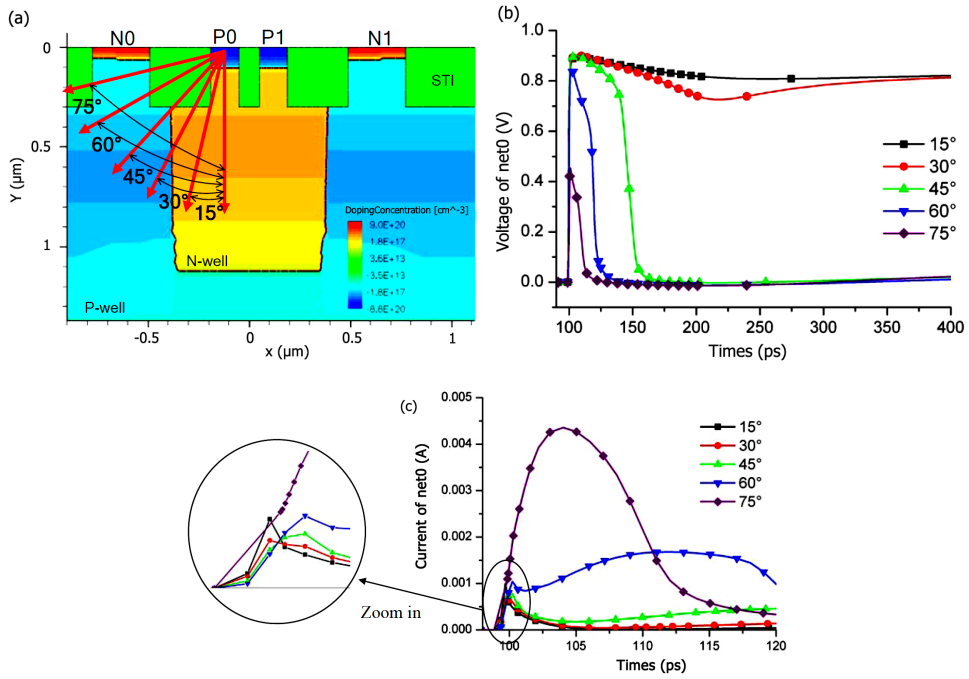

Fig. 3. (Color online) (a) Two-dimensional slice of cross-coupled illustrating the angle of hit particles, (b) voltage pulses and (c) current pulses of net0 at different incident angles.

III. ANALYSIS OF SEUR$_{PN}$ MECHANISM AND CHARACTERISTIC

The entire process of SEUR$_{PN}$ is shown schematically in Fig. 4. After tilted particles strike the center of P0's drain at normal incidence, numerous electron-hole pairs are produced along the ion track in the N-well. In the structure of 3D TCAD block, the P-well-N-well junction is reverse-biased, and it makes the electrons stay in the N-well and the holes drift into the P-well. The potential of N-well under P0 will collapse due to the numerous electrons, and trigger the parasitized bipolar amplification effect for P0. Then, the junction between the P+ source of P0 and the N-well become forward-biased, and the hole current from the source injects into the drain of P0 through the channel [17]. The state of net0 upsets while the drain of P0 collects enough holes. Then, net1 jumps from high to low after the signal of net0 passes through an inverter, and it changes the state of N0 from ON to OFF. The tilted incident particles also enter into P-well and produce electron-hole pairs. Then, the electrons under N0 are collected by the reversed-biased junction between the N+ drain and the P-well due to the OFF state of N0. While the drain of N0 collects enough electronics, net0 upsets again.

The presence of SEUR$_{PN}$ depends on 2 important factors: (1) the Off-PMOS collects charges at first to trigger the first upset after particle striking; (2) the NMOS, whose state has become OFF due to the first upset, collects enough charge to trigger the second upset. Thus, the reason why SEUR$_{PN}$ does not occur at the incident angles of 15° and 30° in Fig. 3(b) is that N0 does not collect enough charge to trigger the second upset. For the incident angle of 75°, P0 does not collect enough charge to trigger the first upset due to the much short particle track under P0, as shown in Fig. 3(a). Thus, no SEU on net0 can be observed. It can be proved in Fig. 3(b), the voltage peak of net0 is less than 0.45 V at 75 degrees angle, which can not change the state of P1 to cause an upset.

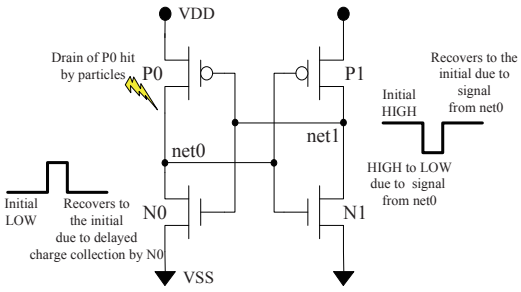

Fig. 4. (Color online) Schematic illustrating the process of SEUR$_{PN}$.

Since the main mechanisms of charge collection by NMOS are drift and diffusion, the P-well potential and electron concentration under N0 determine whether the second upset can occur. For angular incidence, the potential under N0 is increased with the incident angles. So the electrons in the P-well can be collected more easily by N0 at a larger incident angle. Since increased incident angles can enhance the charge collection of N0, SEUR$_{PN}$ can be present easily in angular incidence.

In order to further analyze the characteristics of SEUR$_{PN}$, the relationship between SEUR$_{PN}$ and LETs is studied in this paper. Figure 5 illustrates the voltage and current pulses of net0 at different LETs with the same incident angles of 60°.

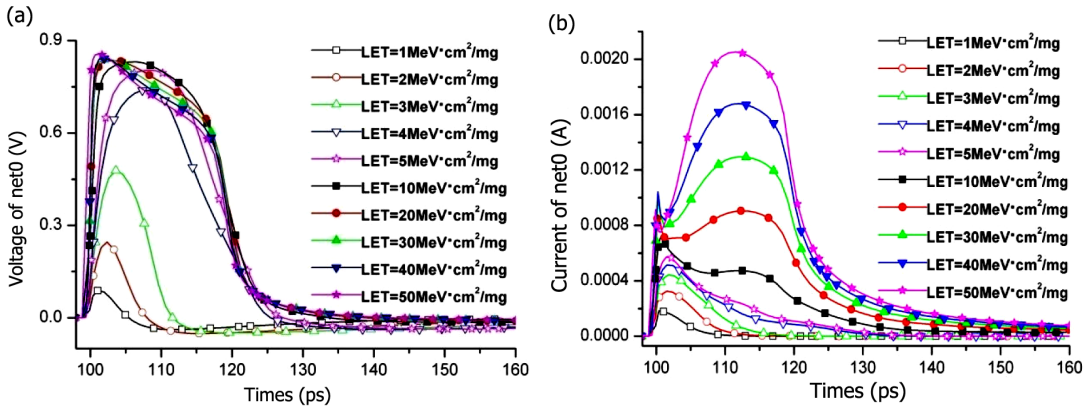

Fig. 5. (Color online) (a) Voltage pulses and (b) current pulses of net0 at different LETs, while the incident angle keeps 60°.

When LETs are 1–3 MeV cm^2/mg, SETs on net0 are inapparent, indicating that P0 does not collect enough charge to trigger the first upset. Since the incident angle reduces the length of the particle track and the charge collected by device, the critical charge in angular incidence is much higher than that in normal incidence. Thus, P0 can not collect enough charge to trigger upset while the LETs are 1–3 MeV cm^2/mg at 60°. SEUR$_{PN}$ occurs on net0 when LET is more than 3 MeV cm^2/mg, indicating that the threshold LET is larger than 3 MeV cm^2/mg at 60° incident angle. The attractive phenomenon in Fig. 5 is that, even though the second current peak of net0 increases with LETs, the width of SET on net0 due to SEUR$_{PN}$ nearly remains the same when LET is more than 10 MeV cm^2/mg. Because this SET width can not be reduced by increasing the LET value, it is the smallest SET width induced by SEUR$_{PN}$.

The width of SET induced by SEUR$_{PN}$ is the time interval between the two upsets. In other words, the SET width is equal to the sum of the generation time of the first and the second upset and the signal transition delay from net0 to net1 passing through an inverter. The inverter delay is not relational to LET. The generation time of upset is decided by the charge absorption rate of the device, which will not change while LET exceeds a certain value. That is the reason why SET width remains the same, while LET being more than 10 MeV cm^2/mg. The delay of the inverter in the SRAM cell is 11–12 ps in Hspice simulations, using the parasitic RC with TT conditions. Then, it can calculate that the shortest generation time of the two upsets is nearly 8–9 ps, while the smallest width of SET is 20 ps in our TCAD simulations.

In 40 nm SRAMs, MCU becomes serious due to the decreased spacing between the devices [18]. Since MCU is composed of multiple SEUs happening in adjacent SRAM cells, SEU mitigation caused by SEUR in a single SRAM can also increase MCU reliability. Reference [19] concluded that SEUR can not only still occur after MCU happens, but also decrease the size of MCU. Thus, for a single SRAM cell in the scope of MCU, if the corresponding conditions of SEUR$_{PN}$ are satisfied, SEUR$_{PN}$ will avoid SEU and decrease the size of MCU, too.

Although SEU is eliminated after SEUR$_{PN}$ occurs, the existing SET could also break the read operation for the SRAM cells. By optimizing the delay of the inverter in the SRAM cells, the width of SET due to SEUR$_{PN}$ can be cut down to reduce the rate of inaccurate read operations. Analyzing the characteristics of SEUR$_{PN}$ in depth is very important for not only learning its mechanisms, but also guiding the approach to increasing the recovery ability of SRAM cells. Thus, the relevant parameters on SEUR$_{PN}$ are studied in the next section.

IV. DEPENDENT PARAMETERS ON SEUR$_{PN}$

A. Spacing dependence

It is well known that the degree of charge sharing significantly depends on the spacing between the hit location and the sensitive nodes. Thus, the spacing between P0 and N0 is important for SEUR$_{PN}$. Figure 6(a) shows SEUR$_{PN}$ happened on net0 at different spacings. It is obvious that SET width is proportional to the spacing between P0 and N0. More details can be seen in Fig. 6(b), which shows the current transients of net0 in the same simulation. Since the first current peak is induced by the charge collection of P0, its generation time and peak value are unchanged at different spacings. As spacing increases, the hit location is far away from N0, and it makes the charge collection of N0 decrease. It delays the generation of the second upset and increases SET width in Fig. 6(a).

We redo these simulations with an LET of 10 MeV cm^2/mg. The SET widths in the all simulations in this section are summarized in Fig. 7. The trend of SET width at an LET of 10 MeV cm^2/mg is much more obvious than that at an LET of 40 MeV cm^2/mg. Moreover, SEUR$_{PN}$ does not occur when LET is 10 MeV cm^2/mg and the spacing is 0.8 μm. It can be concluded that the increase in spacing between Off-PMOS and On-NMOS can weaken and even eliminate SEUR$_{PN}$, and the weakening effect is stronger at smaller LETs. Thus, reducing the spacing between the PMOS and NMOS in the same inverter of the SRAM cells can help to increase the occurrence rate of this kind of SEUR$_{PN}$ and diminish the width of SET by picking up the

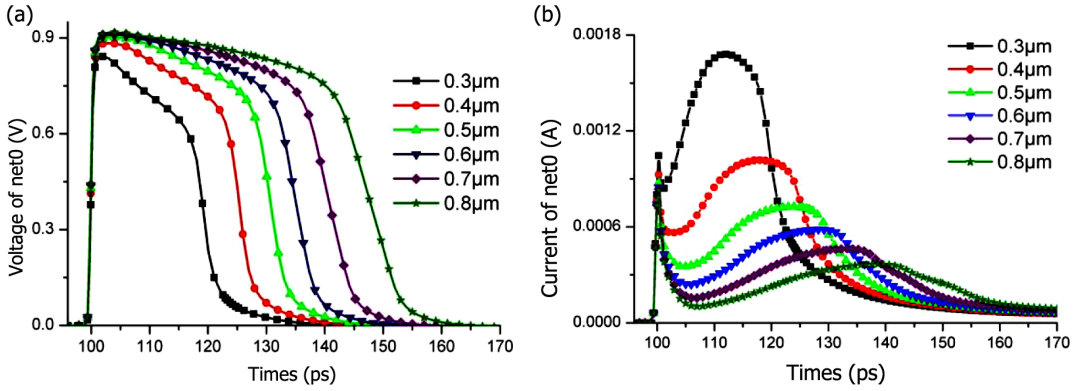

Fig. 6. (Color online) (a)Voltage pulses and (b) current pulses of net0 for different spacings between P0 and N0 with LET of 40 MeV cm^2/mg and the incident angle of 60°.

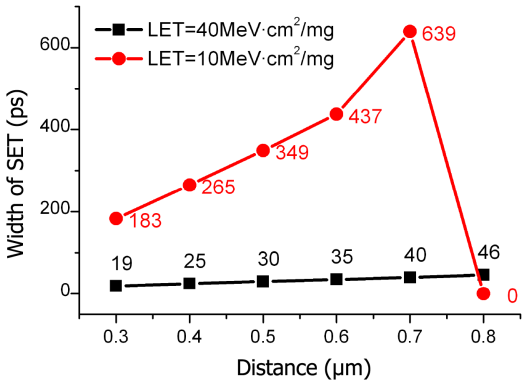

Fig. 7. Width of SETs on net0 for different spacings with LET of 40 and 10 MeV cm^2/mg.

generation time of the second upset.

B. Adjacent transistors dependence

Since the access pass-gate NMOS and the NMOS in the inverter are adjacent to each other and share the same drain in the SRAM cell layout, the access pass-gate NMOS in the Off-state may affect the second upset generated by On-NMOS during the process of $SEUR_{PN}$. We designed 3 simulation cases, as shown in Fig. 8(a) to analyze the effect of the access pass-gate NMOS (N2 in the simulations) on $SEUR_{PN}$. Case1 is the normal case. In Case2, the 3D model of N2 is directly removed from the 3D TCAD block, and a NMOS SPICE model is used to complete the SRAM cell for the simulation. Case3 is designed almost the same as Case2, except that the drain of N2 is held in the 3D TCAD block. Figure 8(b) shows the simulation results at an incident angle of 45° and an LET of 40 MeV cm^2/mg. The width of SET due to $SEUR_{PN}$ in Case2 is much longer than that in Case1. From the second current peak of net0, as shown in Fig. 8(b), one can see that the charge collection of N0 in Case2 is less than that of Case1. It indicates that N2 can help to increase the charge collection of N0. However, there is less distinction between Case1 and Case3 for SET width. So the effect of N2 on $SEUR_{PN}$ is mainly due to the drain of N2, which can increase the area of N0's drain. Moreover, it is also inferred that the drain area of N0 may affect $SEUR_{PN}$ a lot, which will be studied in detail later.

C. Drain area dependence

The drain area is one of the key components to determine the charge collection of the sensitive devices. The charge collection of On-NMOS in the SRAM cells dominates the second upset of $SEUR_{PN}$. Thus, the rate of $SEUR_{PN}$ can be increased by changing the drain area of NMOS to shut down the SER of the SRAM cells.

We chose 3 kinds of drain areas for N0 in the simulations: 0.285 μm × 0.13 μm (normal), 0.285 μm × 0.07 μm (smaller) and 0.285 μm × 0.26 μm (larger), respectively, as shown in Fig. 9(a). The simulation results are shown in Fig. 9(b). It is clearly seen that the SET width increases as the drain area of N0 decreases. The different second current peaks of net0 indicate that the larger the drain area of N0, the more its charge collection. Then the increased charge collection of N0 makes the second upset occur earlier and reduces SET width due to $SEUR_{PN}$. While the area of the SRAM cells stay the same, the increased drain area of NMOS can enhance the $SEUR_{PN}$. It is indicated that the active area occupation rate on total the SRAM cell area increases the occurrence rate of $SEUR_{PN}$.

Based on the conclusions above, enlarging the drain area of NMOS in the inverter can reduce the occurrence rate of SEU in the SRAM cells. But amplifying the drain area will make NMOS easier to be hit with particles, and increases the sensitivity of the 6 T SRAM cells [20]. Thus, setting a reasonable size for the NMOS drain area is needed to make the tradeoff between the occurrence rate of $SEUR_{PN}$ and the sensitivity of NMOS.

There are also some other subsidiary dependent parameters on $SEUR_{PN}$, and they will be discussed briefly below. As discussed in Sec. III, the width of SET induced by $SEUR_{PN}$ is

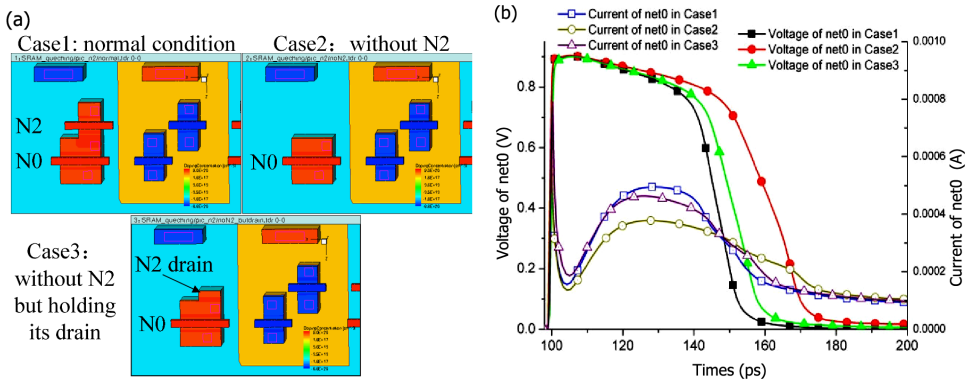

Fig. 8. (Color online) (a) Top view of the 3D TCAD block in 3 different simulation cases, and (b) voltage pulses of net0 and current pulses of net0 for 3 cases with incident angle of 45° and LET of $40\,\mathrm{MeV\,cm^2/mg}$.

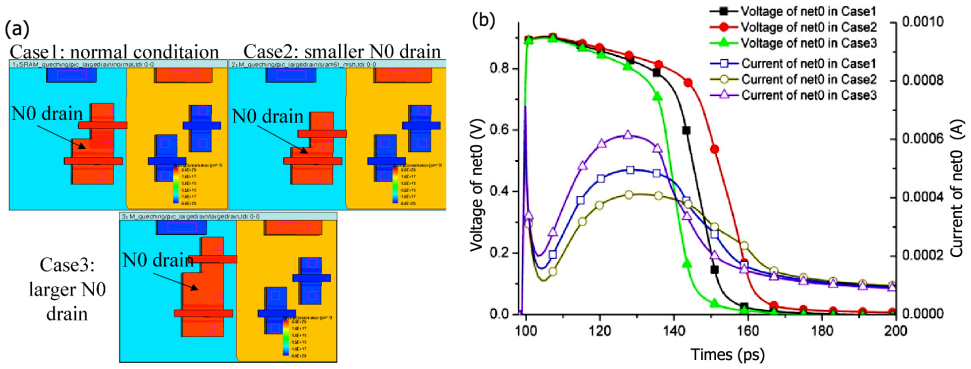

Fig. 9. (Color online) (a) Top view of the 3D TCAD block in 3 different simulation cases , and (b) voltage and current pulses of net0 for different cases at incident angle of 45° and LET of $40\,\mathrm{MeV\,cm^2/mg}$.

equal to the sum of the two upset generation times and the inverter delay in the SRAM cells. Thus, the coupling inverter delay may impact $\mathrm{SEUR_{PN}}$. The state of N0 will be changed later while increasing the coupling inverter delay, and the width of SET induced by $\mathrm{SEUR_{PN}}$ will be delayed. When the coupling inverter delay is larger than the charge collection time of NMOS, the second upset will not be triggered to induce $\mathrm{SEUR_{PN}}$. However, this event can not happen because the coupling inverter delay has a short design to increase the performance of SRAMs. Although the metal wiring delay is one part of the coupling inverter delay, it is short due to the requirement for a small area and high speed, and its effect on $\mathrm{SEUR_{PN}}$ can be neglected. The time gap between the charge collection of PMOS and the charge collection of NMOS is also a dependent parameter for $\mathrm{SEUR_{PN}}$, because it decides the time of the second upset. The spacing discussed in Sec. IV A impacts the time gap. The longer the spacing, the larger the time gap. Thus, it is indicated that the width of SET induced by $\mathrm{SEUR_{PN}}$ increases with the time gap, and reducing the time gap can increase the occurrence rate of $\mathrm{SEUR_{PN}}$.

V. CONCLUSION

In this paper, we analyzed a novel SEUR and studied its generation mechanism and characteristics in commercial $40\,\mathrm{nm}$ 6 T STAM cells by using 3D TCAD simulations. Since this SEUR is due to the charge collection of the Off-PMOS and the delayed charge collection of the On-NMOS, we called it as $\mathrm{SEUR_{PN}}$ for short and to distinguish it from other SEURs. $\mathrm{SEUR_{PN}}$ is absent when the radiation particles perpendicularly hit the center of the Off-PMOS's drain. But angular hits, which are parallel to the gates of the transistors in the layout and tilts to On-NMOS, can trigger $\mathrm{SEUR_{PN}}$ easily. The main factor of influencing $\mathrm{SEUR_{PN}}$ occurrence is whether the On-NMOS can collect enough charge to trigger the second upset after the Off-PMOS triggers the first upset. The width of SET due to $\mathrm{SEUR_{PN}}$ is the sum of the generation time of the first upset and the second upset and the delay of an inverter in the SRAM cells, and it keeps the same after LET increases to a certain value.

Additionally, we study the dependent parameters on $\mathrm{SEUR_{PN}}$, including the spacing, adjacent transistors, and drain area. Through the simulation results, it is indicated that reducing the spacing between PMOS and NMOS in the same inverter can enhance the $\mathrm{SEUR_{PN}}$, and the access pass-gate

NMOS affects the $SEUR_{PN}$ a lot due to the shared drain. The effect of the drain area of NMOS on $SEUR_{PN}$ is large, but it is a required tradeoff to enhance the $SEUR_{PN}$ by enlarging the drain area.

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